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POWER EFFICIENT DESIGN OF COUNTER ON .12 MICRON TECHNOLOGY

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Abstract— As chip manufacturing technology is suddenly on the threshold of major evaluation, which shrinks chip in size and performance is implemented in layout level which develops the low power consumption chip, using recent CMOS, micron layout tools.

This paper compares 2 architectures in terms of the hardware implementation, power consumption and CMOS layout using Microwind CMOS layout tool. Thus it provides solution to a low power architecture implementation of Counter in CMOS VLSI. The Microwind program allows the designer to design and simulate an integrated circuit at physical description level.

Index Terms— microwind, micron Technology, layout, asynchronous counter.

I. INTRODUCTION

Counters are sequential circuits that keep tract of the number of pulses applied on their inputs. They occur frequently in real-world, practical digital systems, with applications in computer systems, communication equipments, scientific instruments, and industrial control, to name a few. Many counter designs have been proposed in literature, patents, and/or used in practice. Counters are usually classified into synchronous counters, such as ring counters and twisted counters, and asynchronous counters, such as ripple counter. In CPUs, microcontrollers, DSPs and many other digital designs which include a program counter, and a timer counter, synchronous counters are usually preferred. Counters are often clocked at a very high rate, usually with an activity factor of 1. In a good design however, the activity factor can be substantially less than 1 and data-dependent leading to lower power consumption.

A counter is a logic circuit that counts the number of occurrence of an input. Each count, a binary number is called the state of the counter. Hence a counter counting in term of n bits has 2n different states. The number of different states of the counter is known as modulus of the counter. Thus, an n bit counter is a module 2n counter.

This type of asynchronous counter is also known as serial or ripples counter. The name asynchronous comes from the fact that's this counters flip flop are not being clocked at the same time. The clock input is applied only the first flip flop also called input flip flop in a cascaded arrangement. The purpose of this thesis is to design with Micro wind a 4-bit asynchronous counter with reset function. This counter will raise the output at a falling edge of the clock. The 4-stage asynchronous counter displays number from 0 to 15, using a chain of four D-register cells. The D register design has been implemented using two D Latch (master slave flip flop) with CMOS inverters.

A digital asynchronous counter is a semiconductor device that is used for counting the number of time that a digital event has occurred. The term ripple counter comes from the mode in which the clock information ripples through the counter. For designing of 4 bit asynchronous counter we need to cascade 4 D register, the clock signal of the each stage is simply carried out by the previous stage to have an asynchronous counter.

With this configuration counter will raise the output at a falling edge of the clock. The counter's output is indexed by one LSB every time the counter is clocked. The 4-stage ripple counter displays number from 0 to 15, using a chain of four D-register cell. In a counter like this after the occurrence of each clock input, the count has to wait for a time period equal to sum of all propagation delay of all flip flop before the next clock pulse can be applied .The propagation delay of each flip flop, of course , will depend upon the logic family to which it belong.

II. DESIGN APPROACH OF ASYNCHRONOUS COUNTER MODULES

Simply, to operate on n-bit values, we can connect n 1-bit Counters. 4-bit Counter is constructed using four 1-bit register as in our case.

A. Bottom – up- Approch-

In a bottom-up approach the individual base elements of the system are first specified in great detail.

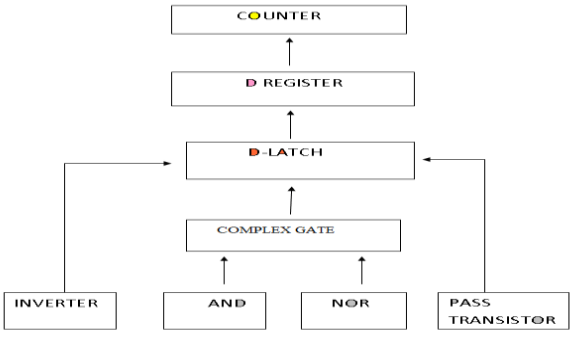

Figure-1 Bottom-up approach design

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These elements are then linked together to form larger subsystems, which then in turn are linked, sometimes in many levels, until a complete top-level system is formed many levels, until a complete top-level system is formed

III. MPLEMENTATION OF ASYNCHRONOUS COUNTER

The counter consists of four stages of cascaded D registers. The D register design has been implemented using CMOS inverter and two D latch with one clock and one input. The clock input is applied to subsequent flip flop comes from the output of its immediately preceding flip flop. For first or instance the output of the first register acts as the clock input to the second register, the output of the second register feed the clock input of third register and the output of the third register feed the clock input of fourth register. The second register can change state only after the output of first register can change its state. That is the second fact that it gets its own clock input from output of the first and not from the input clock. This time delay here the sum of propagation delay of two flip flops. So in this counter four register will change state only after a delay equal to four times the propagation delay of one flip flop.

This is binary counter, since the output is in binary system format, that is only two digits are used to represent the count that is '1' and '0'. With only 4-bits it cans only count up to '1111' or decimal number 15. Counter was designed using .12 micron technology. This chapter explains in detail the 4 bit asynchronous counter design. All of the registers have been implemented using logic gates and then using CMOS logic. Each stage is discussed in detail in the further section of this paper.

A) D Latch-

To design a D latch we use universal NAND and NOR gates. The D latch is simple gated S R latch with a NAND inverter connected between its S and R inputs. Due to inverter S and R is always be the complement of each other. Hence S= R =0 or S = R= 1, these input condition will never appear. And this will avoid the problems associated with SR= 00 and SR = 11 conditions.

To design a D latch we saw a working first, with Dsch software that when the clock is low, output is not affected. When the clock is high, the Q output is equals to input D and the notQ output is the inverse of Q.

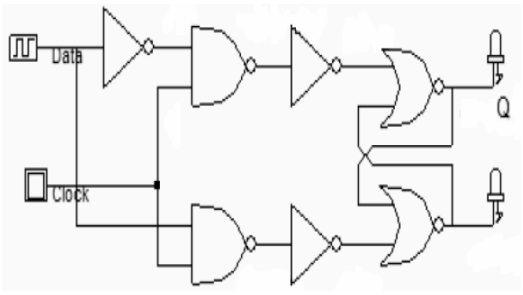

Fig. 2- schematic of D Latch

The previous implementation needs 22 transistors. In order to optimize our design, we decide to use complex gates, which only need 14 transistors. Moreover, we have better propagation delay with its implementation.

This is CMOS D Latch design by using one CMOS inverter and two complex gates. The one input is D and other is clock, and the output is Q and not Q. The Q output is same as D input. The not Q is just opposite to output Q.

B) D Register-

This 4 bit asynchronous counter is design by using four D register. Two D latch are connected in master slave structure and one D input is used to design the D register. Then we connect the clock to the master and inverse the same clock to slave. The D input of the master and the output of the slave are the input and output of the D register.

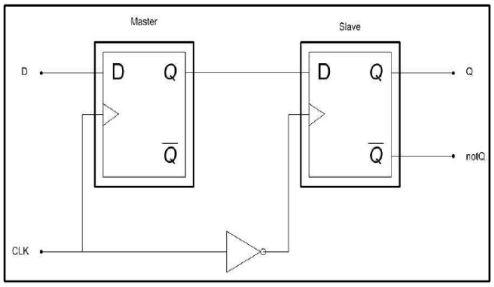

Fig.3 - schematic diagram of a NOT gate

In the following layout which represents our D register, we tried to optimize the design of the D latch (in comparison with the design of the part 2: cf. figure 6) by bringing the inverters and the complex gates closer, in order to minimize the length of the polysilicon gates. In order to have a counter with reset, we decide to add a reset to our D register. For this, we just add one NMOS to force the D input of the Slave D latch . to be at "0" since the NMOS is able to pass well the logic level 0. Thus, the Q output of the D register is "0".

We tried to force the Q output of the D register directly with a NMOS but it doesn't work as you can see on the figure 22. You can notice that this reset only forces the Q output to zero and not the notQ output of the D register

IV- OPERATION OF COUNTER

Now, as we have designed all the components of the counter, we can design it according to the schematic diagram that we have seen in the introduction (cf. figure 1). For each D register we must connect the notQ output to the D input, and the clock signal of each stage (except for the first) is simply carried out by the previous Q output. The first stage receives the clock signal. For the reset, we use the reset of our D registers and we connect them together. However, we need to change the position of the NMOS of the reset of each D register, in order to optimize our layout. Thus, we have not problems with the Q outputs of the counter when we use the reset. Firstly counter is designed by using .6 micron technology and simulate with microwind tools.

The following is a 4-bit asynchronous binary counter and

its timing diagram for one cycle. It has 16 states due to the fourth flip-flop. This counter is display 0000 to 1111 binary number. This counter is constructed by using D flip flop as master slave arrangement. This D master slave flip flop is called D register. This counter is made by four D register. Only one flip flop is connected to clock and other flip flops are clocked by previous flip flop's output. Reset is connected to all the flip flops. When least significant bit makes a transition then information is ripple through all the stats of flip flops. The clock input is applied to subsequent flip flop comes from the output of its immediately preceding flip flop. For instance the output of the first register acts as the clock input to the second register, the output of the second register feeds the clock input of third register and the output of the third register feeds the clock input of fourth register. As a natural consequence of this all 4 register do not change state at the same time .The second register can change state only after the output of first register can change its state. That is the second fact that it gets its own clock input from the output of the first and not from the input clock.

The counter's output is indexed by one LSB every time the counter is clocked. The 4-stage ripple counter displays number from 0 to 15, using a chain of four D-register cell. The Q1, Q2, Q3 and Q4 are the four states of output of the counter.

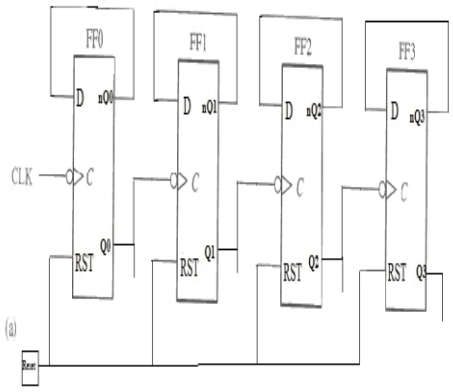

Fig. 4- 4 bit asynchronous counter using D flip flop

Table 1- 4 Bit Asynchronous Binary Counter

Clock Pulse	Q1	Q2	Q3	Q4
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

The layout of counter is design with Microwind software using λ based designing rules is shown in fig.10.

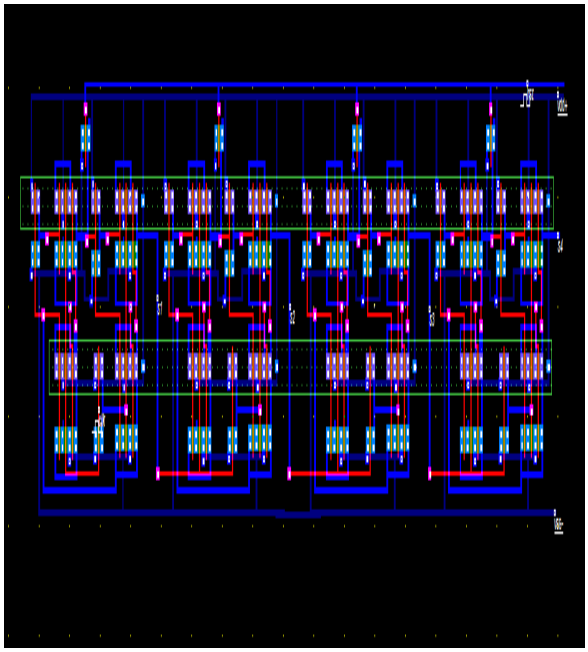

Fig.5 -Layout of counter using .6micron technology

This layout is optimized since we have connected all the Vdd sources, grounds and reset signals together. Moreover, we tried to bring all components closer to save space.

On the following simulation, we see that the truth-table of the counter is verified. It counts from (0000)2 to (1111)2. However, we notice that the outputs don't immediately fall to "0" when the reset starts. We can think with the following figure that we need to wait one "tic" of the clock to see the Q outputs which was to "1", fall to "0" (when the reset start). But the simulation of the figure 9 shows that the outputs can fall to "0" immediately when the reset start. This is the output waveform of counter using .6 micron technology .By analysis this output we get power dissipation and switching delay.

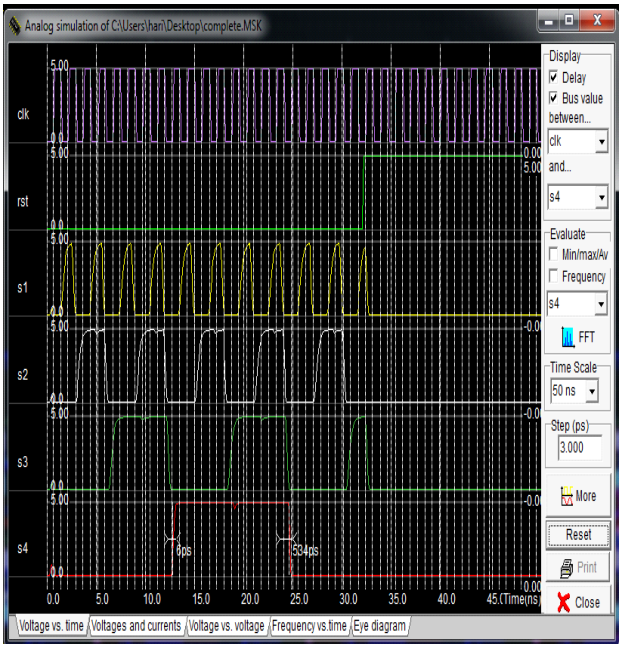

Fig. 6 -simulation of counter using .6micron technology

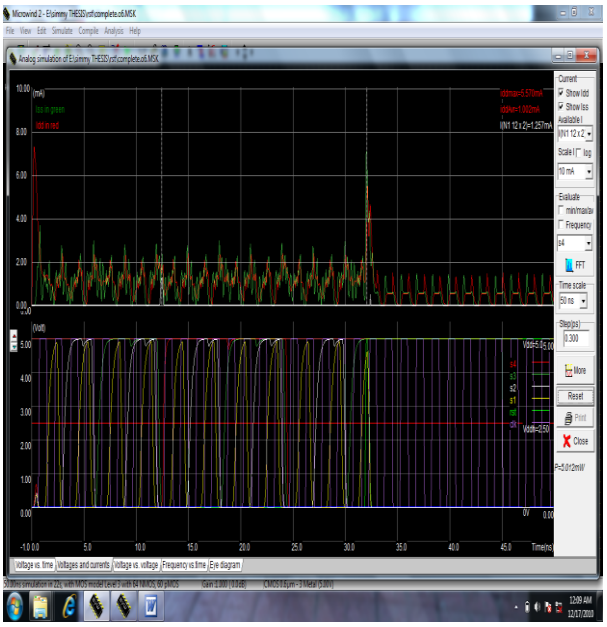

Fig. 7-voltage vs. current waveform of Counter with reset using .6µm technology

Now this layout of the counter is designed by using .12 micron technology and simulate with microwind tools.

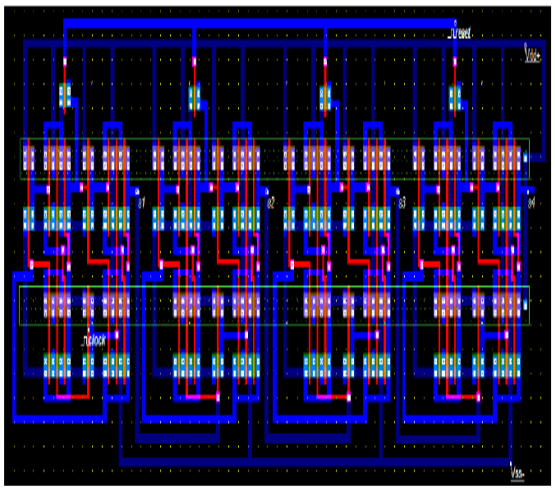

Fig.8 -Layout of counter using .12micron technology

This is the output waveform of counter using .12 micron technology. This is the timing diagram of 4 bit counter. Initial state of counter is 0000 and the last state is 1111.When reset button is switch on then output is goes to zero. Every falling edge of clock pulse the output is raise.

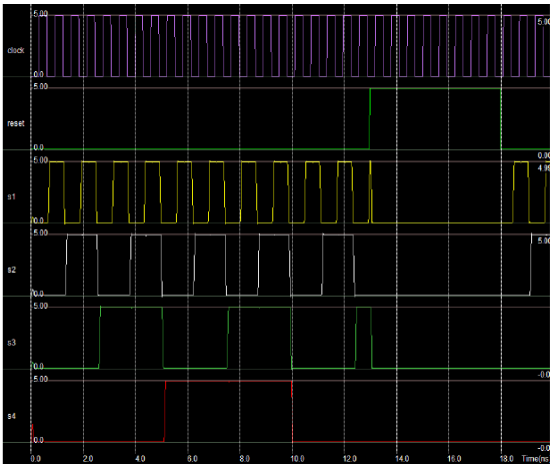

Fig-9- simulation of counter using .12micron technology

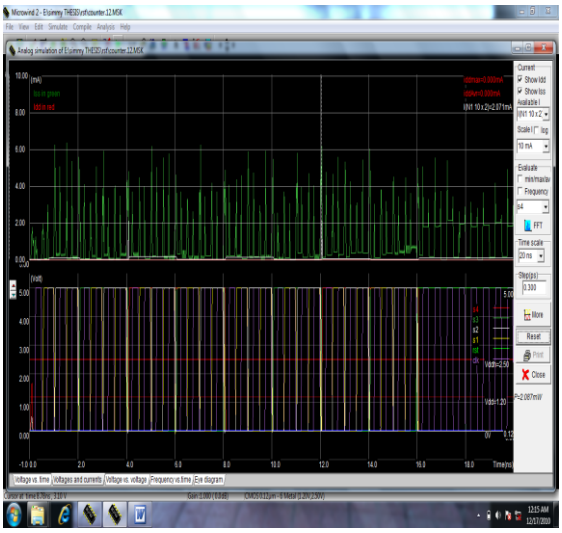

Fig. 10-voltage vs. current waveform of Counter with reset using .12µm technology

V- CONCLUSIONS

Comparison of 4 bit asynchronous counter using .6µm using Technology and .12µm Technology

Table-2 Comparison of 4 Bit Asynchronous Binary Counter

S. NO.	Parameter	.6µ Technology	.12µ Technology
1	Power consumption	4.871m W	2.087m W
2	Number of transistors	124	124
3	Switching delay	267ps	90ps
4	Layout Area	15975.7µm square	440.6µm square

This paper concludes that 4 bit asynchronous counter is best implemented using the 0.12micron technology. In this the required switching delay is minimum i.e. 90 ps, power consumption is 2.087 m. watt , Max operating frequency is 0.13 GHz, layout size area is 440.6 micro sq. meter. Thus that 4 bit asynchronous counter is best implemented using the 0.12micron technology is preferable over .6 micron technologies in maintaining the logic density in fabrication process, power optimization, reducing the propagation delay & surface area. Thus this counter implemented in CMOS chip technology, is the best illustration of VLSI.

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