

Design of an Ultra Low Power Low Phase Noise CMOS LC Oscillator

Mahdi Ebrahimzadeh

Abstract— In this paper we introduce an ultra low power CMOS LC oscillator and analyze a method to design a low power low phase noise complementary CMOS LC oscillator. A 1.8GHz oscillator is designed based on this analysis. The circuit has power supply equal to 1.1 V and dissipates 0.17 mW power. The oscillator is also optimized for low phase noise behavior. The oscillator phase noise is -126.2 dBc/Hz and -144.4 dBc/Hz at 1 MHz and 8 MHz offset respectively.

Index Terms— LC oscillator, Low Power, Low Phase Noise.

I. INTRODUCTION

Oscillators are one of the most common functional blocks in communication systems. Integrated LC Voltage Controlled Oscillators (VCOs) are used as an input for mixers to up- and down-convert signals and have particular importance in fully integrated transceivers. Proper amplitude and low phase noise are two key criteria to achieve suitable performance for a VCO in any transceiver [1]. The strong combination of very low phase noise specifications with very low power consumption (battery operation) pushes designers to use LC-VCOs. A great research effort has been invested in the design of integrated voltage controlled oscillators (VCOs) using integrated or external resonators, but as their power consumption is still unacceptable, today's mobile phones commonly use external LC-VCO modules [2].

This work aims at the overall optimized design of integrated VCOs providing differential outputs with power consumption lower than external VCO modules and lower phase noise.

The paper is organized into six sections. Section 2 discusses the complementary CMOS LC VCO structure. Section 3 and 4 cover systematic LC-VCO design for low power and low phase noise. Section 5 presents the simulation results, followed by the conclusion in Section 6.

II. COMPLEMENTARY CMOS LC VCO

The complementary cross-coupled VCO has two main advantages compared with NMOS transistors only cross-coupled topology. First, with the additional PMOS pair, the complementary topology offers higher transconductance to compensate for the loss of the tank with less current consumption and hence is more power efficient. Second, matching the PMOS and NMOS transistors, the complementary topology provides better symmetry properties

of the oscillating waveform, which decreases the upconversion of $1/f$ noise of devices to the $1/f^3$ phase noise region [3]. Another advantage of using complementary topology without current sources is increment of voltage headroom. The lower output voltage swing level may lead to degrade phase noise performance.

The complementary CMOS oscillator is depicted in Fig. 1. When the oscillation condition is satisfied, oscillation starts to develop. As the oscillation amplitude grows larger, it will reach a point where the negative resistance is not enough to support the positive resistance (loss) of the LC tank if the supply voltage and ground do not first clip the maximum swing. This is where the amplitude stops growing and a stable oscillation is reached [4]. The complementary cross-coupled oscillator shows a better phase noise performance when compared to the NMOS- or PMOS-only cross-coupled oscillators for the same supply voltage and bias current when operating at the current limited regime [5]. This is mainly because the complementary cross-coupled oscillator of Fig. 1 presents a larger maximum charge swing q_{max} than that of the NMOS- or PMOS-only cross-coupled oscillators which overall enhances its phase noise performance [6]. The complementary CMOS LC VCO structure without tail (WT) has better phase noise performance than the fixed biasing (FB) structure. The main advantage of WT topology over the FB (fixed biasing) topology is that without the tail transistor flicker noise source, the only flicker noise source now is of the cross coupled transistors, which have an inherently lower flicker noise due to the switched biasing, resulting in better phase noise performance. Another disadvantage of the FB topology compared to WT topology, is that the tail transistor in the FB topology reduces the headroom available for oscillation which is not negligible for low voltage design. A smaller signal power has an adverse effect on the phase noise, as phase noise is essentially the noise to signal ratio of the VCO. For the FB topology, extra circuitry is needed to provide biasing voltage to the tail transistor. This increases the power consumption and also introduces noise sources to the VCO. The noise current coming from the biasing network will be mirrored into the tail transistor while the WT topology does not encounter this problem [7].

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$$\left(\frac{W}{L}\right)_n = \frac{g_{m,n}^2}{I_B \cdot \mu_n \cdot C_{ox}} = 49 \quad (2)$$

$$\left(\frac{W}{L}\right)_p = \frac{g_{m,p}^2}{I_B \cdot \mu_p \cdot C_{ox}} = 150$$

To limit short channel induced excess noise, the minimum length should be avoided, so we get transistors length = 0.3 μm .

IV. PHASE NOISE

Based on Hajimiri's model the phase noise is [10]:

$$L(\Delta\omega) = 10 \log \left[\frac{\frac{i_n^2}{\Delta f} \sum_{n=0}^{\infty} c_n^2}{8q_{\max}^2 (\Delta\omega)^2} \right] \quad (3)$$

In which, c_n is the n th harmonics coefficient of the oscillator ISF (impulse sensitivity function) Fourier series expansion and q_{\max} is the maximum charge displacement in the tank circuit and $\frac{i_n^2}{\Delta f}$ is the noise power spectrum.

As mentioned in previous section lowering the value of inductor decreases the generated noise from it. Based on this the bias current required for compensating the loss of LC tank decreases which leads to decrease in the noise generated by active devices. For specified value of oscillation frequency, by decreasing inductance value we must increase capacitance value. Setting supply voltage to $v_{th,n} + v_{th,p} = 1.1\text{V}$ leads to minimize the overlap interval of NMOS and PMOS transistors and decreases the generated noise by them. All of them yield to reduce the value of phase noise.

V. SIMULATION RESULTS

To simulate the complementary CMOS LC oscillator, a 1.8 GHz oscillator using TSMC 0.18 μm CMOS process was designed. Circuit parameters of the oscillator are shown in Table 1. The design is based on low power low phase noise oscillator with supply voltage equal to 1.1 V. In this voltage oscillator dissipates 0.17 mW power and has -126.2 dBc/Hz, -144.4 dBc/Hz at 1 MHz and 8 MHz offset frequency respectively. Power consumption and phase noise versus supply voltage are shown in Fig. 2 and Fig. 3 respectively. There may be a question here that by increasing the supply voltage and in consequence in oscillator power why it improves the phase noise? It is clear that by increasing the supply voltage and output power the rate of increase in noise power is lesser. Relevant to phase noise definition that is output power over the noise power in offset frequency this can determine why the phase noise is improved. Also a window of output voltages is depicted in Fig. 4. In this figure Out n, Out P and differential output (Out N-Out P) are drawn. This is a window and the time in horizontal axes is a timeframe. The open-drain buffers M5 and M6 are employed to drive the 50 Ω load of the ADS simulator.

Table I. Circuit Parameters Of The Oscillator

Circuit Elements	Value
M ₁ , M ₂	15 μm / 0.3 μm
M ₃ , M ₄	45 μm / 0.3 μm
M ₅ , M ₆	100 μm / 0.18 μm
L	6.85 nH
C	0.99 pF

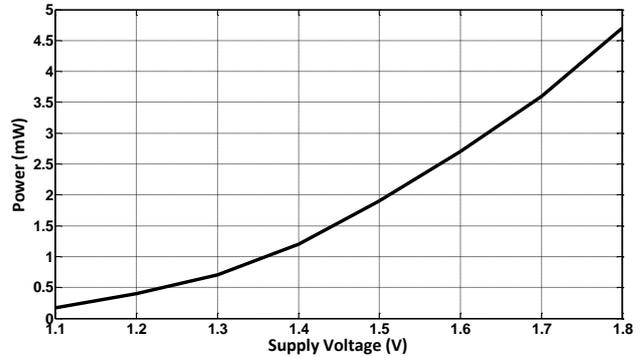


Fig. 2. Average power consumption of the oscillator versus the supply voltage.

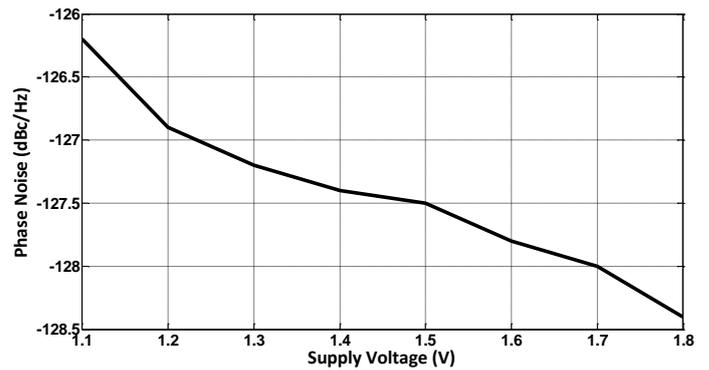


Fig. 3. Oscillator phase noise at 1MHz offset frequency versus supply voltage.

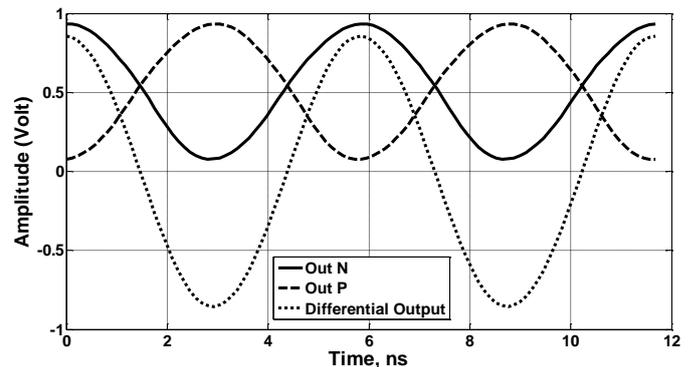


Fig. 4. Oscillator output waveforms

A comparison between this work and state of the art oscillators is shown in Table 2.

To have the best comparison between previously published oscillators those are listed in Table 2, we can use FOM definition.

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The expression for FOM that commonly used to compare oscillators is defined as:

Table II. Performance Comparison of the Oscillator

	[11]	[12]	[13]	[14]	This Work
Technology	0.18 μm	0.18 μm	0.25 μm	0.18 μm	0.18 μm
Supply Voltage	1.2 V	0.45 V	1.5 V	1.5 V	1.1 V
Power Consumption (Main Core)	2.4 mW	0.43 mW	0.08 mW	0.95 mW	0.17 mW
Frequency	5.6 GHz	2.6 GHz	2.4 GHz	2.2 GHz	1.8 GHz
Phase Noise	-119.1 dBc/Hz	-105.9 dBc/Hz	-82.4 dBc/Hz	-124 dBc/Hz	-126.2 dBc/Hz
	At 1 MHz	At 400 kHz	At 1 MHz	At 1 MHz	At 1 MHz
	Offset	Offset	Offset	Offset	Offset
FOM	190.3	185.8	161	191.1	199

$$FOM = L(\Delta\omega) + 10 \cdot \log(P_{DC,mW}) - 20 \cdot \log\left(\frac{\omega_0}{\Delta\omega}\right) \quad (4)$$

Where $L(\Delta\omega)$ is the SSB phase noise measured at $\Delta\omega$ offset from ω_0 carrier frequency and $P_{DC,mW}$ is DC power consumption in mW. This parameter for the oscillators is also listed in Table 2. As can be seen the FOM of the designed oscillator is 199 which is the best compared with the previous arts listed in Table 2.

VI. CONCLUSION

The complementary CMOS LC oscillator was analyzed to design a very low-voltage low-phase-noise oscillator. The oscillator power consumption is decreased with reducing supply voltage and it tends to reach a constant value in low supply voltages. The designed complementary CMOS 1.8GHz, 1.1 V oscillator showed 0.17 mW power consumption and -126.2 dBc/Hz phase noise at 1 MHz offset frequency.

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REFERENCES

1. W. Sheng, B. Xia, A. E. Emira, C. Xin, A. Y. V-López, S. T. Moon, and E. S.-Sinencio, "A 3-V, 0.35- μm CMOS Bluetooth Receiver IC," *IEEE Journal of Solid State Circuits*, vol. 38, no. 1, pp. 30-42, Jan. 2003.
2. M. Tiebout, "Low-Power Low-Phase-Noise Differentially Tuned Quadrature VCO Design in Standard CMOS," *IEEE Journal of Solid State Circuits*, vol. 36, no. 7, pp. 1018-1024, 2001.
3. B. De Muer, M. Borremans, M. Steyaert, G. Li Puma, "A 2-GHz low-phase-noise integrated LC VCO set with flicker-noise upconversion minimization," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 7, pp. 1034 - 1038, July 2000.
4. T. H. Lee, *The Design of CMOS Radio Frequency Integrated Circuits*, 2nd ed., Cambridge University Press, 2004.
5. Ali Hajimiri; Thomas H. Lee, "Design Issues in CMOS Differential LC Oscillators," *IEEE Journal of Solid State Circuits*, vol. 34, no. 5, pp. 717-724, May 1999.
6. Roberto Aparicio, Ali Hajimiri, "A Noise-Shifting Differential Colpitts VCO," *IEEE Journal of Solid State Circuits*, vol. 37, no. 12, pp. 1728-1736, Dec. 2002.
7. C. C. Boon, M. A. Do, K. S. Yeo, J. G. Ma, X. L. Zhang, "RF CMOS Low-Phase-Noise LC Oscillator Through Memory Reduction Tail Transistor," *IEEE Transactions on Circuits and Systems—II: Express Briefs*, vol. 51, no. 2, pp. 85-90, Feb. 2004.

8. Jannesari, A.; Kamarei, M, "Design of a Low Voltage Low-Phase-Noise Complementary CMOS VCO," *Integrated Circuits*, 2007. ISIC '07. International Symposium on, pp. 426-429, Sep. 2007.
9. A. M. Niknejad, R. G. Meyer, "Analysis, design, and optimization of spiral inductors and transformers for Si RF ICs," *IEEE Journal of Solid State Circuits*, vol. 33, no. 10, pp. 1470-1481, Oct. 1998.
10. Ali Hajimiri, Thomas H. Lee, "A General Theory of Phase Noise in Electrical Oscillators," *IEEE Journal of Solid State Circuits*, vol. 33, no. 2, pp. 179-194, Feb. 1998.
11. Sheng-Lyang Jang, Cheng-Chen Liu, Chun-Yi Wu, Miin-Horng Juang, "A 5.6 GHz Low Power Balanced VCO in 0.18 μm CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 19, no. 4, pp. 233-235, Apr. 2009.
12. Hanil Lee, Saeed Mohammadi, "A Subthreshold Low Phase Noise CMOS LC VCO for Ultra Low Power Applications," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 11, pp. 796-798, Nov. 2007.
13. Christina F. Jou, Kuo-Hua Cheng, Hsien-Cheng Hsieh, "An Ultra Low Power 2.4 GHz CMOS VCO," *International Conference on Electronics, Circuits and Systems ICECS*, vol. 3, pp. 1098-1100, Dec. 2003.
14. Shao-Hua Lee; Jang, S.-L.; Yun-Hsueh Chuang; Chao, J.-J.; Jian-Feng Lee; Juang, M.-H, "A Low Power Injection Locked LC-Tank Oscillator With Current Reused Topology," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 3, pp. 220-222, Mar. 2007.

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Mahdi Ebrahimzadeh (IEEE Student Member'08) was born in Ardakan, Iran, in 1985. He received the B.S. degree in electronics engineering from Isfahan University of Technology in 2007 and the M.S. degree in electrical engineering from Iran University of Science and Technology, Tehran, in 2010, where he is currently engaged in research toward the Ph.D. degree in electrical engineering.

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