Real-Time Threshold-Voltage Control Theory for Low Power VLSI under Variable Supply Voltage

Anubhuti Khare, Manish Saxena, Rishabh Dubey

Abstract— In the recent sub-9Onm VLSI generation, a fluctuation exists in a supply voltage due to IR-drop and inductance effects. A supply voltage fluctuation in VISI chips causes large variations in the logic delay time and power consumption. However, in conventional low-power VLSI architecture such as variable threshold voltage CMOS (VTCMOS), the threshed voltage of the transistor is fixed in advance at the system design level. As a result, VTCMOS can't compensate a supply voltage fluctuation. By employing an adaptive threshold voltage control (ATVC), minimization of power consumption under a time constraint is achieved even in the presence of n supply voltage fluctuation. Optimal granularity is discussed to minimize the total power consumption.

Key Words- Low Power, VLSI, Threshold-Voltage Control, VTCMOS

I. INTRODUCTION

A supply voltage fluctuation bas become a serious problem for designing high-performance VLSI in the recent sub-90nm generation. The resistive nature of real interconnect wires ' causes a degradation in the signal levels due to the voltage drop over the wire as shown in Fig. 1. The supply voltage fluctuation occurs especially when long interconnections are connected to many transistors. Moreover, the supply voltage fluctuation becomes large with CMOS process technology scaling down 10 90nm or below [l]. The supply voltage fluctuation becomes remarkable due to IR-drop and the induced voltage as written in Eqs. (1) and (2). Let V_{DD} be a real supply voltage superposed by fluctuation, and let V_d be a desired supply voltage.

$$V_{DD} = V_d + \Delta V \quad (1)$$

$$\Delta V = IR + L\frac{di}{dt} \quad (2)$$

The supply voltage fluctuation might change space-by-space and time-by-time in VLSI processors**.** Because of the fluctuation, power consumptions and delays will be different to each other in the modules, hence affecting the circuit total power consumption and performance. For an example, it has been shown that 10% of a supply voltage fluctuation in a 0.18µm CMOS standard design rule increases the propagation delay of the gates by up to 8% [2] and even cause the circuit to malfunction. In this paper, we compensate the supply voltage fluctuation by using a control circuit, where the threshold voltage of a transistor is controlled, adaptively. We assume that power consumption of the control circuit is small enough, while leakage power consumption of a module ***is*** dominant in its total power consumption.

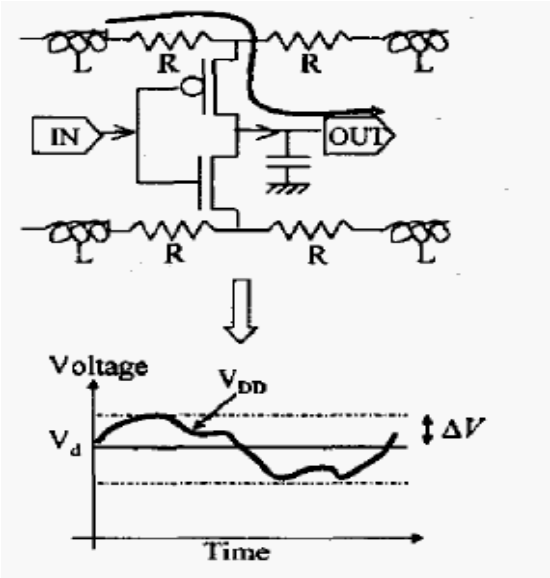

Fig. 1. Supply voltage fluctuation.

The leakage current and the delay in the CMOS gate can be controlled to some extent by changing the body bias voltage of a transistor [3]. There are two ways in controlling the threshold voltage. They are reverse body bias (RBB) [4] and forward body bias (FBB) [5]. REB is used to reduce leakage power consumption effectively by increasing the body bias voltage of a PMOS transistor to be larger than a supply voltage. For an nMOS transistor, the body bias voltage is reduced to be lower than ground. These changes increase the threshold voltage and reduce the leakage current. FBB is used to decrease the threshold voltage and improving circuit performance although it increases leakage power consumption. Both RBB and FBB are commonly used to realize an adaptive threshold voltage control. Figure 2 shows an example the effect of the body bias voltage under RBB and FBB.

The proposed approach is different from a variable threshold voltage CMOS (VTCMOS) scheme [6]. In the VTCMOS scheme, the threshold voltage is fixed which is determined in advance. However, in the adaptive threshold voltage control, the threshold voltage changes according to the deviation of the supply voltage.

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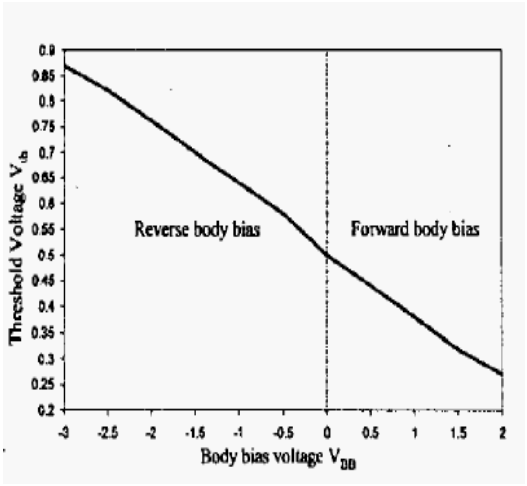

Fig. 2. Effect of the body bias voltage.

II. ADAPTIVE THRESHOLD VOLTAGE CONTROL

Usually, the body bias voltage of a conventional CMOS logic circuit is connected to a supply voltage in a pMOS transistor and to the ground in an nMOS transistor. RBB and FBB can be effectively used to control the threshold voltage Vth because of the supply voltage fluctuation around Vd. A real-time adaptive threshold voltage control (ATVC) scheme is proposed to minimize leakage power consumption under a time constraint even in the presence of a supply voltage fluctuation.

There are three components that establish tbe amount of power consumption P in a CMOS circuit. They are dynamic power consumption, power consumption due to direct-path currents and static power consumption as written in Eq. (3), where pt is the switching activity, C is the output capacitive load. idp is the direct-path current, fclk is the clock frequency and Ileak is the leakage current.

$$P = (p_t C V_{DD}{}^2 + \int i_{dp} dt V_{DD}) f_{clk} + I_{leak} V_{DD} \quad (3)$$

Dynamic power consumption is due **to** the charging and discharging of a load capacitance, while static power consumption is due to I_{leak}. I_{leak} is given by Eq. (4), where I_0 is a constant and S is the sub threshold swing. From Eq. (4), a small change in V_{th} makes a large change in I_{leak}**.** The delay time t_d is given by Eq(5.) where k is a constant.

$$I_{leak} = I_o 10^{-V_{th}/S} \quad (4)$$

$$t_d = \frac{kCV_{DD}}{(V_{DD} - V_{th})^\alpha} \quad (5)$$

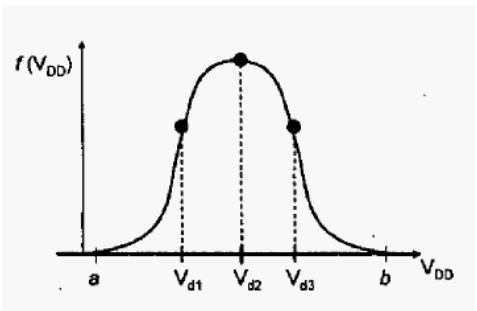

Fig. 3. Probability density function

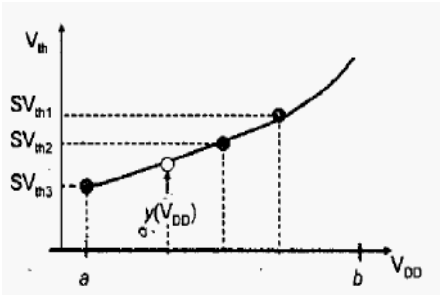

Fig. 4. Example of the 3 threshold voltage levels.

From Eqs. (3) and (5), P is small but td becomes large if VDD is low, so that I/th has to be decreased to retain the speed. If VDD is high, the higher Vth reduces Ileak under the time constraint, and we can save leakage power consumption. Leakage power consumption is reduced by increasing Vth when VDD>Vd. On the other hand, the delay time is retained under the time constraint by lowering Vth when VDD<Vd.

Let the distribution due to supply voltage fluctuation be a<VDD<b. On example of supply voltage distribution is shown in Fig. 3, where f(VDD) is a probability density function for VDD. Let us consider a combination of a sup ply voltage and the associated threshold voltage of (VDD, y(VDD)). Each combination gives the delay time equal to the time constraint. There is no wasted leakage current in such a combination, because the leakage power consumption is being minimized under the time constraint. That is, the combination is optimal.

The number of the selected threshold voltages is set to M, and they are defined to be SVthj (j=1,2,3,..,M). For an example, let us consider 3 threshold voltage levels as shown in Fig, 4. SVth1 and SVth3 and are the selected threshold voltages. As one of the selected threshold voltages y(VDD=a) must be included, so that the time constraint condition can be satisfied for possible values of VDD. The expected value of the wasted current E is given by Eq. (6). We select the M-threshold voltages such that E becomes minimum.

$$E = \int_a^b f(V_{DD})(I_{leak}(SV_{thj}) - I_{leak}(y(V_{DD})))dV_{DD} \quad (6)$$

The leakage current becomes Ileak(SVthj), when SVthj is selected. Similarly, the leakage current, becomes Ileak(y(VDD)) ,when y(VDD) is selected. If possible combinations of SVthl, SVth2 and SVth3 are substituted in Eq. (6), the expected value will change. The minimum expected value leads to the optimal selection of the threshold voltages for SVth1, SVth2 and SVth3.

Under the condition, there are possibilities M threshold voltage levels that can be chosen considering trade-off between power consumption of the control circuit and leakage power consumption of the module. If the number of the threshold voltage levels is increased, power consumption of the control circuit increases but leakage power consumption of the module decreases. By considering the trade-off, we find the total power consumption PM. Let us consider leakage power consumption of the module as g(M) and power consumption of the control circuit as h(M). The summation of both power consumptions are expressed as Eq. (7). If PM IS minimum, M becomes the optimal number of the threshold voltage levels.

$$P_M = min(g(M) + h(M)) \quad (7)$$

If there is no fluctuation, Vth is set to the default threshold voltage and the delay time becomes the time constraint T. Incorrect value of T causes inaccurate value of the optimal threshold voltage.

We assume that Vth=|Vthp|=Vthn, where Vthp and Vthn are the threshold voltages of a pMOS transistor and an nMOS transistor, respectively. The selected threshold voltages are given by Eq. (8). where SVth1>SVth2>.... >SVthM.

$$SV_{th} = \begin{cases} SV_{th1} & \text{if } SV_{th1} \text{ satisfies } t_d \le T. \\ SV_{th2} & \text{if } SV_{th2} \text{ satisfies } t_d \le T \text{ and} \\ & SV_{th1} \text{ does not satisfy } t_d \le T. \\ & \cdots\cdots \\ & \cdots\cdots \\ SV_{thM} & \text{if } SV_{thM} \text{ satisfies } t_d \le T \text{ and} \\ & SV_{thM-1} \text{ does not satisfy } t_d \le T. \end{cases} \quad (8)$$

Figure 5 shows the proposed system composed of a module and a control circuit. The control circuit is composed of the voltage comparators and the voltage selectors. The voltage comparator compares VDD with the reference voltage. The voltage selector is used to select the pMOS and nMOS body bias voltages. Figure 6 shows a schematic diagram of ATVC as an example.

III. OPTIMAL GRANULARITY

Let us consider a module composed of NAND gates as an example. It is unpractical to have a control circuit for each NAND gate. Design optimization is necessary in order to obtain the optimal granularity of a module as shown in Fig. 7. Let the number n of NAND gates be fixed, while let the number N of the control circuits be variable. The optimal granularity of the module is determined by choosing an appropriate number of the control circuits considering trade-off between power consumption, the hardware complexity and the driving capability. As shown in Table 1, if the number of the control circuits becomes large, the driving capability for each module will become high and this leads to better response. On the contrary, power consumption in the control circuits becomes large in proportionate to the hardware complexity.

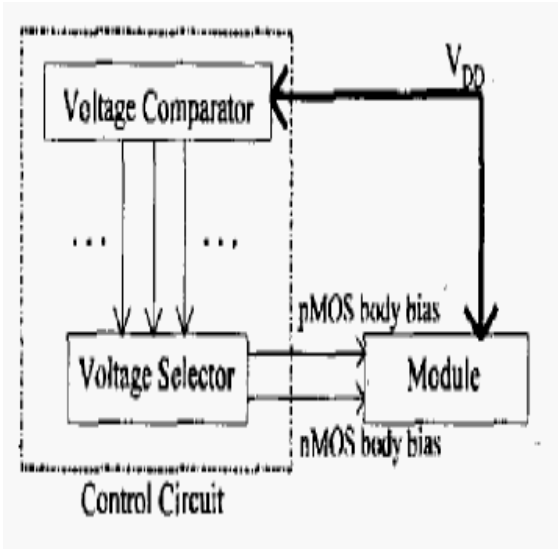

Fig. 5. Block diagram of ATVC.

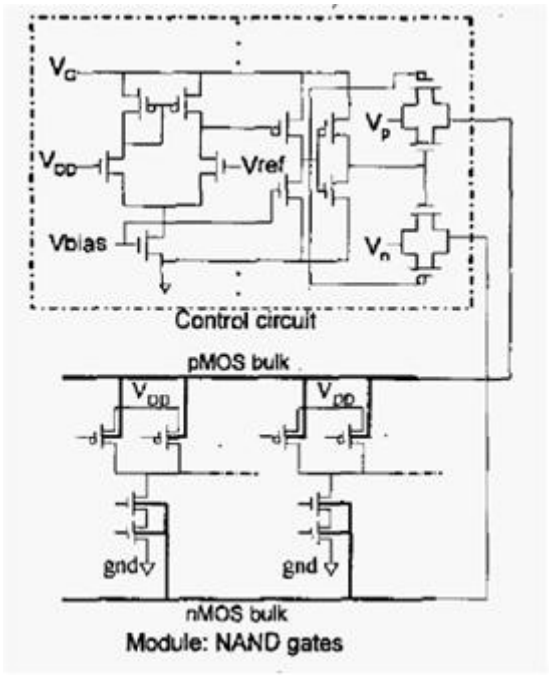

Fig. 6. Schematic diagram of ATVC.

We assume that the supply voltages at each NAND gate in a module are equal to each other, so that we can connect the gates to the same bulk. The supply voltages in the module might be different between modules although it is connected to the same power supply line. The optimal granularity of the module is achieved if the driving capability is satisfied, where the control frequency is higher than the supply voltage fluctuation rate.

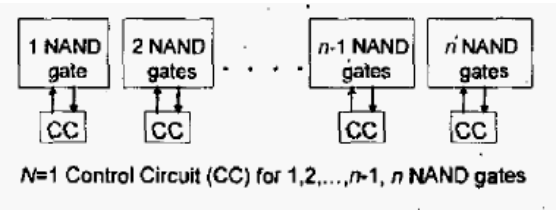

Fig. 7. Module size n versus a single control circuit N=l.

TABLE I. Trade-off between consumption. Drlving capability and 'hardware complexity in the control circuit

Number of the control circuits	Power consumption of the control circuits	Driving capability	Hardware complexity
Small	Small	Low	Small
Large	Large	High	Large

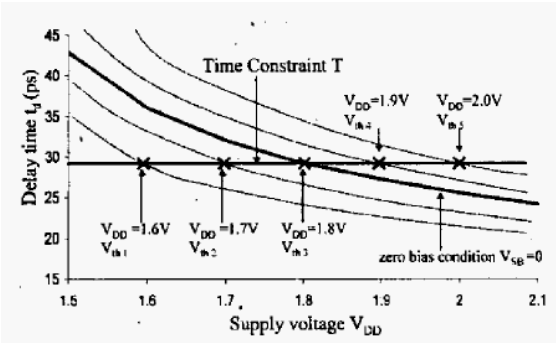

Fig. 8. Delay time for VDD and Vth

IV. SIMULATION AND EVALUATION

As an example, let us consider a module composed of l00, 000 NAND gates. Using 0.18µm CMOS standard design rule, ATVC is verified on HSPICE simulation. Leakage power consumption is assumed to be 80% larger than dynamic power consumption in the module. The control frequency is about 9 times higher than the supply voltage fluctuation rate as an example. We assume that the optimal threshold voltage levels is 5 and the optimal granularity of the module he 10,000 NAND gates per control circuit. The delay time for VDD and Vth are simulated as shown in Fig. 8. Let Vd be 1.8V. Table 2 shows how leakage power consumption is minimized under a time constraint if there is a supply voltage fluctuation. Figure 9 summarizes the ATVC scheme.

TABLE II. Delay time and energy consumption in an atvc example.

V_{DD} [V]	SV_{THi} [V]	Delay t_d(ps)	Energy of the Control [x 10^{-5}]	Energy of the Module [x 10^{-3}]
1.90	0.56	29.2	46.7	30.8
1.85	0.53	28.9	45.4	32.2
1.80	0.50	29.2	44.2	34.4
1.70	0.45	29.0	41.8	37.9
1.60	0.42	29.1	39.3	41.3

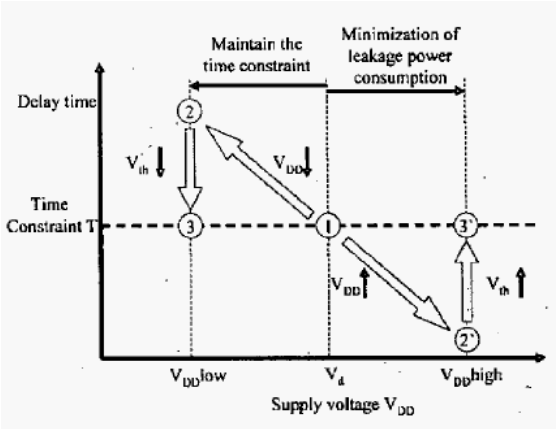

Fig. 9. Summary of ATVC.

V. CONCLUSION

A real-time ATVC scheme using body bias control is proposed to compensate a supply voltage fluctuation. The technique is useful to minimize leakage power consumption under a time constraint. The proposed concept is extended to a software control scheme.

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