Constant Bit Rate Traffic Investigation for Network-on-Chip

Naveen Choudhary

Abstract*— Scalable Networks on Chips (NoCs) are needed to match the ever-increasing communication demands of large-scale Multi-Processor Systems-on-chip (MPSoCs) for high-end wireless communications applications. The heterogeneous nature of on-chip cores, and the performance efficiency requirements typical of high end computing devices call for efficient NoCs architecture which eliminate much of the overheads connected with general-purpose communication architectures. This paper evaluates the performance of regular and Irregular NoC for constant bit rate traffic pattern for various routing algorithms such as X-Y, O-E, Up*/down*. The performance of NoC with varying number of cores is evaluated on the systemC based discrete event, cycle accurate NoC performance simulator.

Index Terms*— NoC, SoC, simulation, traffic pattern, Topology.

I. INTRODUCTION

Modern embedded systems are becoming increasingly complex. With the limitation of semiconductor industry, present-day designs go towards the development of on-chip multi-processor systems. The design focus moves from a computation centric view to a communication centric one. Networks-on-Chip (NoC) is a newly proposed paradigm for System-on-Chip (SoC) which borrows variable concepts from macro-network to build large on-chip networks [1], [2]. As shown in Figure 1, each node (or tile) in the on-chip network is composed of a Processing Element (PE) and a communication unit which is so called a Network Interface (NI). The NI is actually implemented by a Router component in NoC. The communication between the pairs of nodes is organized by connecting a network of routers and switching packages among them. Compared to traditional bus based on-chip communication architecture. The NoC solution provides higher communication scalability, flexibility, predictability, power efficiency and support of Quality-of-Service (QoS).

With the advancement in deep-submicron technology it is now feasible to have huge number of transistors on a single chip now. This allows the present day designers to integrate tens or hundreds of IP blocks together with large amounts of embedded memory. These IP can be CPU or DSP cores, video streaming processors, high-bandwidth I/O, etc [3]. This richness of the computational resources places tremendous demands on the communication resources as well. Additionally, the shrinking feature size in the deep-submicron (DSM) domain makes interconnect delay and power consumption the dominant factors in the optimization of modern systems. Another consequence of the DSM is the difficulty in optimizing interconnects due to the worsening effects such as crosstalk, electro-magnetic interference and soft errors, etc [4].

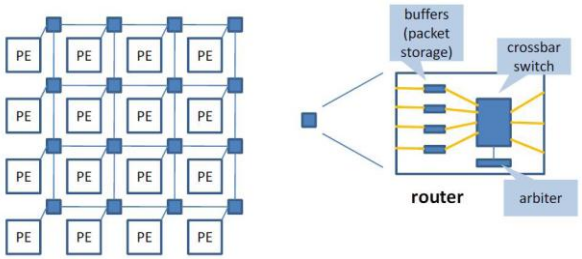

Fig. 1. NoC with 2D-Mesh topology and typical on-chip router architecture

To date, the shared-bus scheme (either single bus or multi-bus) has been the system communication architecture of choice. However, there are several problems associated with the standard bus architectures.

- First, a global bus implies a large capacitive load for the bus drivers. In turn, this implies large delays and huge power consumption.
- Second, the performance of shared bus architecture is inherently non scalable as there can be at most one transaction over the shared bus at any point of time. Moreover, the bus performance has to be degraded if a slow device is accessing the bus. To address this problem, some sophisticated modern bus architectures address this problem through the concept of bus hierarchy and separation. For instance, both the newest IBM Core Connect bus architecture [5] and the ARM AMBA bus architecture [6, 7] divide the bus sub-system into high-speed processor bus, system bus and low-speed peripheral bus which are connected by bridges. However, such a temporary solution falls short when hundreds or over thousands of processors will have to be integrated on a single chip in the near future [4].
- Third, in DSM era, design of long, wide buses becomes a real challenge. While physical information is extremely important for successful bus design, the environment in which the bus is embedded is very hard to predict and characterize early in the design stages.

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Naveen Choudhary, Department of Computer Science and Engineering, College of Technology and Engineering, Maharana Pratap University of Agriculture and Technology, Udaipur, Rajasthan, India, Mobile No: +91-9352356102, (e-mail: naveenc121@yahoo.com).

The scalability and success of switch-based networks and packet-based communication in parallel computing and Internet has inspired the researchers to propose the Network-on-Chip (NoC) architecture as a viable solution to the complex on-chip communication problems [1, 2, 8].

In this paper we analyze the performance of regular and Irregular NoCs for various routing schemes with constant bit rate traffic patterns. Section 2 presents ate basic architecture and modeling issues of the NoC. Section 3 explains some popular routing schemes for regular 2D-mesh based NoC architecture. The routing issues in Irregular NoC are presented in section 4. The performance comparison of application optimized regular and irregular topology based NoCs for various routing function is presented in section 5 and in Section 6 we conclude.

II. NOC ARCHITECTURE

The NoC contains the following three fundamental components Network adapters, Routing nodes and Links. Network adapters implement the interface by which cores (IP blocks) connect to the NoC. Their function is to decouple computation (the cores) from the communication (network). Routing nodes route the data according to chosen protocols. They implement the routing strategy. Links connect the nodes, providing the raw bandwidth. They may consist of one or more logical or physical channels. An on-chip network is defined mainly by its topology and the protocol implemented by it. Topology concerns the layout and connectivity of the nodes and links on the chip. Protocol dictates how these nodes and links are used.

A. Topology

One simple way to distinguish different regular topologies [9] is in terms of *k-ary n-cube* (grid-type), where *k* is the degree of each dimension and *n* is the number of dimensions [10]. The *k-ary tree* and the *k-ary n-dimensional* fat tree are two alternate regular forms of networks explored for NoC. The network area and power consumption scales predictably for increasing size of regular forms of topology. Most NoCs implement regular forms of network topology that can be laid out on a chip surface (a 2-dimensional plane) for example, k-ary 2-cube, commonly known as grid-based topologies. The Octagon NoC is an example of a novel regular NoC topology. Its basic configuration is a ring of 8 nodes connected by 12 bidirectional links which provides two-hop communication between any pair of nodes in the ring and a simple, shortest-path routing algorithm. Such rings are then connected edge-to-edge to form a larger, scalable network. For more complex structures such as trees, finding the optimal layout is a challenge on its own right. Besides the form, the nature of links adds an additional aspect to the topology. In k-ary 2-cube networks, popular NoC topologies based on the nature of link are the mesh which uses bidirectional links and torus which uses unidirectional links. Generally, mesh topology makes better use of links (utilization), while tree-based topologies are useful for exploiting locality of traffic. In tree based topology, the root tile is generally the HotSpot as most of the traffic traverses through this tile

B. Routing and Switching in NoC

Switching can be defined as the mere transport of data, while routing is the intelligence behind it, that is, it determines the path of the data transport [9]. Different aspects of protocol that are commonly addressed in NoC research domain are circuit or packet switching, connection-oriented or connectionless, deterministic or adaptive, minimal or non-minimal routing, Central or distributed control. Circuit switching involves the circuit from source to destination that is setup and reserved until the transport of data is complete. Packet switched traffic, on the other hand, is forwarded on a per-hop basis, each packet containing routing information as well as data.

Connection-oriented mechanisms involve a dedicated (logical) connection path established prior to data transport. The connection is then terminated upon completion of communication. In connectionless mechanisms, the communication occurs in a dynamic manner with no prior arrangement between the sender and the receiver. Thus circuit switched communication is always connection-oriented, whereas packet switched communication may be either connection-oriented or connectionless.

Routing in NoC [9] can be deterministic or adaptive. In a deterministic routing strategy, the traversal path is determined by its source and destination alone. Popular deterministic routing schemes for NoC are source routing and XY routing (2D dimension order routing). In source routing, the source core specifies the route to the destination. In an adaptive routing strategy, the routing path is decided on a per hop basis. Adaptive schemes involve dynamic arbitration mechanisms, for example, based on local link congestion. This results in more complex node implementations but offers benefits like dynamic load balancing. Similarly a routing algorithm is minimal if it always chooses among shortest paths toward the destination; otherwise it is non-minimal.

In centralized control mechanisms, routing decisions are made globally, for example, bus arbitration. In distributed control, most common for irregular topology based NoCs, the routing decisions are made locally. The protocol defines the use of the available resources, and thus the node implementation reflects design choices based on the listed terms. The major components of any routing node are buffers, switch, routing and arbitration unit, and link controller [9]. The switch connects the input buffers to the output buffers, while the routing and arbitration unit implements the algorithm that dictates these connections. In a centrally controlled system, the routing control would be common for all nodes, and a strategy might be chosen which guarantees no traffic contention. Thus no arbitration unit would be necessary. Such a scheme can be employed in a NoC in which all nodes have a common sense of time.

The wide majority of NoC research is based on packet switching networks. The most common switching or data forwarding strategies are store-and-forward, wormhole, and virtual cut-through. The NoC generally follow the delay model of communication in which data can be delayed but is never dropped in it way from source core to sink core. Store-and-forward switching is a packet switched protocol in which the node stores the complete packet and forwards it based on the information within its header. Thus the packet may stall if the router in the forwarding path does not have sufficient buffer space.

Virtual cut-through routing has a forwarding mechanism similar to that of wormhole routing. But before forwarding the first flit of the packet, the node waits for a guarantee that the next node in the path will accept the entire packet. Thus if the packet stalls, it aggregates in the current node without blocking any links.

Wormhole routing combines packet switching with the data streaming quality of circuit switching to attain minimal packet latency. The node looks at the header of the packet to determine its next hop and immediately forwards it. The subsequent flits are forwarded as they arrive. This causes the packet to worm its way through the network, possibly spanning a number of nodes, hence the name. The latency within the router is not that of the whole packet. A stalling packet, however, has the unpleasantly expensive side effect of occupying all the links that the worm spans. Virtual channels can relieve this side effect at a marginal cost. While macro-networks usually employ store-and-forward routing, the prevailing scheme for NoC is wormhole routing. The major benefit of using wormhole switching includes low latency and the avoidance of area costly buffering queues in the routers.

C. Virtual Channels and Flow Control in NoC

Flow control [9] can be defined as the mechanism that determines the packet movement along the network path. Thus it encompasses both global and local issues. Flow control mainly addresses the issue of ensuring correct operation of the network. In addition, it can be extended to include issues on utilizing network resources optimally and providing predictable performance of communication services. Flow control primitives thus forms the basis of differentiated communication services.

Virtual channels (VCs) [9] are the sharing of a physical channel by several logically separate channels with individual and independent buffer queues. Generally, the number of VCs that has been proposed for NoC ranges between 2 and 16 per physical channel. Their implementation results in an area and possibly also power and latency overhead due to the cost of control and buffer implementation. There are however a number of advantages of VCs like avoiding deadlocks. Since VCs are not mutually dependent on each other, by adding VCs per link and choosing the routing scheme properly, one may break cycles in the resource dependency graph to avoid deadlocks. Virtual channels are also helpful in increasing wire utilization, improve performance and for provide differentiated services.

III. ROUTING FUNCTIONS FOR REGULAR NOC

Routing is the process of selecting paths in computer networking along which to send data or physical traffic. Routing algorithms are responsible for correctly and efficiently routing packets or circuits from the source to destination [9].

Routing schemes are usually categorized into two folds: static (deterministic) routing and dynamic (adaptive) routing. Deterministic routing means routing paths are completely determined offline, while adaptive routing is that paths are online determined depending on dynamic network conditions. Deterministic routing has design simplicity and low latency under loose network traffic, but performs throughput degradation when network congestion happens. Adaptive routing uses alternative paths when network is congested, which provides higher throughput, while it will experience higher latency if network congestion is low.

In NoCs, the routing scheme usually selects candidates among the routing paths that have minimum distance between the source and destination nodes. There are many routing algorithms available [9]. The Dimension order routing or XY [9] routing and odd-even routing [11] are popular routing schemes for the 2D-Mesh regular NoCs. They are both theoretically guaranteed to be free of deadlock [9] and livelock [9]. The XY routing strategy can be applied to regular two-dimensional mesh topologies without obstacles. The position of the mesh nodes and their nested network components is described by coordinates, the *x-coordinate* for the horizontal and the *y-coordinate* for the vertical position. A packet is routed to the correct horizontal position first and then in vertical direction. XY routing produces minimal paths without redundancy, assuming that the network description of a mesh node does not define redundancy.

The odd-even [11] turn model is a shortest path routing algorithm that restricts the locations where some types of turns can take place such that the algorithm remains deadlock-free [9]. More precisely, the odd-even routing prohibits the east to north and east to south turns at any tiles located in an even column. It also prohibits the north to west and south to west turns at any tiles located in an odd column.

IV. ROUTING FUNCTIONS FOR IRREGULAR NOC

Prominent examples of topology agnostic table based distributed routing algorithms are up*/down* [12] [18], Left-Right [13], L-turn [13], DOWN/UP [14], prefix-routing [15], smart-routing [16], and FX [17]. These algorithms have in common that they are based on turn prohibition, a methodology which avoids deadlock [9] by prohibiting a subset of all turns in the network. The up*/down* routing is a popular choice for Irregular and is therefore explained in some detail in this Section. The interconnection network between switches can be modeled by a multigraph G (N, C), where N is the set of switches and C is the set of bidirectional links between the switches as shown in Figure 2. The routing scheme used in Autonet, commonly known as up*/down* routing [12], is deadlock-free. The Autonet routing algorithm is distributed, and implemented using table-lookup. When a message reaches a switch, the destination address stored in the message header is concatenated with the incoming port number, and the result is used to index the routing table at that switch. The table lookup returns the outgoing port number that this message should be routed through. When multiple valid routes exist from the current switch to the destination, the routing table returns all the alternative outgoing ports. In the case that multiple outgoing ports are free, the routing scheme selects the one with the lower identifier. The routing table in each switch must be filled before messages can be routed. To do so, a breadth-first spanning tree (*BFS*) on the graph G is computed first using a distributed algorithm. This algorithm has the property that all the switches in the network will eventually agree on a unique spanning tree.

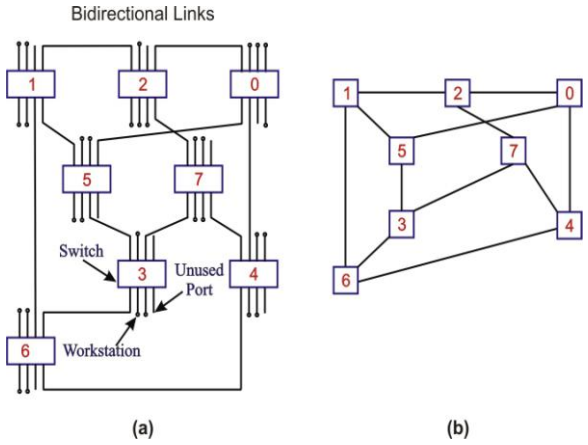


Fig. 2. (a) A network of workstations with switch-based interconnect and irregular topology (b) The corresponding graphs G

Routing is based on an assignment of direction to the operational links, including the ones that do not belong to the tree. In particular, the "up" end of each link is defined as: 1) the end whose switch is closer to the root in the spanning tree; 2) the end whose switch has the lower ID, if both ends are switches at the same tree level (Figure 3). Links looped back to the same switch are omitted from the configuration. The result of this assignment is that each cycle in the network has at least one link in the "up" direction and one link in the "down" direction. To eliminate deadlocks while still allowing all links to be used, the up*/down* routing algorithm uses the following rule: a legal route must traverse zero or more links in the "up" direction followed by zero or more links in the "down" direction. Thus, cyclic dependencies between channels are avoided because a message cannot traverse a link along the "up" direction after having traversed one in the "down" direction. Such routing not only guarantees deadlock-freedom, but also provides some adaptivity. The lookup tables can be constructed to support both minimal and nonminimal adaptive routing. However, in some cases, up*/down* routing is not able to supply any minimal path between some pairs of switches, as shown in the following example.

Figure 3 shows the example irregular network of the network shown in Figure 2(a). Switches are arranged in such a way that all the switches at the same tree level are at the same vertical position in the figure. The root switch for the corresponding *BFS* spanning tree is switch 0. The assignment of "up" direction to the links in the network is illustrated. The "down" direction is along the reverse direction of the link. Note that every cycle has at least one link in the "up" direction and one link in the "down" direction. It can be observed that all the alternative minimal paths are allowed in some cases. This is the case when the destination host is connected to the root switch. For example, a message transmitted from switch 7 to switch 0 can be routed either through switch 4 or switch 2. In some other cases, however, only some minimal paths are allowed. For example, a message transmitted from switch 2 to switch 5 can be routed through switch 0 but it cannot be routed through switch 1. It should be noted that any transmission between adjacent switches is always allowed to use the link(s) connecting them, regardless of the direction assigned to that link. However, when two switches are located two or more links away, it may happen that all the minimal paths are forbidden. This is the case for messages transmitted from switch 4 to switch 1. The only minimal path (through switch 6) is not allowed, because it requires one transition from "down" to "up" direction. All the allowed paths (through switches 0, 2, and through switches 0, 5) are nonminimal since they require three hops, while the illegal path through switch 6 requires only two hops.

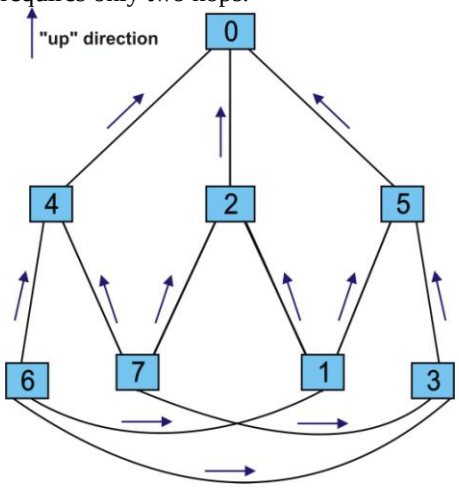


Fig. 3. Link direction assignment for network in Figure 2

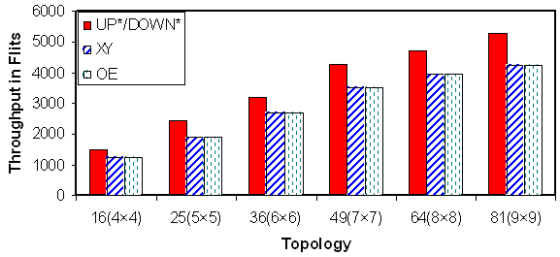
This problem with minimal paths becomes more important as network size increases. In general, up*/down* concentrates traffic near the root switch, providing minimal paths only between switches that are located near the root switch. In most cases, only nonminimal paths are provided between nonadjacent switches located far from the root switch. Thus, the percentage of nonminimal paths increases with network size. Additionally, the concentration of traffic in the vicinity of the root switch produces a premature saturation of the network near the root switch, thus reducing network throughput. Also, it leads to uneven channel utilization. However if the topology is designed according to the application and up*/down* routing requirement than this routing can also perform quite efficiently.

V. EXPERIMENTAL RESULTS

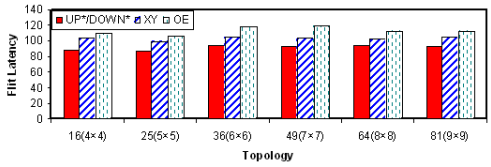
For analyzing the performance of various routing algorithms for irregular and regular NoCs with constant bit rate traffic on NoC simulation framework, a discrete event, cycle accurate simulator called *IrNIRGAM* [19] is used. *IrNIRGAM* is an extension of NIRGAM [20]. *IrNIRAGM* is a cycle-accurate SystemC based simulator for regular and irregular topology based NoC framework supporting various routing schemes. For *IrNIRGAM* a wormhole switching based network architecture is implemented, where an IP Core directly connected to a dedicated router, is assumed (*Direct Network*). In general, the topology represents the most important characteristic of NoC architectures. It defines how router nodes are physically interconnected and has a predominant influence on network performance and implementation costs.

In *IrNIRGAM*, input buffered routers can have multiple virtual channels (VCs) and uses wormhole switching for flow control. The packets are split into an arbitrary number of flits (flow control units) and forwarded through the network in a pipelined fashion. A Round-Robin scheme for switch arbitration is used in the router nodes to provide fair bandwidth allocation while effectively preventing scheduling anomalies like starvation.

For performance comparison of constant bit rate traffic patterns on NoCs, the *IrNIRGAM* was run for 10000 clock cycles and network throughput in flits and average flit latency were used as parameters for comparison. Network throughput is the number of flits received by various cores of the NoC during the simulation run. The flit latency determines the number of clock cycles it takes from entering the network until the reception at the target node. All data queues in the network routers can buffer eight flits per channel.



(a)

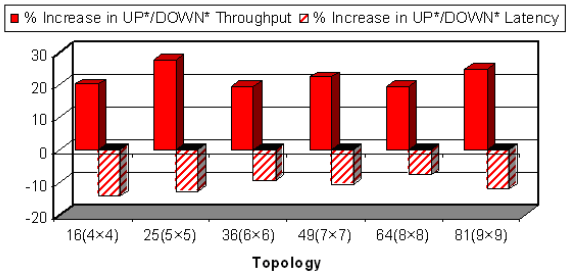


(b)

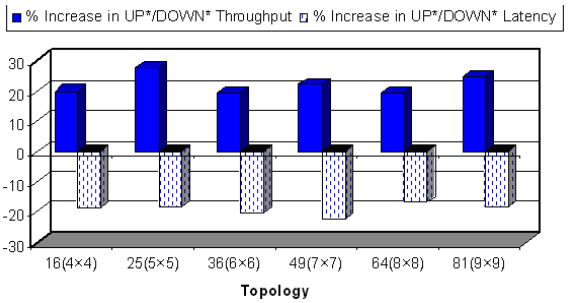
Fig. 4. Performance results of communication requirement optimized irregular NoC and 2D Mesh regular NoC for constant bit rate traffic (a) Throughput (in its) and (b) Flit latency (in clocks)

In general, the topology represents the most important characteristic of NoC architectures. It defines how router nodes are physically interconnected and has a predominant influence on network performance and implementation costs. Keeping this in view in our experimental analysis we have chosen application optimized NoC. For Irregular NoC the optimized communication performance based topology is designed using the methodology presented in [21]. Similarly for regular NoC, the communication performance optimized task to core mapping is dune using the intelligent mapping scheme proposed in [22].

Figure 4 summarizes the comparative performance results of various constant bit rate traffic patterns averaged over 50 communication requirement optimized irregular NoCs with permitted node/core degree of 4 for number of cores varying between 16 to 81 and 2D-mesh NoC with communication requirement optimized intelligent task to core(tile) mapping as proposed in [22] and same number and size of with XY and OE (odd-even) routing. For Irregular NoCs table based distributed up*/down* routing [12] supporting deterministic deadlock free routing function was used and the permitted channel length was taken as 2 times the length of the core/tile.



(a)



(b)

Fig. 5. Performance comparison of communication requirement optimized irregular NoC and 2D Mesh regular NoC for constant bit rate traffic of Figure 4 with (a) XY routing (b) OE routing

Figure 5 shows the comparative results regarding throughput and average flit latency as displayed in Figure 4 of Irregular NoC with up*/down* routing in comparison to 2D-Mesh with XY and OE routing. Irregular NoC with up*/down* routing function shows on average an increase in throughput of 22.3% and reduction in average flit latency of 11.2% and 19% in comparison to 2D-Mesh with XY and OE routing respectively.

The communication optimized Irregular NoC designed according to application requirement showed better performance for constant bit rate traffic patterns in comparison to mapping optimized 2D-Mesh according to application requirement because the irregular topology provides increased flexibility for the topology design in comparison to standard regular topology.

VI. CONCLUSION

This paper evaluates the performance of regular and irregular NoC for constant bit rate traffic pattern for various routing algorithms such as X-Y, O-E, Up*/down*. It is observed that although up*/down* routing may not provide minimal paths in all the case but provides better performance oriented NoC design in comparison to 2D-Mesh according to communication requirement. The results clearly show that the greater flexibility provided in the design of irregular NoC helps it in outperforming it regular NoC counterpart.

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AUTHORS PROFILE

Dr. Naveen Choudhary received his B.E, M.Tech and PhD degree in Computer Science & Engineering. He completed his M.Tech from Indian Institute of Technology, guwahati, India and PhD from Malviya National Institute of technology, Jaipur, India in 2002 and 2011 respectively. Currently he is working as Associate Professor and Head, department of Computer Science and Engineering, College of Technology and Engineering, Maharana Pratap University of Agriculture and Technology, Udaipur, India. His research interest includes Interconnection Networks, Network on Chip, Distributed System and Information Security. He is a life member The Indian Society of Technical Education, Computer Society of India and The Institution of Engineers, India. E-mail: naveenc121@yahoo.com