FPGA Based Hardware Efficient Digital Decimation Filter for ∑-Δ ADC

Subir Kr. Maity, Himadri Sekhar Das

***Abstract—** This paper focuses on the design of a FPGA based off chip digital decimation filter for single bit sigma-delta A/D converter with medium oversampling ratio for the processing of audio signal. A second-order single-stage sigma-delta (∑-Δ) modulator with single bit quantizer with oversampling ratio 96 from FALCON Instrument is used in this work as a reference modulator. To reduce hardware requirement, multiplier less FIR filter architecture used. Total three cascaded comb type filter are used for decimation and filtering purpose. Those filters are designed and simulated with MATLAB Filter Design Toolbox and finally mapped into XILINX SPARTAN-II XC2S50PQ208 series FPGA. The overall ADC gives 14 bit resolution.*

***Index Terms—** Oversampling, quantization, SNR, Sigma-Delta, Decimation, CIC Filter, FPGA.*

I. INTRODUCTION

Nyquist-rate ADC sample the analog input signal at the fs=2fb, where fb is the highest frequency component of the input signal and fs is the sampling frequency. If the input signal is not band limited, an anti-aliasing filter must be used before the converter to prevent aliasing. To ensure that the filtered signal does not contain any frequency components above fs/2, the anti-aliasing filter must have a very narrow transition band, which is not easy to realize. Also the resolutions of Nyquist rate converter are low which is not suitable for a very low voltage signal conversion. Oversampled ADC architecture is preferred over Nyquist ADC due to their high signal to noise ratio and high resolution [1]. So for moderate speed application such as voice communication or digital audio technology oversampled ADC architecture are most preferable compared to Nyquist rate converters [6]. In case of Sigma Delta A/D converter the modulator portion behaves like a noise shaper and digital filter remove the out of band quantization noise thus ensure much higher SNR which is impossible to achieved in Nyquist A/D converter [2 , 4].

II. BASICS OF SIGMA DELTA MODULATOR

In addition to the substantial improvement in the SNR, oversampling possesses inherently the motivation for prediction. Especially the signal does not change significantly in the interval between successive samples when it is oversampled. This can lead a reduction in the number of quantization levels if the difference of two consecutive

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samples is encoded [5]. Since the values of these samples are very close, they are highly correlated and therefore future samples could be predicted from the past one. The simplest predictive modulator is the linear Delta modulator. A further improvement in the SNR can be achieved by pushing most of the in band noise outside signal frequency band [13]. This is attainable if signal transfer function is a low pass whereas and most important Noise transfer function is high pass. This technique is called noise shaping and can be easily and efficiently implemented by modifying the delta modulator [8]. Here the integral of the input signal is encoded rather than the input signal directly. Clearly integration being a linear function does not effect system transfer function. The demodulation integrator at output can be placed at the input of Delta modulator. The significant modification of Delta modulation system is that matching of two integrator is not require any more and this new system is called Sigma Delta Modulator[6]. Block diagram of a 1st order Sigma Delta modulator shown in Fig.1
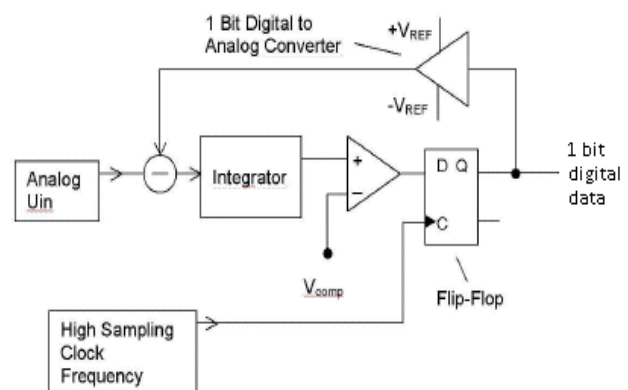

Fig.1 Block diagram of a 1st order Sigma Delta modulator

III. DESIGN OF DIGITAL FILTER

A. Purpose of Filtering

Basic tasks are to be performed in the digital filter sections:

1) Remove shaped Quantization Noise: The ∑-Δ modulator is designed to suppress quantization noise in the baseband. Thus, most of the quantization noise is at frequencies above the baseband. The main objective of the digital filter is to remove this out-of-band quantization noise. This leaves a small amount of baseband quantization noise and the band-limited input signal component. Reducing the baseband quantization noise is equivalent to increasing the effective resolution of the digital output [4].

2) Decimation or sample rate reduction: The output of the ∑-Δ modulator is at a very high sampling rate. This is a fundamental characteristic of ∑-Δ modulators because they use the high frequency portion of the spectrum to place the bulk of the quantization noise. After the high frequency quantization noise is filtered out, it is possible to reduce the sampling rate. It is desirable to bring the sampling rate down to the Nyquist rate which minimizes the amount of information for subsequent transmission, Storage or digital signal processing [4, 7].

B.   Choice of Filter topology

There are a number of factors that make it difficult to implement the digital decimation filter. The input sampling rate of the modulator is very high and the digital decimation filter must perform computationally intensive signal processing algorithms in real time [7]. Thus, the decimation filter must perform very well to remove the excess quantization noise. Applications like high quality audio conversion impose the additional constraint that the digital signal processing must perform its task without distorting the magnitude and phase characteristics of the input signal in the baseband. The goal is to implement the digital filter in minimum amount of logic and make it feasible for monolithic implementation [9].

The simplest and most economical filter to reduce the input sampling rate is a "Comb-Filter", because such a filter does not require a multiplier. A multiplier is not required because the filter coefficients are all unity. This comb-filter operation is equivalent to a rectangular window finite impulse response (FIR) filter. Magnitude response of a Comb filter shown in Fig.2
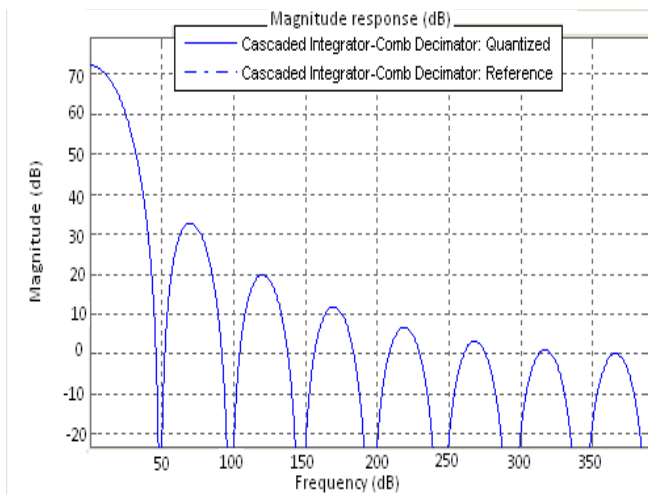
Fig.2 Magnitude response of a Comb filter

However, the comb-filter is not very effective at removing the large volume of out-of-band quantization noise generated by the ∑-Δ modulators and is seldom used in practice without additional digital filters.

Also, the frequency response of the comb-filter can cause substantial magnitude drooping at the upper region of

baseband. For many applications which cannot tolerate this distortion, the comb-filter must be used in conjunction with one or more additional digital filter stages.

C. Design of Cascaded Integrated Comb (CIC) Filter

A comb-filter of length N is a FIR filter with all N coefficients equal to one. The transfer function of a comb-filter is:

$$H(Z) = \sum_{N=0}^{N-1} Z^{-N} = \frac{Y(Z)}{X(Z)} \ldots\ldots\ldots\ldots(1)$$

Or, in the discrete-time domain for N = 4:
$$y(n)=x(n) + x(n-1) + x(n-2) + x(n-3)$$

Clearly the filter is a simple accumulator which performs a moving average. Using the formula for a geometric sum can be expressed in closed form as:

$$H(Z) = \frac{1-Z^{-N}}{1-Z^{-N}} = \frac{Y(Z)}{Z(Z)} \ldots\ldots\ldots\ldots(2)$$

The closed form solution in Eqn. (2) can be factored into two separate processes-integration followed by differentiation as shown in Eqn.3:

$$Y(Z) = \left[\frac{1}{1-Z^{-1}}\right]\left[1-Z^{-N}\right]X(Z)\ldots\ldots\ldots(3)$$

Now, since the comb filter will be followed by an N: 1 decimator, the differentiation function can be done at the lower rate.
• No multipliers are required
• No storage is required for filter coefficients
•Intermediate storage is reduced by integrating at the high sampling rate and differentiating at the low sampling rate, compared to the equivalent   implementation using cascaded uniform FIR filters
• The structure of comb-filters is very "regular "consisting of two basic building blocks
• Little external control or complicated local timing is required
• The same filter design can easily be used for a wide range of rate change factors,   N, with the addition of a scaling circuit and minimal changes to the filter timing.

A single comb-filter stage usually does not have enough stop-band attenuation in the region of interest to prevent aliasing after decimation. However, cascaded comb-filters can be used to give enough stop-band attenuation [9]. Block diagram representation of CIC Filter shown in Fig.3
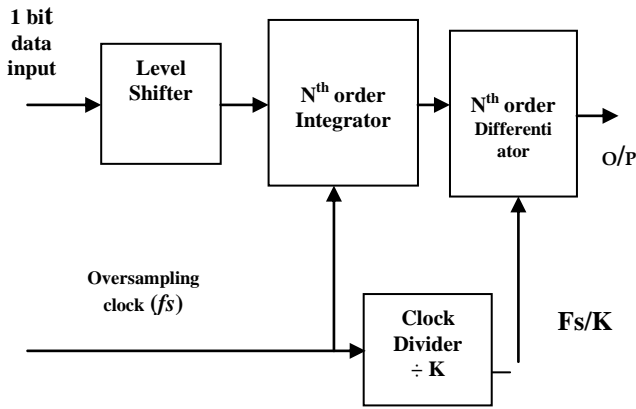
Fig.3 Block diagram of CIC Filter (N= no of section)

D. MATLAB Simulation

To determine filter characteristic and performance one behaviour model of 2nd order Sigma Delta ADC designed and simulated using MATLAB-SIMULINK. Block diagram of behavioural model shown in Fig.4
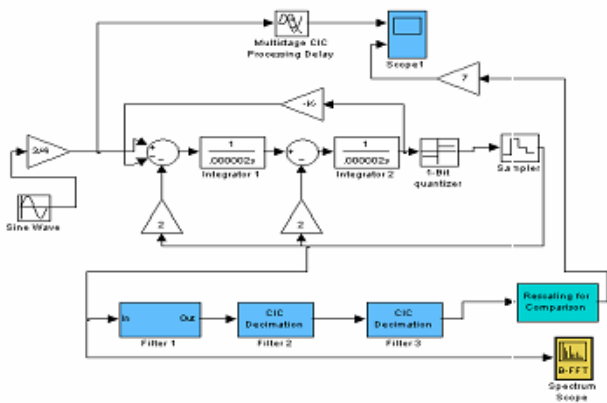
Fig.4 Block diagram of behavioral model

Sampling frequency is 781 KHz. Input sine wave frequency is 3 KHz. Thus Oversampling ratio 96 is chosen for this design. For digital filtering purpose, 3 filter stages are used here. Each stage consists of Cascaded Comb filter with separate decimation factor shown in Table 1.

TABLE 1
DESIGN PARAMETERS FOR DIGITAL FILTER SECTION

Filter Name	Decimation factor	Sampling Frequency(KHz)	No. of stage
Filter 1	16	781	5
Filter 2	3	48	3
Filter 3	2	16	3

2nd order modulator shift the noise component towards high frequency band. Time domain representation of input signal and digitally approximated signal at output shown in Fig.5
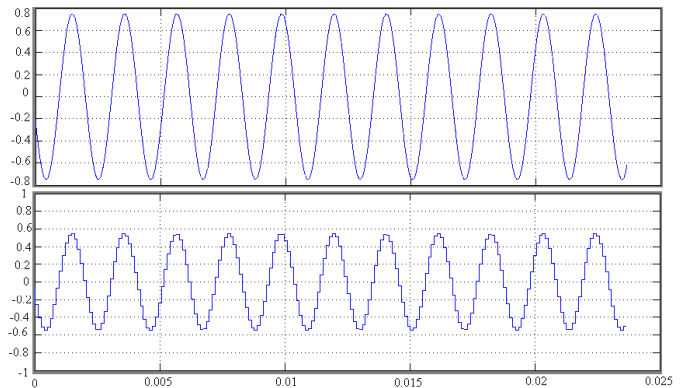
Fig. 5 Time domain representation of input signal and digitally approximated signal at output

Spectrum plot of output bit stream from modulator shown in Fig.6. Here the quantization noise factor shifted towards high frequency band from low frequency signal band. After final stage filtering spectrum of output digital data shown in Fig.7.

Advantages of 3 stage filtering compared to single stage filtering are to suppress quantization noise component more efficiently. For single stage filtering spectrum of output data shown in Fig.8 where noise floor is not so smooth compared to 3 stage filtering shown in Fig.7
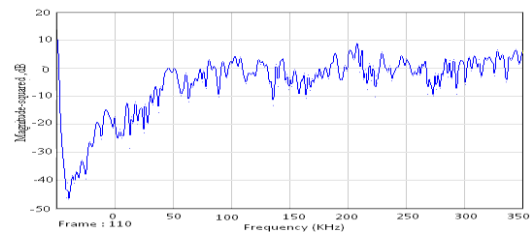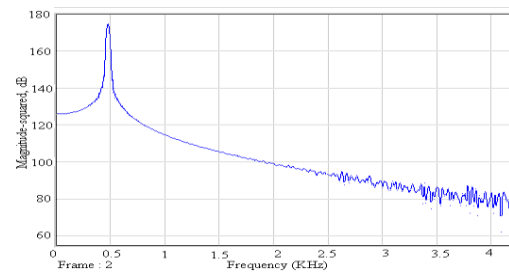
Fig.6 Spectrum plot of output bit stream from modulator

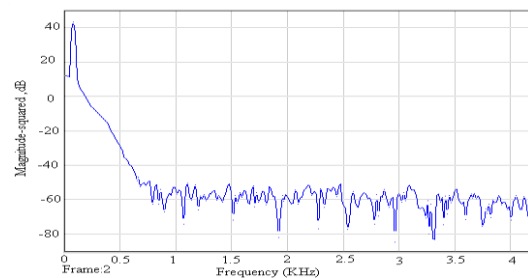**Fig.7 After final stage filtering spectrum of output digital data**

Fig.8 single stage filtering spectrum of output digital data

E. *FPGA* Implementation

After successful simulation in MATLAB those digital filters are implemented into XILINX SPARTAN II FPGA [3, 10]. Using Simulink HDL coder VHDL codes of filters are generated and mapped into FPGA using XILINX ISE V10.1 design tools. Reference sigma delta modulator portion is taken from FALCON digital communication trainer kit [12]. Input and output waveforms of modulator observed using Digital storage oscilloscope shown in Fig.9
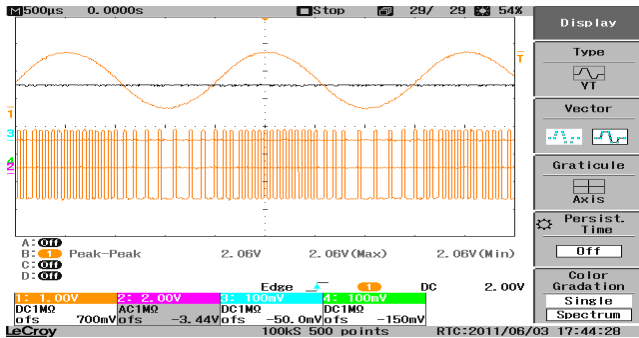

Fig.9: Input and output waveform of Modulator

IV. RESULT

Output of modulator is a single bit data, applied into FPGA board for digital filtering. Output of digital filter which is a multi bit digital data is displayed by using a PC based 34 channels Logic analyzer from HANTECH shown in Fig 10. Also the logic analyzer records the digital value into PC for offline processing [11]. Output of logic analyzer shown in Table 2 and digitally approximated waveform shown in Fig. 11
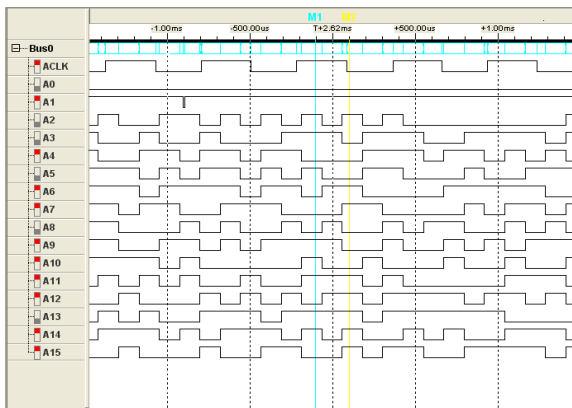
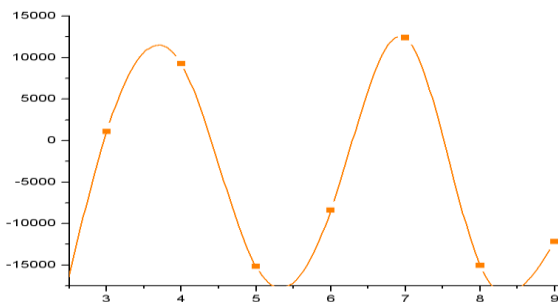

Fig.10 Output of logic analyzer

Fig.11 Digitally approximated waveform

TABLE 2 OUTPUT BINARY DATA AND ITS ANALOG EQUIVALENT VALUE

I/P Para-meter	Sign bit	Binary code	Digital Equivalent	Analog Equivalent (Volt)
Vin= 1 volt (peak), Freq = 3kHz	1	11111010010110	16022	-0.9780
	0	00010000110100	01076	+0.0657
	0	10010000110100	09268	+0.5657
	1	11101101001000	15176	-0.9261
	1	10000011001001	08393	-0.5123
	0	11000001110001	12401	+0.7569
	1	11101011001001	15049	-0.9186
	1	10111101111110	12158	-0.7421

V. CONCLUSION

One digital decimation filter for Sigma Delta ADC is successfully implemented into Xilinx Spartan series FPGA. This ADC gives overall 14 bit resolution. The digital filter uses multiplier less FIR filter architecture to reduce hardware requirement. Due to noise and buffering problems, the discrete output value does not exactly coincide with the sine wave at all points. It is either less or more than the exact sine wave value. This problem can be eliminated by adding a low-pass filtering block at the output of the decimator stage but it also increases hardware requirement.

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