Direct Digital Frequency Synthesizer Design with Modified Parabolic Method Approximation Method

Snigdha Madhab Ghosh, Anindya Sundar Dhar, Sunandan Bhunia

Abstract-The efficiency of the traditional DDFS is greatly depends on the large size of memory. The ROM less architecture for generating sine wave and its necessary corrective measure based on parabola has already been developed. This paper proposes a modified parabola by adding a triangular wave to achieve a sine wave with less distortion. This architecture gives better performance.

Index Terms: Direct Digital Frequency Synthesizer, Parabolic approximation.

I. INTRODUCTION

The concept of DDFS was first projected by J.Tierney in 1971[1]. Direct Digital Frequency Synthesis (DDFS) is an electronic means of generating discrete samples from single or multiple sources for converting them to sine wave of different frequencies with the help of reference frequency. Direct Digital Frequency Synthesis (DDFS) also known as Numerically Controlled Oscillator (NCO), is a technique which uses digital-data and mixed signal processing blocks to generate signal waveforms that are repetitive in nature. A DDFS can provide fast switching[2] and high frequency resolution, over a wide band of frequency. In addition, it provides linear phase and frequency shifting with good spectral purity. With the advent of VLSI technology and the requirement of mobile communication systems, direct digital frequency synthesizers have been widely used in wireless transceivers [3]since the 1980's.

DDFS solutions are implemented in LSI (large-scale integration) and they play an ever-increasing role in digital waveform and clock generation, and modulation. A major advantage of a direct digital synthesizer (DDS) is that its output frequency, phase and amplitude can be precisely and rapidly manipulated under digital processor control [2]. Other inherent DDFS attributes include the ability to tune with extremely fine frequency and phase resolution, and to rapidly "hop" between frequencies.

It is easy to include different modulation capabilities in the DDFS by using digital signal processing methods, because the signal is in digital form. By programming the DDFS, adaptive channel bandwidths, modulation formats, frequency hopping and data rates are easily achieved. The implementation of digital functional blocks makes it possible to achieve a high degree of system integration. The DDFS addresses a variety of applications, including cable modems, measurement equipments, and arbitrary waveform

The demand for DDFS in modern communication is increasing by leaps and bound, because of its obvious advantages over VCO-PLL synthesizer in terms of fast frequency switching[2][4], better resolution, low noise, and transient free frequency changes.

A trade-off is drawn upon the various characteristic of DDFS on a particular application. For example accuracy and resolution for instrumentation whereas logistics is important for cellular mobile communication. The frequency generation is generally 1/3 of the reference frequency [2].

A standard DDFS architecture consists of a phase accumulator, a ROM /lookup table, a DAC and some reconstruction filters

There are different methods of sine/cosine wave generation have reported with different merit and their limitations. These are with memory, reduced memory and memory less architecture. Few are DDFS with Look-Up-Table (LUT), DDFS with sine and cosine function, interpolation based and parabola based Taylor Series Based DDFS [4].

Direct Digital Frequency Synthesizer with Look-Up-Table is the method in which phase value of sine wave is stored in a Erasable Programmable Read Only Memory (EPROM) and phase angle is called for to form sine wave. The address to the LUT is generated through a phase accumulator.

The resolution of the DDFS depends on the memory size, if the memory locations are more, the frequency resolution is more. The phase accumulator size is greatly depends on the memory. The phase accumulator works on the principle of arithmetic over flow. The value of the phase accumulator keeps on increasing in steps in each cycle of the reference clock till the accumulator overflows and repeat the same sequence.

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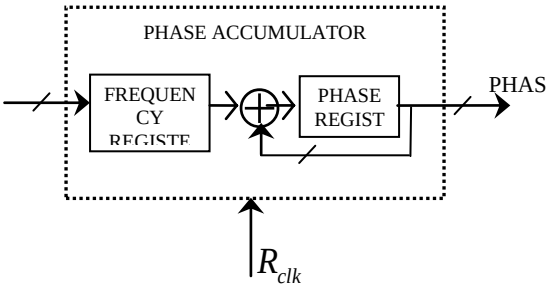

Fig-1 Diagram of Phase accumulator

The phase accumulator size is greater than the address bits of memory locations and accumulator bits are truncated. If M is the tuning ratio, then

The output frequency $f_{out} = \frac{M * f_{clk}}{2^n}$

and resolution $\frac{f_{clk}}{2^n}$

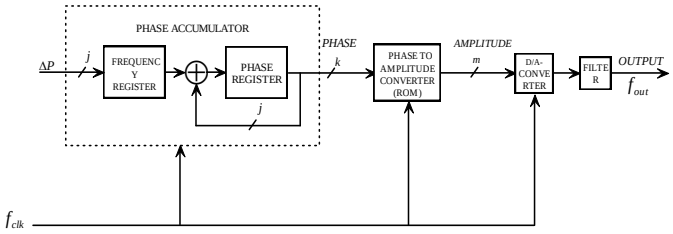

Fig-2. The block diagram of DDFS

compatible for loading in the EPROM. The first stage of hardware implementation is phase accumulator. The diagram of phase accumulator is shown in Fig-1

II. PARABOLIC APPROXIMATION OF SINEWAVE

The parabolic wave is very close resembles of sine wave. In parabolic approximation method[5], the quadratic polynomial $–ax^2 + bx + c$ is considered to approximate a parabola . The x-axis or time axis is segmented in to $2^N–1$ segments[6], and the required address from phase accumulator is any value between 0 to $2^N–1$. For simplicity of arithmetic and scaling, a=1 , b= 2^N—1 and c =0 are taken. The number of segments of x-axis or time axis is of 2^N—1and generally N is taken 12 or 8 as the 12bit or 8bit DAC is readily available in the market. The final equation becomes $n(n – 2^N -- 1)$ or $–n(2^N—1 –n)$, where n corresponds to integers from 0 to $2^N–1$. So the parabola has zero values at 0 and 2^n-1. The vertex or the peak amplitude of the parabola is given by –D/4a. Where $D= b^2 - 4ac$.

So, in our experiment, we have considered N=10 so the maximum number of samples of parabola will be 1024. The polynomial n(1023—n) is taken for simplification as the parabola would form on the first quadrant of two dimensional Cartesian coordinate system. The abscissa can have 0 to 1023 integer and convenient for 10-bit addressing, it is also compatible with available DACs.

If we take n = 8 or 12, then the compatibility with DAC becomes easier. The equation $n(2^N—1 –n)$ indicates two factors viz n and $[(2^N—1) –n]$, the second factor is the 2's complement of n [6] and multiplied with n gives parabolic polynomial. The necessary scaling is an important factor.

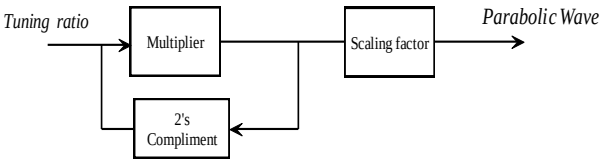

Fig-3. Block diagram of parabolic approximation of sine wave

To increase the number of samples or phase values, the 8-bit address lines from phase accumulator may increase to 10-bits, to increase the number of samples. The address lines may be increase from 8-bit to 10bit to increase samples from 256 to 1024 for every half cycle. The half sine wave, thus generated by parabolic approximation is shown Fig-4.

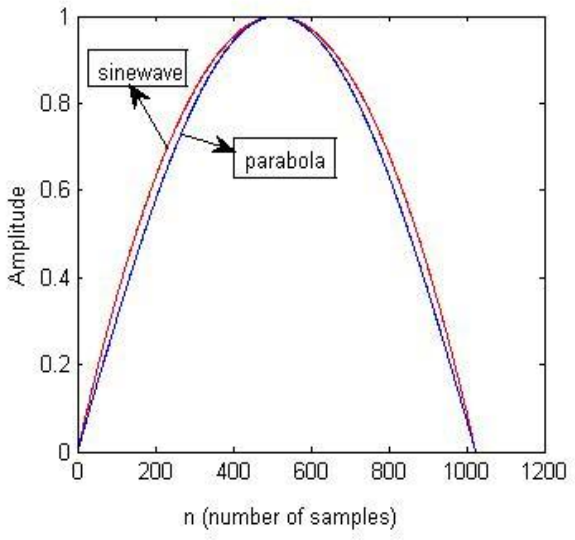

Fig-4. Plot of half sine wave and parabola

However this parabola differ from pure half sine wave. The subtraction of parabola from half sine wave gives the difference between the parabola and the half sine wave. A thorough investigation of Fig-4, reveals a vertical symmetry, that the error is more in the middle of the quarter wave and less at the top and bottom of the quarter curve. The error curve is given in Fig-5.

The error signal is given by equation (1).

$$\text{Error} = [n(2^N - n)] \div 262144 - \text{Sin}\frac{2\Pi n}{T} \quad for\ 0 \le n \le 2^N \qquad \text{-eq(1)}$$

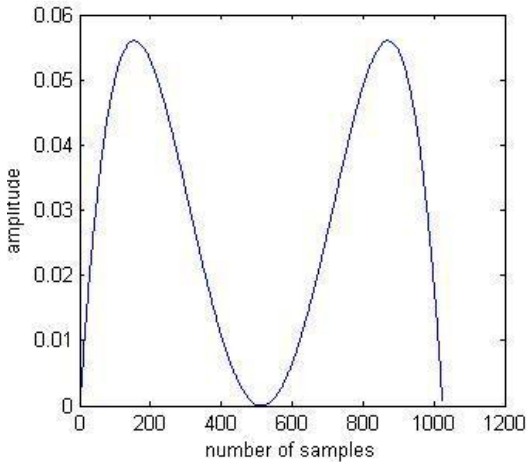

Fig-5. Error between half sine wave and parabola

III. MODIFICATION OF PARABOLA AND ARCHITECTURE

The observation of error curve as shown in Fig-5, indicates that the error curve is a multiple curves similar to parabola with asymmetric in nature and the sample values of parabola are greater than the sine wave and non-uniform in nature, through a quarter cycle. The error curve is linearly approximated and found a curve similar to triangular wave with different slopes as shown in Fig-6. It is observed that first and fourth line have same slope in magnitude where as second and third have different slopes in magnitude.

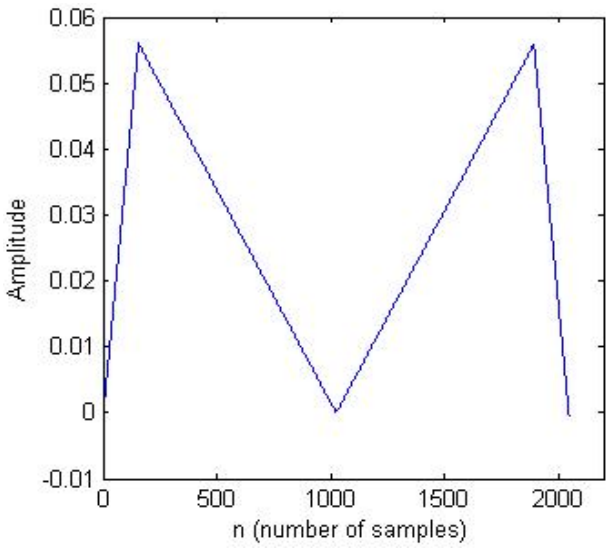

Fig-6 Error signal is approximated to double triangular wave

It requires a further modification of curve in Fig-6 to a double triangular wave with a slope of 0.056/256 for each n/4 segments, where n-bits are taken for forming parabola. For the simplicity of arithmetic of addressing , the curve in fig-6 further modified to a double triangular wave with a slope of 0.112/256 for each n/4 segments, where n-bits are taken for forming parabola.

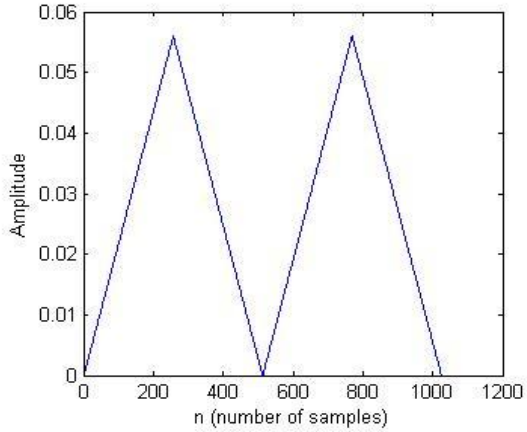

Fig-7. Modified double triangular wave

This particular curve indicates that the values of n from 0 to 255, 255to 512, 512 to 768 and 768 to 1023 have been defined for the function of $\frac{112}{256000}x$, $\frac{112(513-x)}{256000}$, $\frac{112(x-513)}{256000}$ $\frac{112(1023-x)}{256000}$ respectively with a slope of 0.112/256.

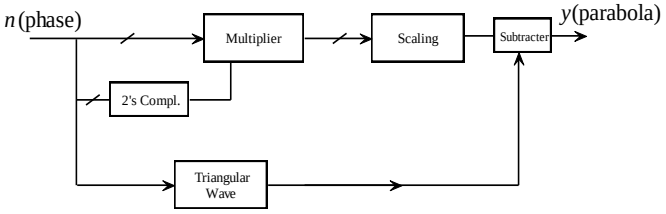

Fig-8. Block diagram of parabolic approximation after due modification

IV. EXPERIMENTAL RESULT

The Xilinx block sets and Matlab mathwork are used to implement the above parabola generation scheme and to evaluate various parameter variations and their effect on parabola. The circuit also implemented in the Spartan kit and verified the out put. Now it is observed that the error before modification, the peak magnitude was 0.056 and after error

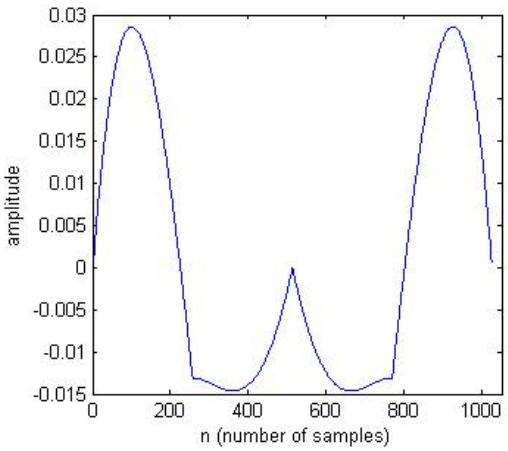

Fig-9, Final error curve

correction the peak error magnitude is 0.0286.. It is further observed that keeping the frequency control word at 01 and changing N from 8 to 16 in steps of one's, does not affect the error. The error remains fixed at a maximum magnitude of 0.0286. Further modification can be done but the circuit would be complex. The final error curve is shown in Fig-9

It is also observed that the error curve swings between the +0.0286 to -0.0056, so the mean error is around 0.0115.

The sine wave so formed with the help of modified parabola is compared with the pure sine wave and sine wave formed with the help of pure parabola is shown in the Fig-10. The pure parabola, modified parabola and pure sine wave are indicated as red, blue and green respectively.

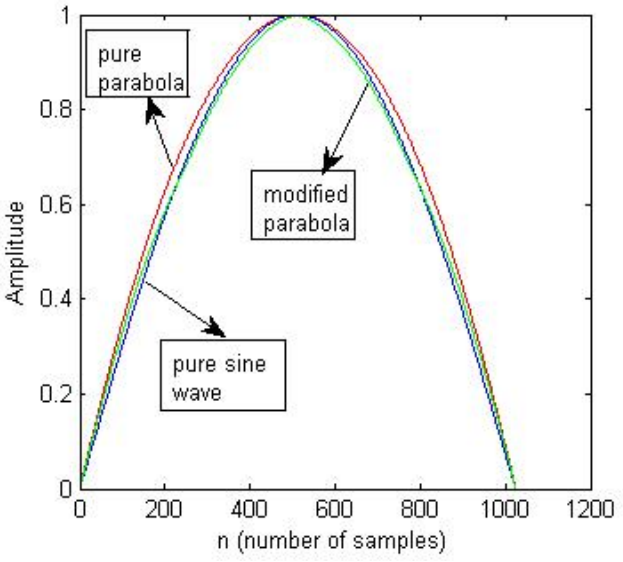

Fig-10. Pure and modified parabola with pure sine wave

The power spectrum is also checked and FFT of the sine wave by the modified parabola, is shown in Fig-11, which is almost same as a pure sine wave.

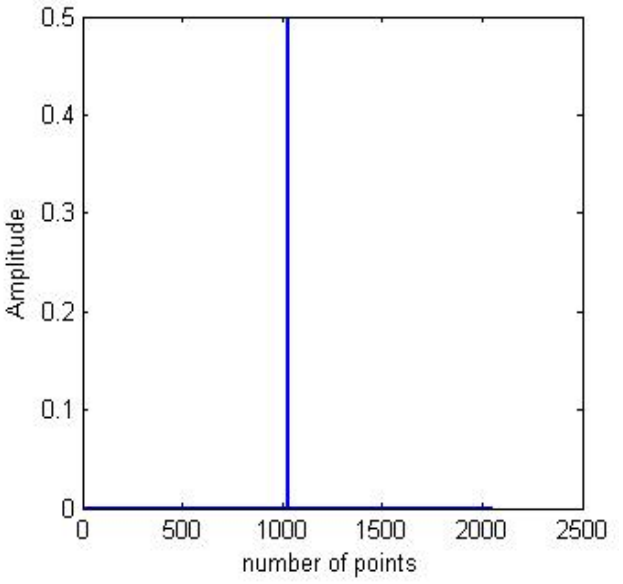

Fig- 11.FFT of sine wave by modified parabola

Further the SDFR performance of the sine wave with the help of modified is 102 dBc

V. CONCLUSION

Every system or process suffers some accuracy, but the systems have their relative advantages in terms of accuracy, speed, logistics and every system has its own applications. The main objective of this design is to remove the look-up-table and to reduce the hardware complexity with reasonable accuracy in terms of dBc.

It is evident from the following table that the objective of the design is met.

Table-1 Comparison of performance

Chip	Type	SFDR
Ours	Parabolic	102 dBc
Ref. [9]	Quadrature	75 dBc
Ref. [10]	Quadrature Cosine only	75 dBc 75 dBc

REFERENCES

1. A Digital Frequency Synthesizer- J.Tierney, C.M.Radre, and B.Gold IEEE Transactions on Audio and Electroacoustics, March 1971
2. Avanindra Madisetti, Alan Y kwentus, Alan N Willson "A 100-MHz, 16-b, Direct Digital Frequency Synthesizer with a !00-dBc Spurious-Free Dynamic Range".IEEE Journal of solid-state circuits, vol 34, 8 August 1999,pp1034-1043.
3. D. Soudris, M. Kesoulis, C. Koukourlis, A. Thanailakis, and S. Blionas"Alternative Direct Digital Frequency Synthesizer Architectures with Reduced Memory Size"
4. K.I Palomaki and J Niittylahti, "A Low-Power, Memoryless direct Digital Frequency Synthesizer Architecture" P.O. Box 553,FIN-33101,Tampere Finland.
5. David J. Betowski, Daniel Dwyer and Valeriu Beiu "A Novel Segmented Parabolic Sine Approximation for Direct Digital Frequency Synthesizers"
6. Amir M. Sodagar and G. Roientan Lahiji "A Pipelined ROM-Less Architecture for Sine-Output Direct Digital Frequency Synthesizers Using the Second-Order Parabolic Approximation"IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol48 No 9, September 2001.
7. H T Nicholas and H Samueli, "A 150 MHz direct digital frequency synthesizer in 1.25- μm CMOS with – 90 dBc spurious performance," IEEE j. Solid –State Circuits vol. 26, pp.1959-1969, Dec.1991.
8. Harris HSP45106 datasheet, Jan 1999.
9. Stanford Telecommunications 1178A datasheet, Mar. 1994.
10. "Qualcomm 2368," Synthesizer Data Book, 80-24127-1A, Aug. 1997.

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Dr. Sunandan Bhunia obtained his B.Tech, M.Tech from institute of Radiophysics and Electronics, Calcutta University in 1999 and 2002 respectively. He obtained PhD degree in engineering from Jadavpur University in 2009. He was awarded gold medal from Vidyasagar University for 1st class 1st in Physics (H) in 1999. He is currently working as Associate professor and Head, Department of Electronics and Communication Engineering, Haldia Institute of Technology, Haldia, under WBUT. He has published about 18 research articles in reputed international & national journal and conferences. His area of research interest includes, Microstrip Antenna, Microstrip Filter, and Frequency Selective Surfaces, VLSI etc. He is the member of Chief Technical Advisory Board of International Journal of Soft Computing and Engineering (IJSCE) and member of editorial board of International Journal of Computer Technology and Electronics Engineering (IJCTEE).