Comparative Study for Delay & Power Dissipation of CMOS Inverter in UDSM Range

Jagannath Samanta, Bishnu Prasad De, Banibrata Bag, Raj Kumar Maity

Abstract— Delay and power are two major issues in design and synthesis of VLSI circuits which depends on different design parameters. In this paper, the relative study of propagation delay and power consumption of UDSM CMOS inverter is found considering the channel length below 100nm. The simulation results are taken for different technology (32nm, 45nm, 65nm and 90nm) with the help of Tanner (T-spice) simulation tool. The values of model parameters are used from current Berkeley Predictive Technology Model (PTM). Also the results are analyzed by varying load capacitance, supply voltage & transistor widths.

Index Terms— UDSM, T-Spice, BPTM, Delay, Power dissipation, PDP, CMOS Inverter.

I. INTRODUCTION:

MOSFETs are continuously scaled to smaller dimensions to reduce the space complexity. UDSM (Ultra Deep Sub-Micron) Technology deals with MOS devices with channel length in the order of 0.25µm to 0.022µm or even less. The integration of nanostructures at room temperature smaller than 10nm is far too sensitive to size variations of even a few atomic widths [1]. Propagation delay and power dissipation are two major roles for design & synthesis of any VLSI circuits in this range. There are different secondary effects like Body Bias effect, Channel Length Modulation Effect (CLM), Velocity Saturation effect, Drain Induced Barrier Lowering (DIBL), etc which will modify the delay and power models.

There are lots of researches on delay model for CMOS inverter is given in [2,4-6,11,18]. The most popular delay model is descried in nth power law [12] where velocity saturation is main consideration. A closed form expression to accurately estimate the delay of a CMOS deep submicron (DSM) inverter is presented in [14] where a large interconnect RLC load is driven. Accurate drain current and propagation delay modeling for DSM CMOS circuits is essential in the design and analysis of high performance digital integrated circuits in [16]. The expression for power dissipation of CMOS inverter is presented in [2,4-6,11,18].

But all the above models are only valid upto DSM range. In this paper, the simulation of a CMOS Inverter is done considering the channel length in the order of 32nm, 45nm, 65nm and 90nm. The results show that how these two major factors will depends on different design parameters for different channel length. It is also observed the Power Delay Product (PDP) and threshold voltage of CMOS Inverter circuit. It can be easily analyzed the characteristic of the UDSM CMOS Inverter and their application in the field of VLSI.

The rest of paper is organized as follows. The section-II & section-III presents the brief description of the delay and power modeling of CMOS Inverter. Simulation results & Discussions are given in section-IV. Summery & Conclusion are presented in section-V.

II. DELAY MODELING OF CMOS INVERTER

Based on nth power law [12], delay model of CMOS **inverter** includes for both very fast input as well as very slow input signal. The critical input transition time t_{T0}

$$t_{T0} = \frac{C_0 V_{DD}}{2 I_{D0}} \frac{(n+1)(1-v_T)^n}{(1-v_T)^{n+1} - (v_V - v_T)^{n+1}}$$

Where $v_T = V_{T0} / V_{DD}$ and $v_V = V_{INV}/V_{DD}$. Then the delay t_d, the delay from $0.5V_{DD}$ of input to $0.5V_{DD}$ of output, and the effective output transition time t_{TOUT} can be expressed as follows. t_{TOUT} can be used as t_T for the next logic gate;

($t_T \le t_{T0}$: for the faster input)

$$t_d = t_T \left\{ \frac{1}{2} - \frac{1-v_T}{n+1} + \frac{(v_V - v_T)^{n+1}}{(n+1)(1-v_T)^n} \right\} + \frac{1}{2} \frac{C_0 V_{DD}}{I_{D0}} t_T$$

$$t_{OUT} = \left\{ \frac{C_0 V_{DD}}{0.7 I_{D0}} \frac{4 v_{D0}{}^2}{(4 v_{D0} - 1)} \right\}$$

($> t_{T0}$: for the slower input)

$$t_d = t_T \left[v_T - \frac{1}{2} + \left\{ (v_V - v_T)^{n+1} + \frac{(n+1)(1-v_T)^n}{2 t_T I_{D0} / C_0 V_{DD}} \right\}^{\frac{1}{n+1}} \right]$$

$$t_{OUT} = \left\{ \frac{C_0 V_{DD}}{0.7 I_{D0}} \left(\frac{1-v_T}{t_d / t_T + 1/2 - v_T} \right)^n \right\}$$

Where C_0 is an output capacitance, $v_{D0}=V_{D0}/V_{DD}$ and n=velocity saturation index.

III. POWER MODELING OF CMOS INVERTER

Three types of power dissipation occur in CMOS inverter circuits, which are given below:

A. Leakage power Dissipation: In OFF-state, the main components of leakage currents are sub-threshold leakage (I_{sub}), gate induced drain leakage (I_{GIDL}), gate tunneling leakage (I_{GATE}) and band-to-band tunneling (I_{BTBT}).

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B. Short-circuit Power: From the α-power law[1] the short circuit power dissipation model is

$$P_{Sht\_ckt\_pw} = V_{DD} t_T I_{DO} \frac{1}{\alpha+1} \frac{1}{2^{\alpha-1}} \frac{(1-2v_T)^{\alpha+1}}{(1-v_T)^{\alpha}}$$

$$Where \quad v_T = \frac{V_{TH}}{V_{DD}}$$

C. DYNAMIC POWER OR SWITCHING POWER:

This type of power dissipation occurs due to the charging and discharging of load and parasitic capacitors.

$$P_{dynamic} = \alpha \cdot C_L \cdot V_{DD}^2 \cdot f + \sum_{i=1}^{n} \alpha_i \cdot C_i \cdot V_{DD} \cdot (V_{DD} - V_T)$$

Dynamic power expression indicate that the average dynamic power of a complex gate due to the output load capacitance. Where, C_L=Load Capacitance, V_{dd}=Supply Voltage, f=Operating Clock Frequency and α → switching activity of gate (the probability of a 0-1 switch in a cycle.

IV. SIMULATION RESULTS & DISCUSSIONS

All simulations are done in TANNER EDA Tool using the PTM technology of level 54 [8] for 32nm, 45nm, 65nm and 90nm. Model parameters are extracted from BSIM4.6.1 user manual [9 & 10].

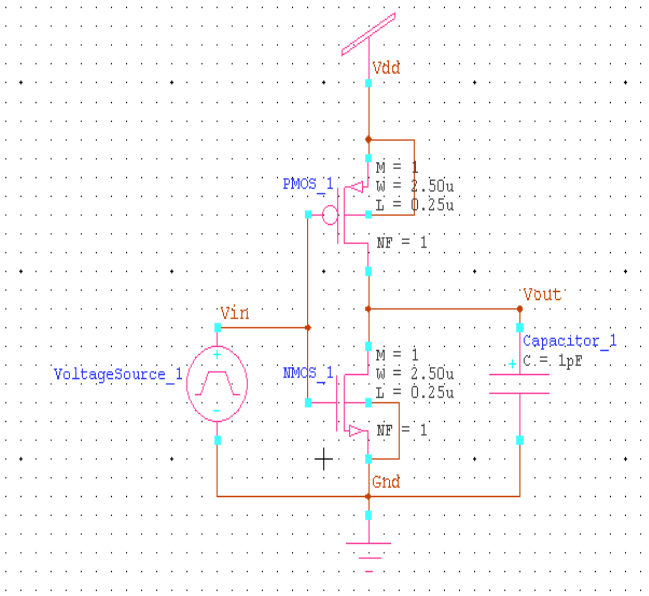

Fig-1: Schematic diagram of CMOS Inverter

The fig-1 shows the snapshot of CMOS inverter which is taken from EDA Tanner simulation tool.

The results clearly show how power dissipation and delay relate to the different design parameters like supply voltage, load capacitance, width of PMOS & NMOS transistor. In all the cases the pulse type {PULSE (0V 1V 0NS 10NS 10NS 100NS 250NS)} input signal is used with rise time (tr=10ns), fall time (tf=10ns) and initial delay time (td=0ns), pulse width (tpw=100ns) and time period (tper=250ns). We compare our results in 32nm, 45nm, 65nm and 90nm for a UDSM CMOS Inverter. The threshold voltage of CMOS inverter is varying with supply voltage and Transconductance ratio.

Since the output waveform expression for each of the regions of operation is known, propagation delay can be calculated as the time from the 50% of the rising /falling input to 50% of the falling/rising of the output waveform.

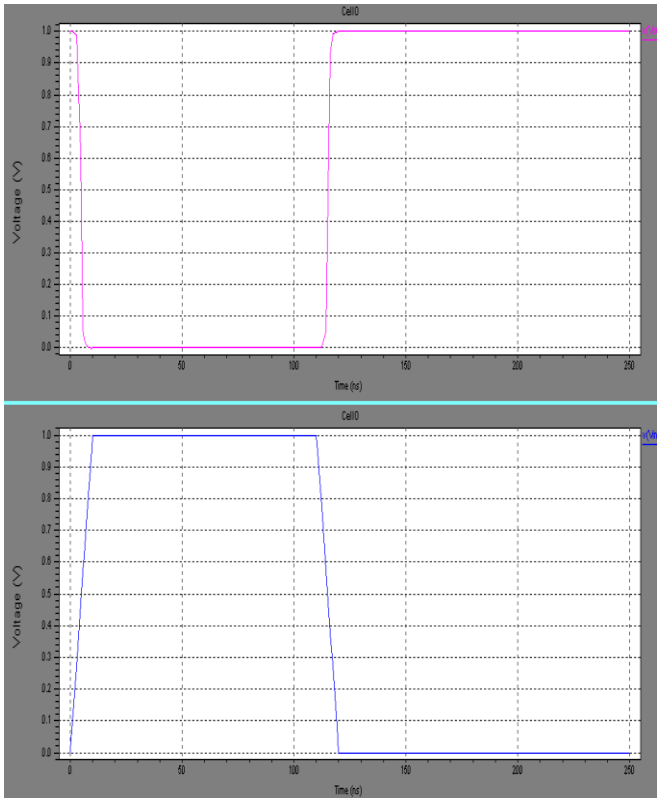

Fig-2: Transient Characteristics of CMOS Inverter

Transient response of CMOS inverter is showing in Fig-2 i.e. input and output waveform w.r.t time in ns.

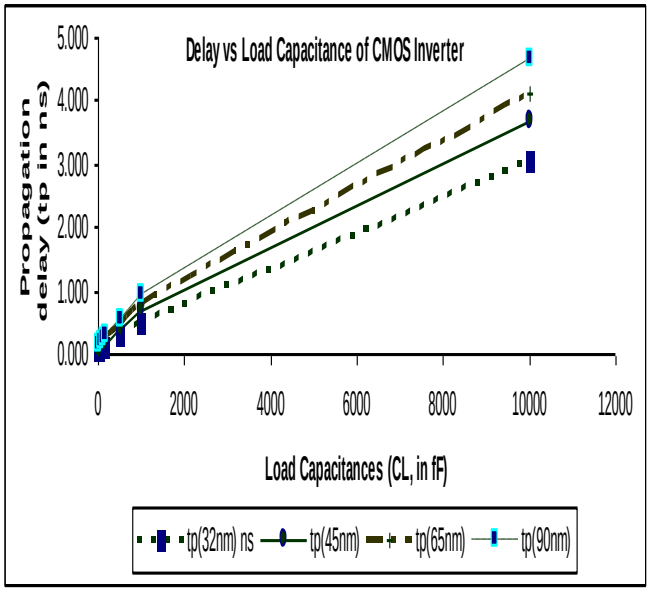

Fig-3: Propagation Delay time (tp in ns) vs. Load capacitance (CL in fF) when Vdd=1V, Wp=5um, Wn=2.5um.

By increasing the load capacitance (CL) of CMOS inverter the Propagation delay time is linearly increased. Fig-3 shows that lowest delay occurs in 32nm technology where as highest delay occurs in 90nm technology.

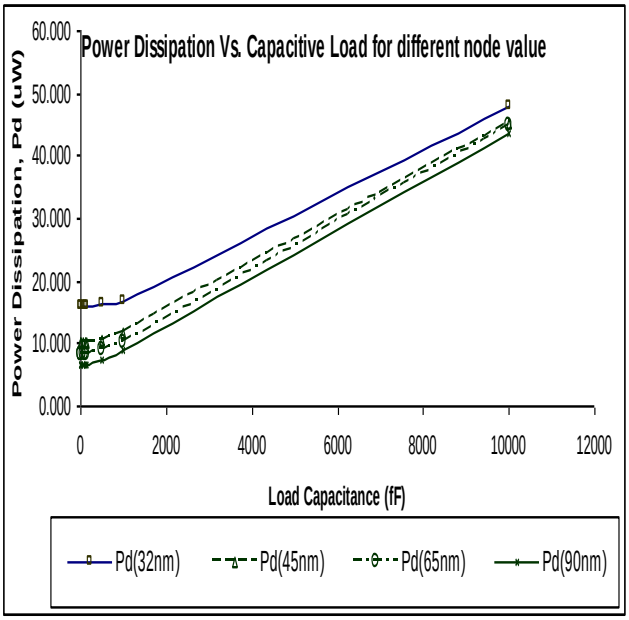

Fig-4: Power Dissipation (Pd in uW) vs. Load capacitance (CL in fF) when Vdd=1V, Wp=5um, Wn=2.5um.

By increasing the load capacitance (CL) of CMOS inverter the power dissipation is linearly increased. Fig-4 shows that lowest power dissipation occurs in 90nm where as highest occur in 32nm.

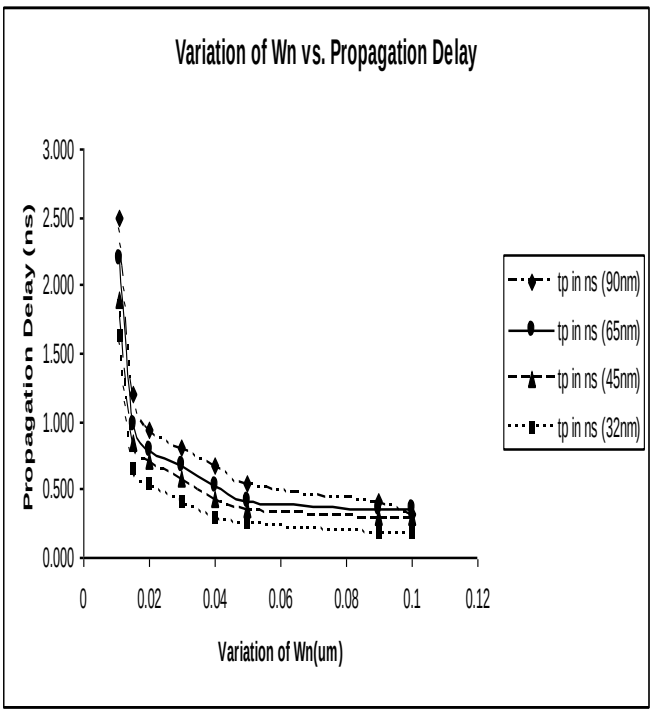

Fig-5: Propagation Delay time (tp in ns) vs. Variation of Wn (um) when Vdd=1V, CL=10fF

Fig-5 shows that the propagation delay is changing with variation of width of NMOS for 32nm, 45nm, 65nm & 90nm.

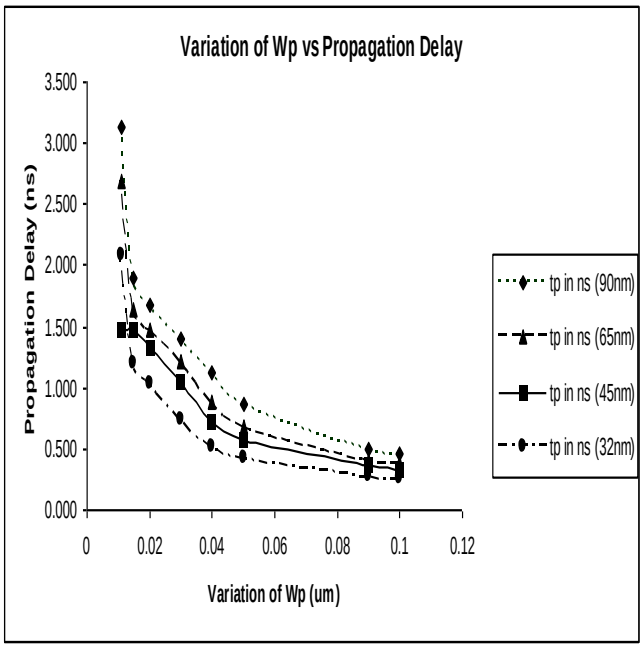

Fig-6: Propagation Delay time (tp in ns) vs. Variation of Wp (um) when Vdd=1V, CL=10fF

Fig-6 shows that the propagation delay is changing with variation of width of PMOS for 32nm, 45nm, 65nm & 90nm.

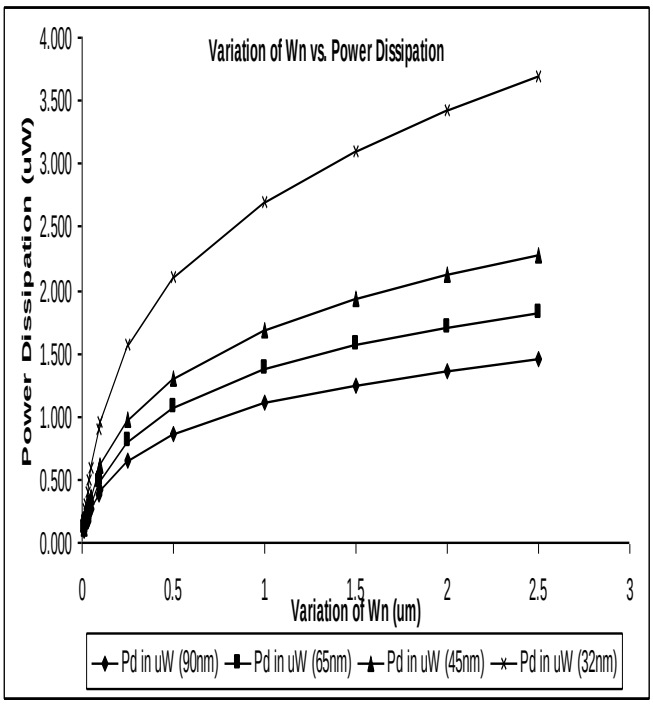

Fig-7: Power Dissipation (Pd in uW) vs. Variation of Wn (um) when Vdd=1V, CL=10fF

Fig-7 shows that the power dissipation is changing with variation of width of NMOS for 32nm, 45nm, 65nm & 90nm.

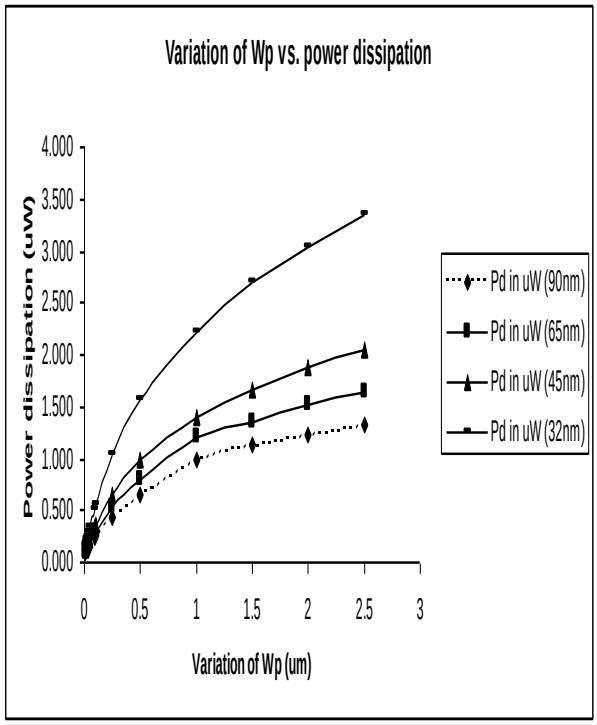

Fig-8: Power Dissipation (Pd in uW) vs. Variation of Wp (um) when Vdd=1V, CL=10Ff

Fig-8 shows that the power dissipation is changing with variation of width of PMOS for 32nm, 45nm, 65nm & 90nm.

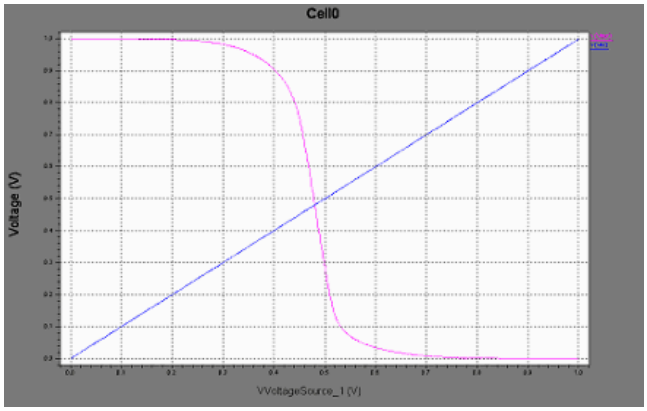

Fig-9: DC Characteristics of CMOS Inverter

Fig-9 shows the DC or transfer characteristic of UDSM CMOS inverter. From this graph we measure the threshold voltage (Vth) (Cross section of the two graphs).

The table-1 shows that variation of supply voltage Vdd how delay and power dissipation will change for different technology. Power dissipation (Pd) will decrease by decreasing supply voltage (i.e. Pd is proportional to the square of the Vdd). In case of propagation delay (tp) is inversely proportional to the supply voltage. From this table we also calculate the Power Delay Product ((PDP=average power consumed * propagation time delay), in fJ ($10^{\wedge -15}$)).

Table-1: Delay, power dissipation and PDP relate with supply voltage (CL=10fF, Wp=0.5um, Wn=0.25um)

Vdd (V)	32nm			45nm			65nm			90nm		
	PD (uW)	tp (ns)	PDP (fJ)	PD (uW)	tp (ns)	PDP (fJ)	PD (uW)	tp (ns)	PDP (fJ)	PD (uW)	tp (ns)	PDP (fJ)
0.5	0.02	116.07	2.68	0.02	4.60	0.10	0.02	4.55	0.10	0.02	4.45	0.09
1	1.56	0.13	0.21	0.98	0.19	0.19	0.81	0.26	0.21	0.66	0.31	0.20
1.5	119.85	0.11	13.63	8.66	0.13	1.14	6.16	0.19	1.15	4.62	0.21	0.96
2	183.19	0.08	14.19	44.90	0.07	2.97	22.19	0.25	5.53	14.62	0.33	4.90
2.5	930.46	0.03	25.82	436.40	0.01	6.02	176.54	0.14	25.50	77.43	0.04	2.89

Table-2: Threshold voltage of CMOS Inverter varying with supply voltage for different technology. (CL=10fF, Wp=5um, Wn=2.5um)

Vdd (V)	vth (mV) (32nm)	vth (mV) (45nm)	vth (mV) (65nm)	vth (mV) (90nm)
1	482.07	478.48	483.86	480.28
1.5	712.36	706.97	720.41	712.34
2	964.14	960.55	971.31	960.55
2.5	1220	1220	1400	1200

Inverter threshold voltage will dependent on supply voltage. The table-2 shows the variation of threshold voltage with supply voltage for different technology. We assuming the value of CL=10fF, Wp=5um, Wn=2.5um.

Table-3: Threshold voltage of CMOS Inverter varying with load capacitance for different technology. (Vdd=1V, Wp=5um, Wn=2.5um)

CL(fF)	vth (mV) 32nm	vth (mV) 45nm	vth (mV) 65nm	vth (mV) 90nm
10	482.07	478.48	483.86	480.28
100	482.07	478.48	483.86	480.28
500	482.07	478.48	483.86	480.28
1000	482.07	478.48	483.86	480.28
10000	482.07	478.48	483.86	480.28

From the above table-3, it is clearly seen that the threshold voltage is independent to the Load Capacitance.

Trans-conductance ratio (Kr=Kn/Kp≈2*Wn/Wp) and corresponding Wn, Wp values are given in the table-4, shows how threshold voltage depends on Kr value.

Table-4: Threshold voltage of CMOS Inverter varying with transconductance ratio for different technology. (Vdd=1V, CL=10fF)

Kr(Wn/Wp)	vth (mV) (32nm)	vth (mV) (45nm)	vth (mV) (65nm)	vth (mV) (90nm)
4 (Wp=5u, Wn=10u)	419.31	415.72	410.34	404.97
2 (Wp=5u, Wn=5u)	451.59	446.21	446.21	442.62
1 (Wp=5u, Wn=2.5u)	482.07	478.48	483.86	480.28
0.5 (Wp=10u, Wn=2.5u)	516.14	415.14	525.1	451.52
0.25 (Wp=20u Wn=2.5u	548.41	451.64	559.17	564.55

V. SUMMARY & CONCLUSION

In this paper, basically compare the results of delay and power dissipation of CMOS inverter in UDSM range and also how these are related with different design parameters. From the simulation it has been seen that when channel length less than or equal to 10nm then output waveform are not appeared due to in this range size of the channel length below atomic width. This is the limitation of Nano range [1]. Threshold voltage and Power Delay Product (PDP) are shown in the table form. This work will help to proper characterize and analyze of the CMOS inverter in the Nano range.

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