Design of Digital Logic Circuits using Carbon Nanotube Field Effect Transistors

Subhajit Das, Sandip Bhattacharya, Debaprasad Das

Abstract*—The work in this paper designs the basic logic circuits using the carbon nanotube field effect transistor (CNTFET). CNTFET is a novel device that is projected to outperform scaled CMOS technologies. CNTFET-based devices offer high mobility for near-ballistic transport, high carrier velocity for fast switching, as well as better electrostatic control due to the quasi one-dimensional structure of carbon nanotubes. CNTFET utilizes a semiconducting carbon nanotube (CNT) channel controlled by isolated electrostatic gates. It demonstrates p-type or n-type switching behavior depending upon the polarity-gate voltage. In this paper ambipolar CNTFETs are used to design basic logic circuits. The datapath logic blocks like half and full-adders are designed and their performances have been investigated.

***Index Terms*— Carbon nanotube (CNT), CNT field-effect transistor (CNTFET), Transmission gate (TG), Verilog-AMS.**

I. INTRODUCTION

Silicon-based integrated circuit technology is approaching its physical limit as the device dimensions scale to the nanometer regime [1]. In the post silicon era, carbon nanotube field effect transistor (CNTFET) is a promising candidate for future integrated circuits because of its excellent properties like near ballistic transport [2], high carrier mobility (10^3–10^4 $cm^2/V{\cdot}s$) in semiconducting carbon nanotube (CNTs) [3, 4], and easy integration of high-k dielectric material resulting in better gate electrostatics. CNTs are basically hollow cylinders of rolled-up graphene sheet composed of one or more concentric layers of carbon atoms in a honeycomb lattice arrangement. Depending on the direction in which the nanotubes are rolled (chirality), they can be either metallic or semiconducting [5]. In a nanotube, low bias transport can be nearly ballistic across distances of several hundred nanometer and it is attractive for nanoelectronic applications due to its excellent electrical properties. The carbon nanotube field-effect transistor thus already achieved widespread attention as possible alternative to nanoscale MOS transistor. Due to the similar *I-V* characteristics of CNTFET as that of MOS devices, qualitatively most of the CMOS circuit can be implemented using CNTFET [11-13].

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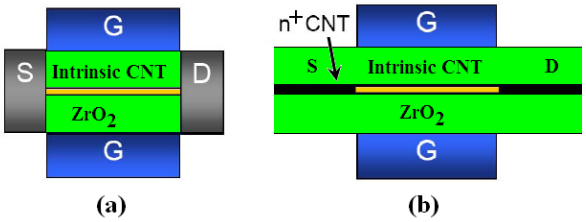


Fig. 1. Different types of CNTFETs: (a) Schottky barrier (SB) CNTFET (b) MOSFET-like CNTFET.

In this work we developed the compact SPICE compatible model for CNTFET using Verilog-AMS language [14]. The SPICE compatible circuit model of double gate (DG) Schottky barrier (SB) CNTFET with an ambipolar behavior (n/p-type depending on the polarity-gate voltage) [6, 7] is implemented in Verilog-AMS for the circuit simulation of basic logic gates. In the proposed circuits, the logic levels are represented in terms of voltage value considering sufficient noise margin to avoid any error in computation. Both static logic and transmission gate (TG) based designs are implemented and the performances are evaluated. The simulation results show excellent performance on power and speed of operation.

The remainder of the paper is organized as follows. Section II describes the fundamentals of ambipolar CNTFETs with special emphasis on circuit compatible model that we have used for our simulation. Section III describes the I-V characteristics of CNTFET devices. The logic gate implementations using ambipolar CNTFETs and the simulation results are discussed in Section IV. Finally, conclusions are provided in Section V.

II. MODEL FOR CNTFET

CNTs are used in the channel region of the CNTFET. Different types of CNTFET have been demonstrated in the literature. There are mainly two types of CNTFET: Schottky barrier CNTFET (SB-CNTFET) and MOSFET-like CNTFET as shown Fig. 1.

In SB-CNTFET the channel is made of intrinsic semiconducting CNT and direct contacts of the metal with the semiconducting nanotubes are made for source and drain regions. The device works on the principle of direct tunneling through the Schottky barrier (SB) at the source-channel junction. The barrier-width is modulated by the application of gate voltage, and thus, the transconductance of the device is controlled by the gate voltage.

In MOSFET-like CNTFET doped CNTs are used for the source and drain regions and channel is made of intrinsic semiconducting CNT.

A tunable CNTFET with electrical

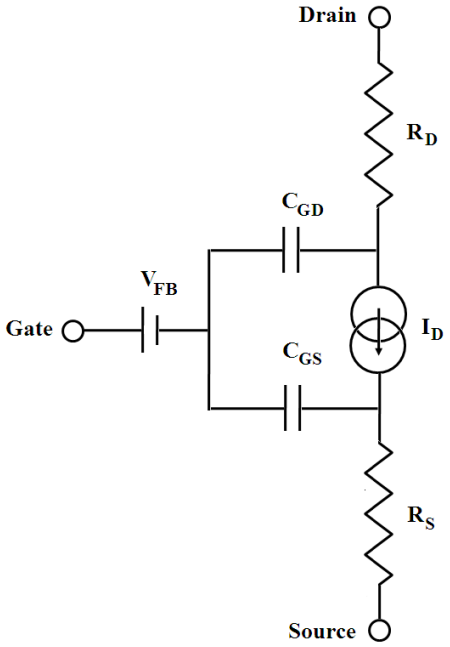


Fig. 2. Schematic of SPICE compatible CNTFET model, where C_{GS} is gate to source capacitance, C_{GD} is gate to drain capacitance, R_D is drain resistance, R_S is source resistance, V_{FB} is flat-band voltage, and I_D is drain current.

doping is also proposed. It works on the principle of barrier-height modulation by the application of gate potential.

In this work we use the SB-CNTFETs to design basic logic circuits. Before going into the realization of the high performance digital circuits using CNTFETs, let us discuss our simulation model. First we present the compact model of double gate (DG) SB-CNTFET with ambipolar characteristics. We have developed this model in Verilog-AMS using the compact model which was developed at Purdue University [8] (Fig. 2). It is a surface potential-based SPICE compatible model which is used to simulate the CNTFETs with ballistic behavior.

This model is applicable to a range of CNTs with diameter between 1 to 3 nm. The computational procedure to evaluate the drain current I_D and the total channel charge Q_{CNT} is illustrated in Fig. 3. The main quantities used in the model are the surface potential Ψ_S and the specific voltage $\xi_{i(S/D)}$ that depends on the surface potential, the subband energy level Δ_p and the source (drain) Fermi level $\mu_{S/D}$. The specific voltage is given by

$$\xi_i = \left(\frac{\Psi_S - \Delta_p - \mu_i}{k_B T} \right) . \quad (1)$$

for i = source (S), and drain (D). Here, k_B is the Boltzmann constant, and T is the operating temperature. When the conduction band minima for the first subband is set to half the nanotube bandgap Δ_1 ($\Delta_1 \approx 0.45$/diameter (in eV)) then the p^{th} equilibrium conduction-band minima Δ_p is given by [9]

$$\Delta_p = \Delta_1 \frac{\left(6p - 3 - (-1)^p\right)}{4} . \quad (2)$$

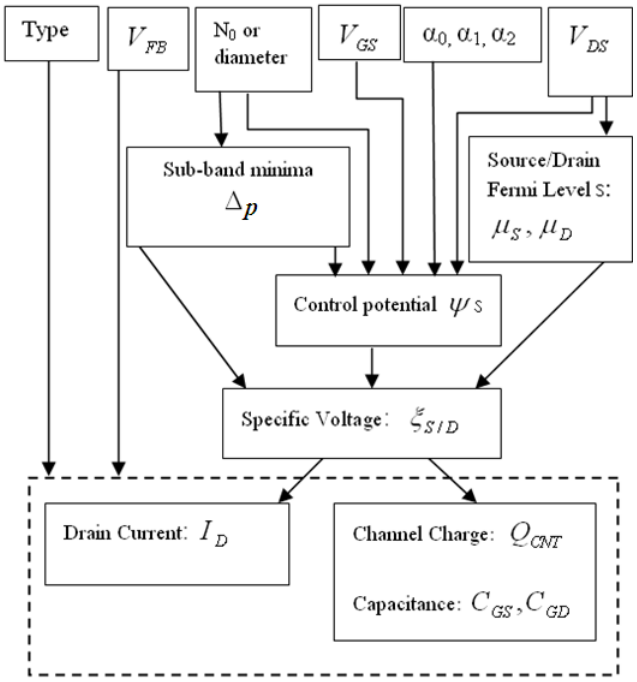


Fig. 3. Structure of CNTFET compact model.

An important step in this model formation is to get the control potential Ψ_S with gate bias voltage. The knowledge of Ψ_S is required to get the specific voltage ξ. This allows us to determine the required output parameter drain current I_D and the total charge Q_{CNT}. In [8] the following approximation is proposed.

$$\begin{aligned} V_{GS} - \psi_S &= 0 && \text{for } V_{GS} < \Delta_1 \\ &= \alpha(V_{GS} - \Delta_1) && \text{for } V_{GS} \geq \Delta_1 \end{aligned} \quad (3)$$

where the parameter α is given by

$$\alpha = \alpha_0 + \alpha_1 V_{DS} + \alpha_2 V_{DS}^2 . \quad (4)$$

where α_0, α_1 and α_2 are dependent on both CNT diameter and gate oxide thickness [8]. The total drain current I_D is given by [8]

$$I_D = \frac{4ek_B T}{h} \sum_p \left[\ln\left(1 + e^{-\xi_S}\right) - \ln\left(1 + e^{-\xi_D}\right) \right], \quad (5)$$

where p is the number of subbands, e is the charge of electron and h is the Planck constant.

The gate bias V_G required to produce the assumed Ψ_S based on the electrostatic capacitance given by [8]

$$\psi_S = V_G - \frac{Q_{CNT}}{C_{INS}} . \quad (6)$$

where C_{INS} is the insulator capacitance. The complete charge relation can be obtained by the sum of charges contributed by all the conduction bands that is populated by drain and source Fermi levels.

So in this way we obtain a simplified SPICE-compatible model of CNTFET and p-type and n-type CNTFET can be obtained by only altering the polarity of the polarity gate (PG) [10]. In the remaining part of the paper we shall use the SPICE compatible model CNTFET for logic circuit realization.

III. *I-V* CHARACTERISTICS OF CNTFET

The circuit compatible model of SB-CNTFET shown in Fig. 2 has been successfully implemented in Verilog-AMS. At first the p-type and n-type CNTFETs are modelled and simulated in SPICE. The series of *I-V* characteristics of both types of CNTFET (Fig. 4 (a) & (b)) are obtained for 1.5 nm diameter CNT with $R_{S/D}$ = 75 kΩ at room temperature (300 K). In order to demonstrate the versatility of this model, we employed it to design basic logic gates. This ambipolar CNTFETs behavior is very similar to the conventional MOSFET. The p-type characteristics are obtained when the polarity-gate voltage is set to –0.2V and the n-type characteristics are obtained when the polarity-gate voltage is set to +0.2V. These ambipolar CNTFETs are used to design circuits replacing the traditional MOS transistors. To perform the simulation of these circuits we arbitrarily decided to use 900 mV power supply and supposed that the flatband voltages are equal to +450 mV and –450 mV for n-type and p-type CNTFETs. The p-type and n-type characteristics curves shown in Fig. 4 validate the developed model in Verilog-AMS.

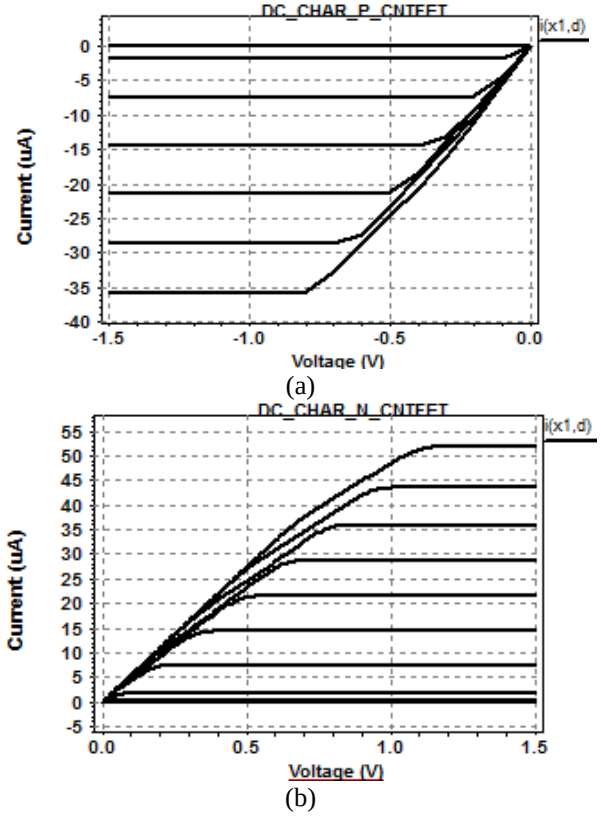


Fig. 4. (a) I_D- V_{DS} characteristics of p-type CNTFET. (b) I_D-V_{DS} characteristics of n-type CNTFET. Parameters: d = 1.5 nm, RS/D = 75 kΩ, T = 300K.

IV. DESIGN AND SIMULATION OF BASIC LOGIC CIRCUITS USING CNTFET

We have designed an inverter circuit as shown in Fig. 5(a) using CNTFET. The pull-up network (PUN) is implemented using p-type CNTFET and the pull-down network (PDN) is implemented using n-type CNTFET. The circuit is simulated in SPICE environment. The CNTFETs with diameter of 1.5 nm, shows very good result. The voltage transfer characteristic of the CNTFET inverter is shown in Fig. 5(b). There is a stiff transition between two states with a threshold voltage equal to half the power supply. The transient simulation result of the inverter circuit is shown in Fig.5(c). The waveforms indicate that there is no logic degradation in both the logic 0 and logic 1 states. The propagation delay through the gate, dynamic power dissipation, and the power delay product (PDP) are calculated which are shown in Table I.

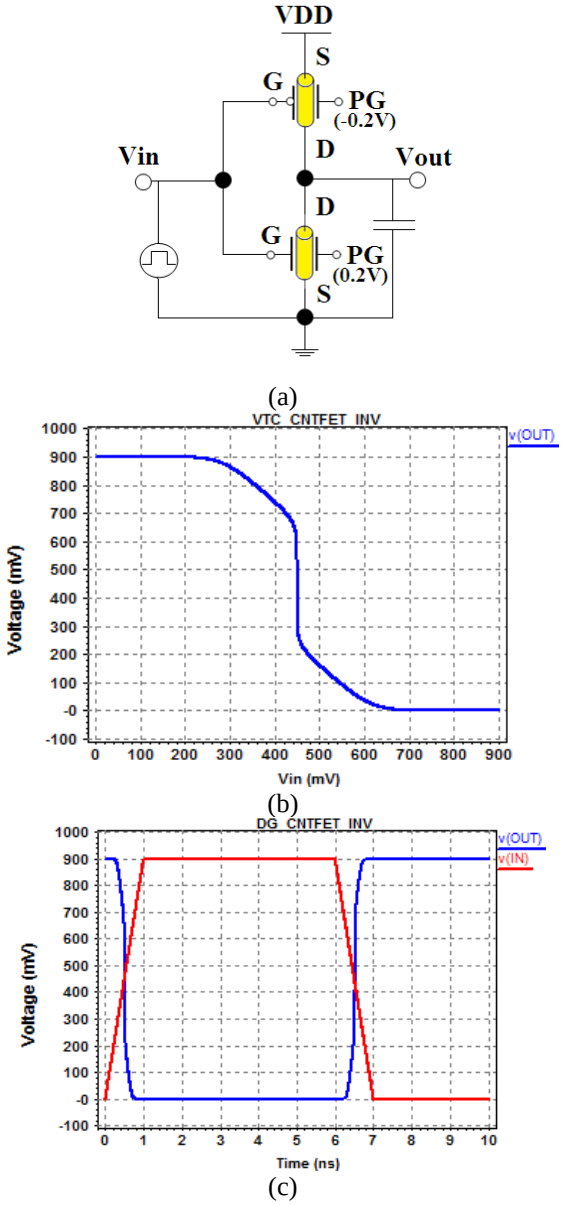


Fig. 5. CNTFET inverter (a) schematic, (b) voltage transfer characteristic, (c) and transient characteristics.

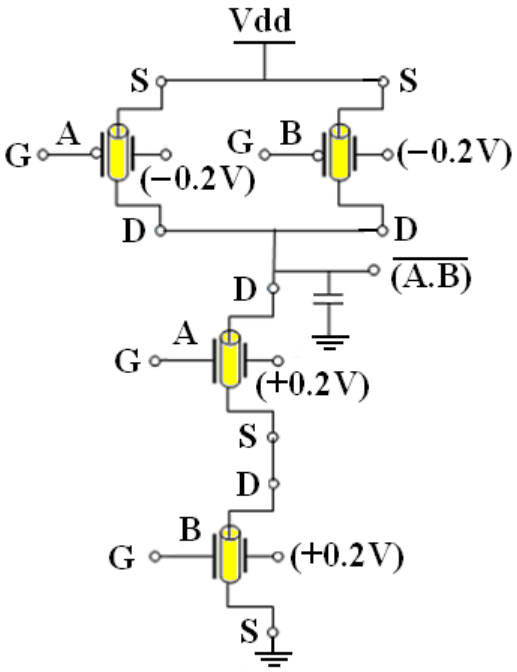


Fig. 6. Two input NAND gate using CNTFET.

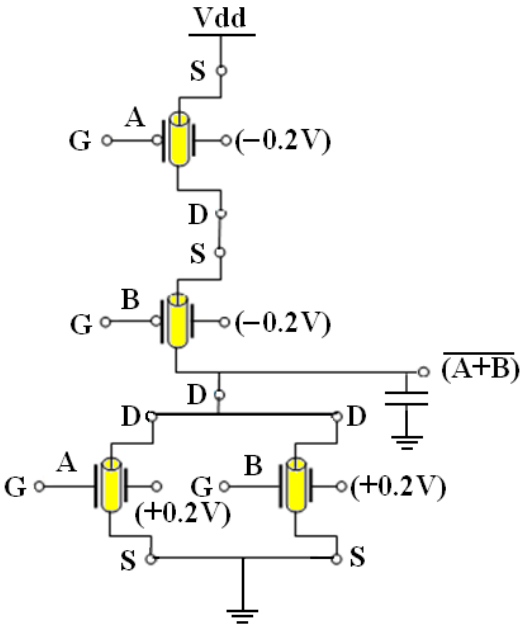
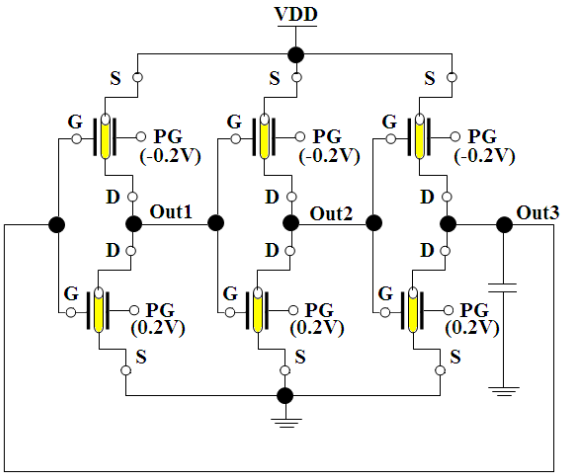


Fig. 7. Two input NOR gate using CNTFET.

Fig. 6 shows the implementation of two-input NAND logic and Fig. 7 shows the implementation of two-input NOR logic circuits. The implementation of the 3-stage ring oscillator is shown in Fig. 8(a). From the transient characteristics shown in Fig. 8(b) the time period (T) of the ring-oscillator is measured as 8.77 ps, which indicates that the frequency of the ring oscillator circuit is 114 GHz.

The transmission-gate (TG) is designed using CNTFET in this paper which is analogous to the conventional CMOS-TG. In order to demonstrate the utility of CNTFET-TG based logic, we have employed it to design basic logic gates. In a CNTFET-TG, an n-type and a p-type device are connected in parallel as shown in Fig. 9. This configuration ensures that one of the two transistors restores the signal level in all cases.



(a)

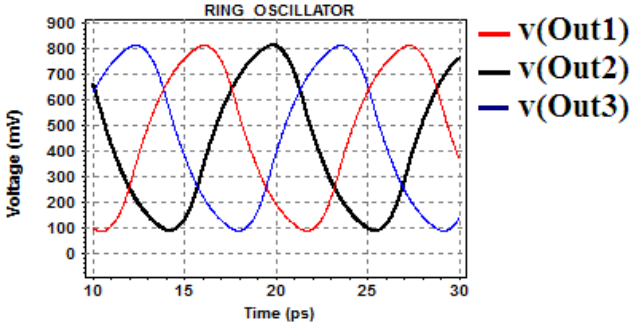


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Fig. 8. 3-stage ring oscillator using CNTFET (a) schematic (b) transient characteristics.

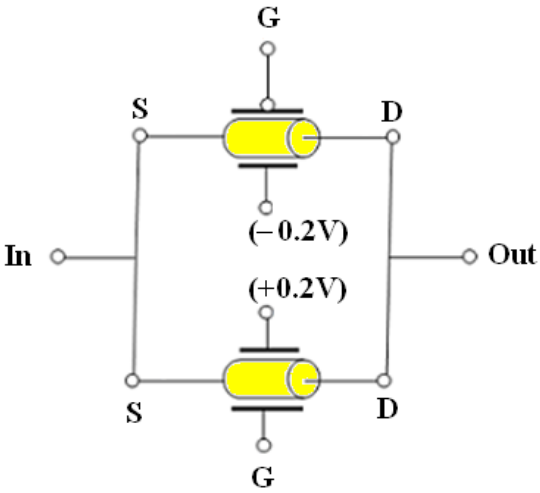
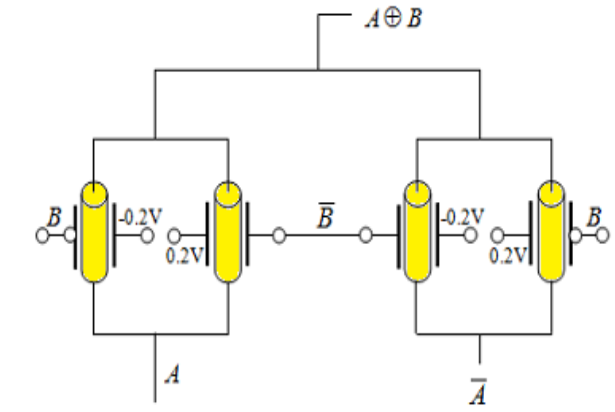
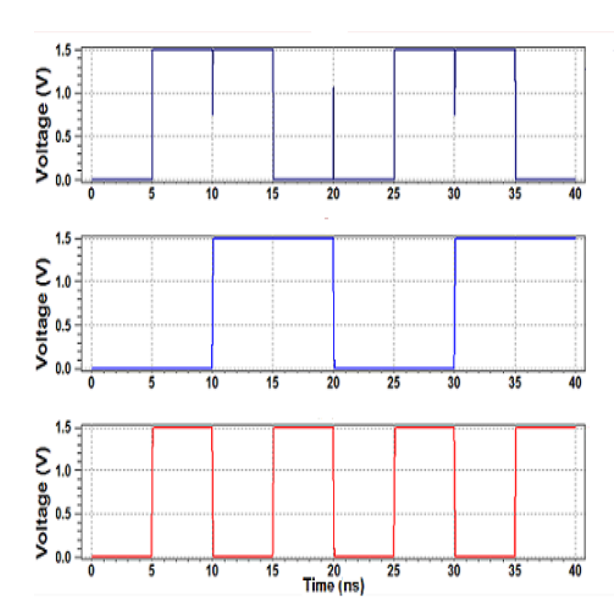


Fig. 9. Transmission-gate using CNTFET.

First we demonstrate the XOR logic implemented using CNTFET-TGs as shown in Fig. 10(a). Fig 10(b) shows the transient characteristics of TG XOR. In the XOR logic design both the polarities of *A* and *B* are needed. It is possible to implement more functions by utilizing the same configuration just by altering the inputs utilised in the XOR function. For example just by replacing A by I_0 and complement of A by I_1 we can implement the 2:1 multiplexer. The TG is the first step toward the reconfigurable logic design, i.e. by changing the inputs only the same configuration can result different Boolean functions.



(a)



(b)

Fig. 10. (a) TG XOR using CNTFET, (b) transient characteristics of CNTFET TG XOR.

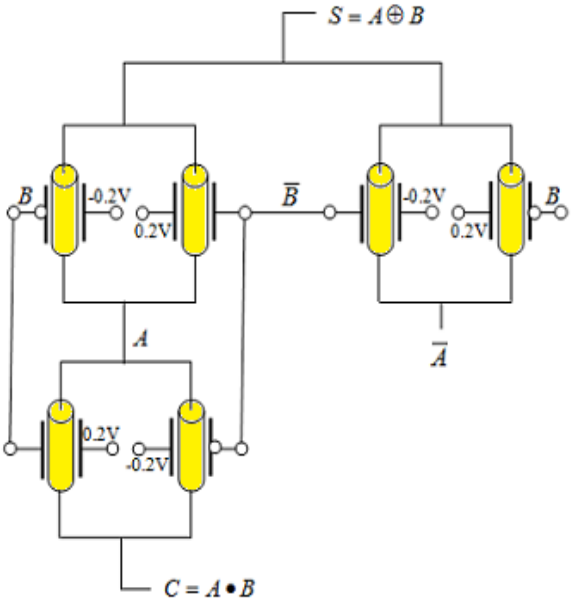


Fig. 11. Half-adder using CNTFET-TG.

Next we have designed the half-adder, and full-adder using static CNTFET logic and CNTFET-TG logic. The designs are simulated in the SPICE environment to characterize their performances in terms of power dissipation and delay. The CNTFET-TG based designs show excellent power and delay performance than the ambipolar static CNTFET logic families. The delay, power, and PDP for different logic circuits are shown in Table I and II. The results show that CNTFET-TG based logic is much superior than the static CNTFET based logic.

TABLE I
AVERAGE DELAY, POWER, AND POWER-DELAY-PRODUCT (PDP) FOR CNTFET BASED DESIGNS.

Logic block	Power (J/s) (×1e-7)	Delay (s) (×1e-9)	PDP (J) (×1e-16)
Inverter	1.80	2.52	4.53
NAND	1.84	2.58	4.74
NOR	1.82	2.54	4.63
XOR	2.10	2.58	5.41
Half-adder	2.82	6.00	16.92
Full-adder	3.21	7.09	22.76
Transmission Gate Inverter	1.40	2.24	3.14

TABLE II
AVERAGE DELAY, POWER, AND POWER-DELAY PRODUCT OF TG-XOR, TG-HALF-ADDER AND TG-FULL-ADDER

	CNTFET-TG based logic		
Logic block	Power (J/s) ($\times 10^{-7}$)	Delay (s) ($\times 10^{-9}$)	PDP (J) ($\times 10^{-16}$)
TG XOR	1.62	1.96	3.18
TG Half-Adder	1.9	4.6	8.74
TG Full-Adder	2.4	6.2	14.8

V. CONCLUSION

In this paper we have developed a SPICE compatible model for carbon nanotube field-effect transistor using Verilog-AMS. The model is used to design static logic circuits, transmission gate based logic circuits and datapath logic circuits like half-adder, and full-adder. The performances are studied in terms of power, delay, and PDP. The CNTFET-TG based logic circuits show excellent power and delay results as compared to that of CNTFET based static logic circuits. The model provides an integrated framework to support SPICE based CNTFET circuit design and simulation. The CMOS and CNTFET co-design and simulation are also enabled with this model.

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