High Speed VLSI Architecture for Multilevel Lifting 2-D DWT using MIMO

Srikanth S., M. Jagadeeswari

Abstract: ***The Discrete Wavelet Transform (DWT) Lifting architecture is a powerful signal analysis technique for non-stationary data. High speed implementation of this architecture is a challenging task. This paper proposes an efficient multi-input/multi-output VLSI architecture (MIMO) for two-dimensional lifting-based discrete wavelet transform (DWT). Computing time for this high speed architecture is as low as N^2/M for an N X N image with controlled increase of hardware cost. M is the throughput rate. The experimental results show that proposed architecture provides high throughput and power consumption compared to the conventional architecture.***

Index Terms— Discrete Wavelet Transform Lifting Scheme, MIMO, Memory Buffer, SISO.

I. INTRODUCTION

2-D DWT has evolved as essential part of modern compression system such as JPEG 2000. This is because the DWT can decompose the signals into different sub bands with both time and frequency information and facilitate to arrive a high compression ratio [1]. In addition ,a wavelet based compression system, not only presents superior compression performance over DCT ,but provides four dimension of scalabilities resolution, distortion, spatial and color, which are very difficult to achieve in DCT based compression system. In a compression system, the function of DWT is to decorrelate the original image pixels prior to compression step such that they can be amenable to compression. The computation of DWT can be done either by convolution based scheme or Lifting based scheme. The lifting scheme of computation of DWT has, however, become more popular over the convolution-based scheme for its lower computational complexity [2] .The main feature of the lifting-based DWT scheme is to break up the high pass and low-pass filters into a sequence of upper and lower triangular matrices and covert the filter implementation into banded matrix multiplications. Such a scheme has several advantages, including "in-place" computation of DWT, integer-to integer wavelet transform, symmetric forward and inverse transform.

Several lifting-based architectures have been suggested. Andra et al [4] have proposes a four processor Block based architecture which requires large internal buffer and involves significantly high latency .Wu et al[5] have

proposed a line based scanning scheme and a Folded architecture which involves simple control circuit and performs multilevel DWT using external frame buffer. Some Recursive architectures based on recursive pyramid algorithm have been proposed for concurrent implementation. The Recursive architecture [6]-[7] eliminate the requirement of external buffer but involves complex control circuits and more internal memory than Folded structures. The Frame buffer can also be eliminated by pipeline implementation [8] of multilevel algorithm, but direct mapping of multilevel DWT into pipeline architecture results poor hardware utilization efficiency. All these reported architectures are designed for a fixed processing speed and cannot be easily extended to achieve a higher processing speed. The higher processing speed has been achieved in [12] when parallel FIR structures are used. However, FIR structures result in the increase of the hardware cost

The aim of this paper is to construct an efficient multi-input/multi-output VLSI architecture (MIMO) based on lifting scheme, which meets the high processing speed requirement with controlled increase of hardware cost and simple control signals. High processing speed can be achieved when multiple row data samples are processed simultaneously. And time multiplexing technique is adopted to control the increase of the hardware cost for the MIMOA. It provides a variety of hardware implementations to meet different processing speed requirements by selecting different throughput rates.

II. CONCURRENT ARCHITECTURE FOR 2-D DWT

The computation of 2-D DWT [13] of any given level can be decomposed in two distinct stages. In stage-1, 1-D DWT Transform is performed on each of the rows of the input matrix for obtaining two intermediate coefficient matrices $[V_L]$ and $[V_H]$. In stage-2, 1-D transform is again performed on each of the columns of $[V_L]$ and $[V_H]$ for obtaining the four sub band coefficient matrices [A], [B], [C], [D].

Concurrent Architecture consists of (N/2) processing elements (PEs), arranged in a linear array structure. The input data of size (N x N) is cyclically extended by one row and one column and fed line-by-line from bottom to top order to the input register. Row of input consisting of (N+1) samples is fed to the input- interface (IP-1) of the structure of size (N+1) such that during the (m+l)-th cycle period the n-th PE will receive the sample values {A°(m, N+2-2n), A°(m, N+1-2n), A°(m, N-2n)} from the PIPOSR and the intermediate values {rl(m, M-n-i), r2(m, M-n-1), VH(m, M-n-l)}from the (n+l)-th section, where=N/2. The intermediate values {r1 (m, M-n-1), r2 (m, M-n-1), V_H (m, M-n-1)1 corresponding to the (M/2)-th PE are initialized to zero.

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S. Srikanth.S, ME VLSI DESIGN, Sri Ramakrishna Engineering College, Coimbatore, Tamilnadu, INDIA, +919940717614.
(E-mail: sri88sns@gmail.com).
M. Jagadeeswari, Professor & Head, M.E VLSI DESIGN , Sri Ramakrishna Engineering college, Coimbatore, Tamilnadu, INDIA, 9486355965, (E-mail:jagadee_raj@rediffmail.com).

Each PE consists of two sub cells working in separate pipeline stages. Subcell-1 performs the computations pertaining to stage-1, while subcell-2 performs the computations of stage-2.Each subcell-1 comprises of four multiplier-adder units (MU), where each MU consists of one multiplier and two adder units. Each MU performs computations pertaining to one lifting step. Each of the multipliers stores the lifting constant corresponding to the lifting step. The multiply-add operation of the MU is performed serially in one computation cycle, where a computation cycle is defined as T= Tm +2Ta. Subcell-1 will produce the high-pass intermediate output (V_H) and low-pass intermediate output (V_L) after a latency of 3 and 4 cycles, respectively. The successive outputs of a subcell-1 correspond to the successive samples of a given column of the intermediate matrix which can be used directly as the input for stage-2 without any intermediate buffering or transposition.

The entire computation of stage-2 is mapped into a subcell-2 parallel-in parallel-out shift register (PIPOSR). In every cycle, subcell-2 receives two intermediate output from subcell-1 and performs the corresponding filter computations in time multiplexed form using a 9/7 wavelet filter [3]. Each subcell-2 consists of four MU, one input delay unit (ID), three middle delay units (MD) and one scale normalization unit (SU). The ID consists of two SIPOSR corresponding to the intermediate outputs V_L and V_H and three 2-to-1 line MUX. Each MUX selects the input alternately from two SIPOSR. MU1, therefore, receives the required input samples in each cycle from the ID through the MUX. The DWT components of a pair of sub bands D' and B are obtained from MU4 of subcell-2 during (i+4)-th cycle, and sub bands C' and A' are obtained during (i+5)-th cycle. The components of the sub band A' and D' need a scale normalization operation.

III. PROPOSED EFFICIENT MIMO FOR 2D LIFTING-BASED DWT

A 2D DWT consists of horizontal filtering along the rows followed by vertical filtering along the column. The proposed Architecture is suitable for any lifting-based DWT. The throughput rate is denoted by a 1D variable M, which is an even integer. To illustrate the proposed MIMOA, CDF97 is selected as an example. By assuming M is 8, the original image size N X N = 16 X 16, and the original image is represented in matrix format as shown below.

$$X = \begin{bmatrix} x_{0,0} & \cdots & x_{0,15} \\ \vdots & \ddots & \vdots \\ x_{15,0} & \cdots & x_{15,15} \end{bmatrix}$$

A. Architecture for the Horizontal Filtering Along the Rows

First, CDF97 is applied to the row dimension, which is a 1D DWT. The architecture for the horizontal filtering along the rows consists of eight SISO modules as shown in fig 1. The input data flow is shown in Fig. 2.

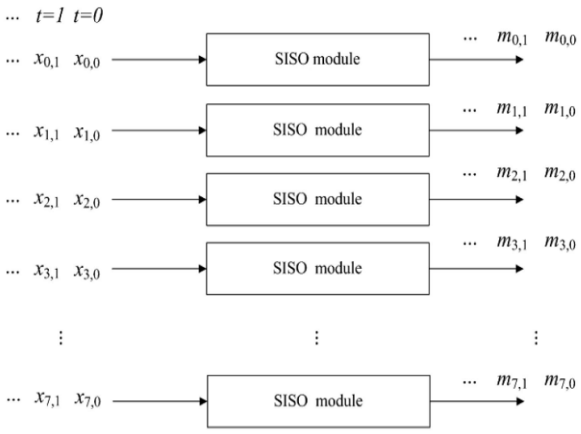

Fig. 1 Architecture for the horizontal filtering

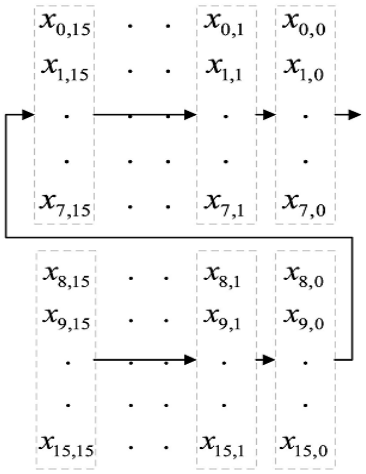

Fig. 2 Input data flow of the architecture for the horizontal filtering

The elements from each row are processed by one SISO module. We can accordingly get output data flow of the architecture for the horizontal filtering, as shown in Fig. 3, where $m_{i,j}$ denotes the computation results after we apply CDF97 to the row dimension. Many SISO architectures for the 1D DWT are proposed. An efficient SISO architecture is proposed in [9] by employing the fold technique. Therefore, we adopt it in our SISO modules, which consist of two multipliers, four adders, and ten registers.

B. Architecture for the Vertical Filtering Along the Columns

Second, CDF97 is applied to the column dimension. Eight elements from each column arrive simultaneously.

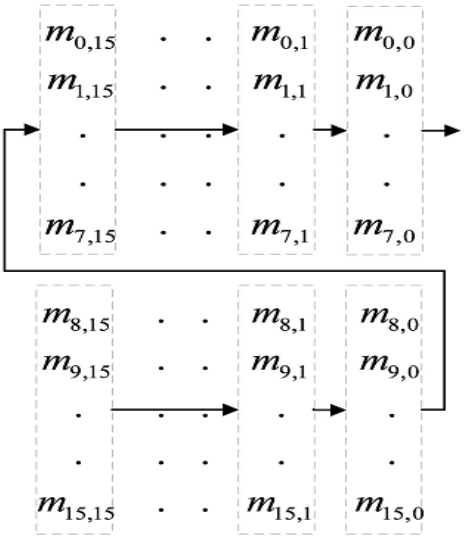

Fig. 3 Output data flow of the architecture for the horizontal filtering

One solution is to design an eight-input/eight-output architecture by directly mapping, which can process eight elements per clock cycle. However, it will lead to a complex architecture, which has complicated control signals and cannot be easily extended for its irregularity. The eight-input/eight-output architecture will be more complicated. The problem can be solved by time multiplexing technique, which converts the possible complex architecture into a combination of some simple TITO modules. The proposed architecture for the vertical filtering is shown in Fig. 4. It consists of four TITO modules, some multiplexers (mux), and line delay registers (LD).Each TITO module is designed to receive two elements simultaneously. The LD is composed of some delay registers, which are used to temporarily store the elements. Port A (Port B, Port C, Port H) is used as a symbol to demonstrate how the mux works. The elements, which have been delayed by the LD, will be selected by the mux and sent to TITO modules at a proper time. The LD is composed of some delay registers, which are used to temporarily store the elements. Port A (Port B, Port C, Port H) is used as a symbol to demonstrate how the mux works.

The elements, which have been delayed by the LD, will be selected by the mux and sent to TITO modules at a proper time. The number of delay registers in LD (LD1, LD2, LD3) is determined by the rule: The time interval arriving at the same TITO module for every two elements from one column is constant. The time interval is measured by the number of clock cycles (ccs). The computation time interval between the first pair and the second pair of the elements from one column is Δccs. Therefore, the number of the input in the architecture for the vertical filtering is M, then the computing time interval between the first pair and the $(M/2+1)^{th}$ pair is M/2 x Δccs. On the other hand, from Figs. 5 and 6, the time interval between the first pair and the $(M/2+1)^{th}$ pair arriving at the same TITO module is equal to

(N pixels $_x$ M) / (M pixels $_/$ccs) = N ccs (1)

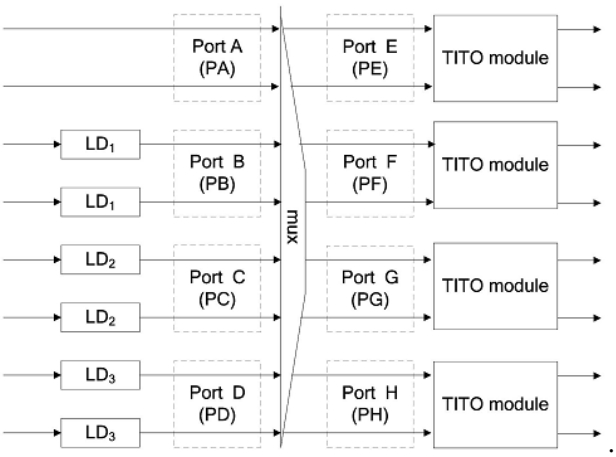

Fig. 4 Architecture for the vertical filtering

Therefore, the following formula should be satisfied:

M/2 x Δ =N (2)

By solving (2) we get

Δ= (2N/M) (3)

By considering M = 8 and N =16 .Then $m_{0,0}$ $m_{1,0}$ will arrive at PE in clock (CLK) 0. $m_{2,0}$ $m_{3,0}$ in CLK 4, $m_{4,0}$ $m_{5,0}$ in CLK 8, $m_{6,0}$ $m_{7,0}$ in CLK 12, $m_{8,0}$ $m_{9,0}$ in CLK 16, The number of delay registers in LD1, LD2, LD3 are separately four, eight, and twelve. The input and output data flow of the mux is shown in Fig. 5 and 6,

Fig. 5 Input data flow of the mux

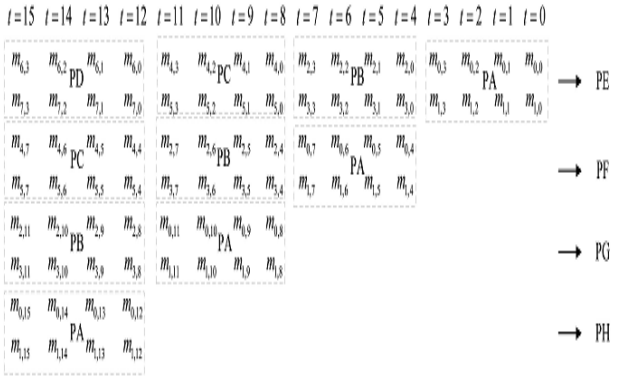

Fig. 6 output data flow of the mux

respectively. The selected time interval for the mux from one input port to another is equal to Δccs. The architecture of the TITO module is shown in Fig. 7. The LD4 is used to synchronize the intermediate results of the vertical filtering, in which the number of delay registers is equal to Δ.

C. MIMOA for 2D Lifting-Based DWT

If the particular application requires higher processing speed, then throughput rate M will be larger than 8. The proposed MIMOA is M SISO modules, M/2 TITO modules, some multiplexers, and delay registers, which is shown in Fig.8. "2N/M D" in Fig. 8 represents that the number of delay registers is 2N/M. The number of registers required in one SISO module is 10. Thus, the total number of registers required in MIMOA is given by

$$= M \times 10 + 2\,[2N/M + 4N/M + \ldots.. + [(M-2)\,N]/M + [M/2] \times 5 \times [2N/M]$$

$$= 10M + N\,(M-2)/2 + 5N \quad (4)$$

$$= 10M + (NM/2) + 4N$$

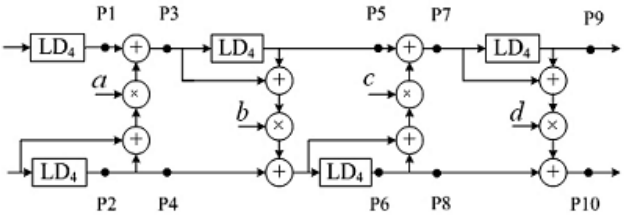

Fig. 7 Architecture of the TITO module

The number of the required adders is equal to

$$4M + (M/2) \times 8 = 8M \quad (5)$$

The number of the required multipliers is equal to

$$2M + (M/2) \times 4 = 4M \quad (6)$$

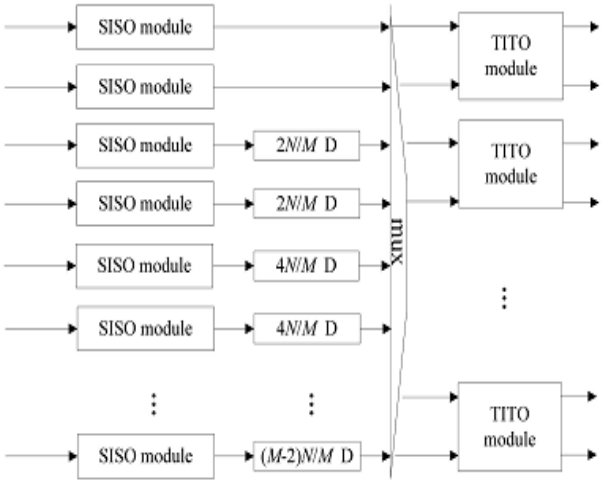

Fig. 8 MIMOA for 2D lifting-based DWT

IV. COMPARISON AND RESULTS

The hardware cost is measured by the number of multipliers and adders used in the architecture. The on-chip memory refers to the number of registers consumed (the width of the register is equal to the word length for the internal data). The computing time is normalized as clock cycles. Compared with the similar architectures, computing time of MIMOA is reduced with less increase of hardware cost. The proposed design is simulated and synthesized using Xilinx 10.1i. A comparison is among different 2D DWT architectures for the CDF97 as shown in Table I.MIMO architecture is compared in terms power delay Product and speed performance as shown in Table II.

Table I
Comparison Among Different 2d Dwt Architectures For The Cdf97

Architecture	Multiplier	Adder	DWT Scheme
Chrysafis [9]	32	28	Convolution
Wu [5]	32	32	Convolution
Dillen [10]	16	24	Lifting
Barua [11]	10	16	Lifting
Cheng [12]	24	76	FIR
Proposed	4M	8M	Lifting

TABLE II COMPARISON OF POWER DELAY AND SPEED PERFORMANCE

Sl. No.	Architectur	Power delay product(ns)	Speed Performance (MHz)
1.	Folded	4.207	20.438
2.	Recursive	3.8493	21.562
3.	Pipelined	3.023	25.463
4.	MIMO	2.7545	29.769

V. CONCLUSION

An efficient MIMOA for 2D lifting-based DWT is proposed in the paper. It provides a variety of hardware implementations to meet different processing speed requirements with controlled increase of hardware cost and simple control Signals. To evaluate the performance of the proposed architecture, different 2D DWT architectures have been compared.

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REFERENCES

1. S. Mallat, "A Theory for Multiresolution Signal Decomposition: The Wavelet Representation," IEEE Trans. Pattern Analysis and Machine Intelligence, Vol. 11, No. 7, pp. 674–693, July 1989.
2. W. Sweldens, "The Lifting Scheme: A Custom-Design Construction of Biorthogonal Wavelets," Applied and Computational Harmonic Analysis, Vol. 3, pp.186-200, 1996.
3. B.F.Wu and C.F. Lin, "High-performance memory-efficient pipeline architecture for the 5/3 and 9/7 discrete wavelet transform of JPEG 2000 codec," IEEE Trans. on Circuit and System for Video Technology, vol.15, no.12, pp.1615-1628, Dec. 2005.
4. Andra, K. Chakrabarti, C. and Acharya, T. "A VLSI Architecture for Lifting-based Forward and Inverse Wavelet Transform," IEEE Trans.Signal Process., Vol. 50, No. 4, pp. 966–977, 2001.
5. Wu, P.C. and Chen, L.G. "An Efficient Architecture for Two-Dimensional Discrete Wavelet transform," IEEE Trans. Circuits Syst. Video Technol., Vol. 11, No. 4, pp. 536–545.
6. Huang, C.T. Tseng, P.C. and Chen, L.G. "Generic RAM-based Architectures for two-Dimensional Discrete Wavelet Transform with Line based method," IEEE Trans. Circuits Syst. Video Technol., Vol. 15, No. 7, pp. 910–920, 2005.

7. Huang, C.T. Tseng, P.C. and Chen, L.G. "Analysis and VLSI architecture for 1 D and 2 D DWT," IEEE Trans. Signal Process., Vol.53, No.4, pp.1575-1586, Apr. 2005.
8. Xin Tian , Lin Wu , Yi-Hua Tan "Efficient Multi-Input/Multi-Output VLSI Architecture for Two-Dimensional Lifting-Based Discrete Wavelet Transform," IEEE Transactions on Computers, vol. 60, no. 8, August 2011.
9. Chrysafis C. and Ortega A., "Line-Based, Reduced Memory, wavelet Image Compression," IEEE Trans. Image Processing., vol. 9, no. 3, pp. 378-389, Mar.2000.
10. Dillen G. et al., "Combined Line-Based Architecture for the 5-3 and 9-7 Wavelet Transform of JPEG2000," IEEE Trans. Circuits and Systems for Video Technology, vol. 13, no. 9, pp. 944-950, Sept. 2003.
11. Barua, S. Carletta J.E., Kotteri K.A., and Bell A.E., "An Efficient Architecture for Lifting-Based Two-Dimensional Discrete Wavelet Transform, "Integration, the VLSI J., vol. 38, no. 3, pp. 341-352, 2005.
12. Cheng C. and Parhi K.K., "High-Speed VLSI Implementation of 2D Discrete Wavelet Transform," IEEE Trans. Signal Processing, vol. 56, no. 1, pp. 393-403, Jan. 2008.
13. Meher, P. K. Mohanty, B. K. and Patra, J. C.(2008) 'Memory Efficient Modular VLSI Architecture for High throughput and Low-Latency Implementation of Multilevel Lifting 2-D DWT'. IEEE Transactions on Signal processing, vol. 59, no. 5, may 2011.

AUTHORS PROFILE

M. Jagadeeswari received her B.E Electronics and Communication Engineering from Government College of Technology, Coimbatore and ME (Applied Electronics) from P.S.G College of Technology, Coimbatore in the year 1992 and 1999 respectively. She has completed her PhD from Anna University, Chennai, India in 2010. She is presently working as Professor and head in the department of Electronics and Communication Engineering (PG) at Sri Ramakrishna Engineering College, Coimbatore, India. She has published more than 25 research papers in the National & International Journals/ Conferences. Her research interests are VLSI design, Hardware Software co-design, Computer architecture and Genetic algorithms.

S. Srikanth received his B.E. degree in electronics and communication engineering from S.N.S College Of Technology, Coimbatore. He is currently pursuing his M.E. degree in VLSI design at Sri Ramakrishna Engineering College, Coimbatore. His area of interest is VLSI signal processing and Computer Architecture.