Design of Phase Frequency Detector and Charge Pump for High Frequency PLL

S. B. Rashmi, Siva S. Yellampalli

Abstract*— A simple new phase frequency detector and charge pump design are presented in this paper. The proposed PFD uses only 4 transistors and preserves the main characteristics of the conventional PFD. Both PFD and charge pump are implemented using cadence 0.18 µm CMOS Process. The maximum frequency of operation is 5 GHz when operating at 1.8V voltage supply. It has free dead zone. It can be used in high speed and low power consumption applications. This makes the proposed PFD more suitable to low jitter applications.

***Index Terms*— PFD, PLL, High speed.**

I. INTRODUCTION

Phase locked loop (PLL) is a main block in many applications such as wireless communication systems, digital circuits, and receivers. It is a clock or carrier generator. These applications need low power blocks to have long life battery. The Two non linear components present in PLL are Phase Frequency Detector (PFD) and Voltage controlled oscillator (VCO). The main concept of PFD is comparing two input frequencies in terms of both phase and frequency. In a PLL the two frequencies are reference frequency (Fref) and the voltage controlled oscillator (VCO) output after division by N (Fvco). The output is a pulse proportional to the phase difference between the inputs and it drives the charge pump to either increase the control voltage of the VCO or decrease it or keep it without change. A PFD is usually built using a state machine with memory element such as D flip-flop. There are many topologies moving towards simplifying the circuit and reducing the dead zone. Dead zone is a main property in the PFD phase characteristics as it introduces jitter to the PLL system. The PFD doesn't detect the phase error when it is within the dead zone region, then PLL locks to a wrong phase. This paper presents a novel PFD architecture. is composed of only 4 transistors. It has free dead zone, consumes low power, and operates at high speed.

II. PHASE FREQUENCY DETECTORS

The basic architecture of a PFD is the conventional PFD as shown in Figure 1. D-FF is implemented using CMOS logic. It has the drawbacks of dead zone, high power consumption when operating at high frequency as the internal nodes are not completely pulled up or pulled down, limited speed as the maximum operation frequency is inversely proportional to the reset pulse width of the circuit, and large area for large no. of transistors. Inverters are used as a delay circuit to reduce dead zone [1]

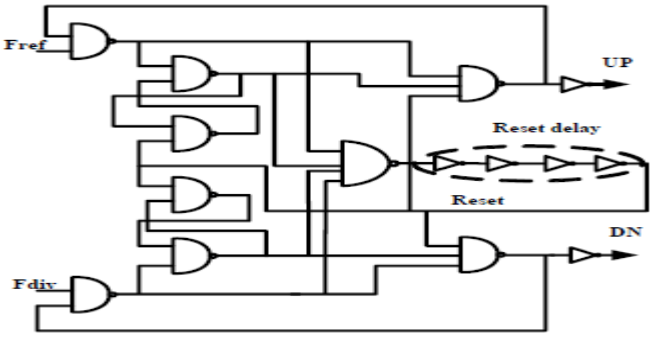

Fig. 1 Architecture of conventional PFD

TSPC D-FF is more used in designing D-FF of PFD for supporting high speed operation (Johnson et al, 2004). Modified pre-charge type PFD (MPt-PFD) is designed using TSPC-DFF as shown in Figure 2. It has free dead zone using 16 transistors (Lee et al, 1999).

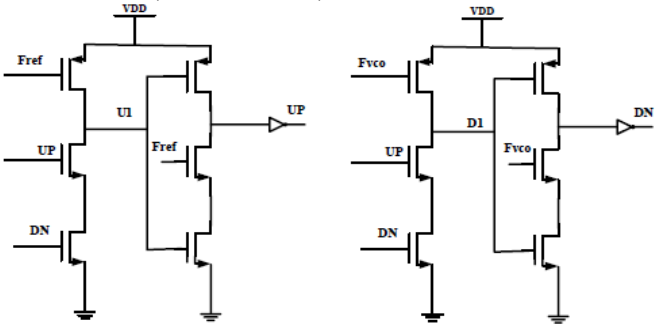

Fig. 2 PFD designed by using TSPC D-FF

III. DEAD ZONE

As we mentioned before, dead-zone is due to small phase error. When the phase difference between PFD's input signals, the output signals of the PFD will not be proportional to this error [10]. The reason of this problem is the delay time of the internal components of the flip-flop and the reset time that need s the AND gate to reset both flip flops [11]. Figure 3 illustrates the dead zone problem. When the two clocks are very close to each other (small phase error), due to the delay time the reset delay, the output signals UP and DOWN will not be able to charge and no output will signal leading to losing this small difference.

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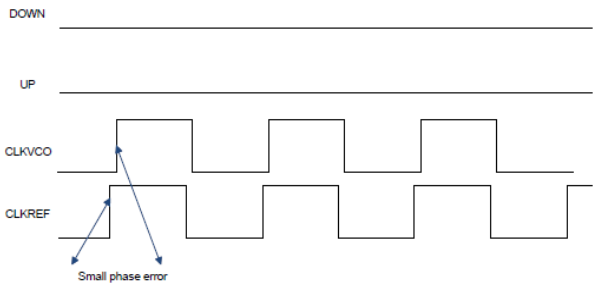

Fig 3 : Dead Zone

Figure 4 illustrates the output voltage vs. the phase error measured by the PFD. Figure.4a illustrates the relation in no dead zone PFDs, while figure 4b illustrates the relation in the presence of a dead zone. We can see that in a dead zone PFDs the relation become nonlinear around zero. This is due to inability to detect the phase error in this region. Plenty of solution has been done for this problem some of them reduce the delay time in the internal components of the PFDs, other solution eliminate the reset path by implementing new reset techniques that will not create a delay and produce a high speed PFDs

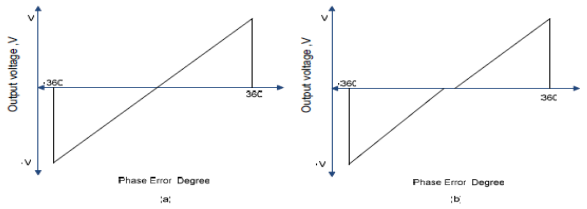

Figure 4: Phase Error vs. Output Voltage
No Dead Zone (b) Dead Zone

IV. PROPOSED PHASE FREQUENCY DETECTORS AND ITS SIMULATION RESULTS

The circuit diagram of proposed PFD is as shown in below figure 7 it works similar to conventional PFDs but it has many advantages compared to conventional PFDs. This PFDs is basically constructed with two GDI (Gate Diffusion Input) cells. A basic GDI cell contains four terminals – G (common gate input of nMOS and pMOS transistors), P (the outer diffusion node of pMOS transistor), N (the outer diffusion node of nMOS transistor), and D (common diffusion node of both transistors) . This technique allows reducing power consumption, propagation delay, and area of digital circuits. The GDI method is based on the simple cell shown in Figure Table I shows how different logic functions implemented with GDI cell.

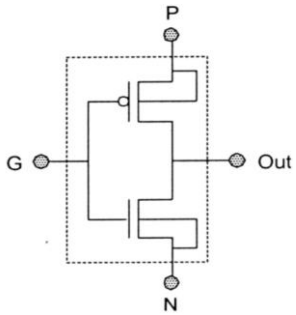

Fig 5 Basic GDI cell

When Fclk is equal to Fvco both the outputs that is Up and Down are zero, if Fclk is high compared to Fvco Then up signal is high else down signal is high indicating the phase error between Fclk and Fvco The conditions of inputs and outputs are depicted in state machine diagram shown in fig 6.

TABLE I. LOGIC FUNCTIONS IMPLEMENTED WITH GDI CELL

N	P	G	D	Function
„0"	B	A	A"B	F1
B	„1'	A	A"+B	F2
„1"	B	A	A+B	OR
B	„0"	A	AB	AND
C	B	A	A"B+AC	MUX
„0"	„1"	A	A"	NOT

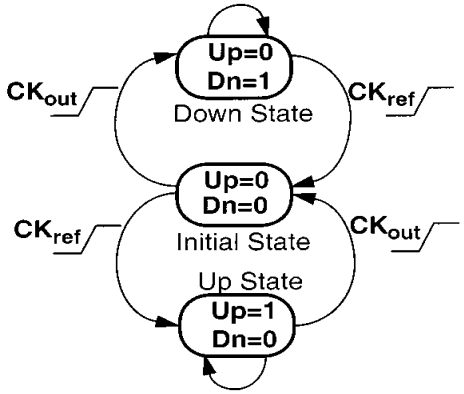

Fig 6 PFD state diagram

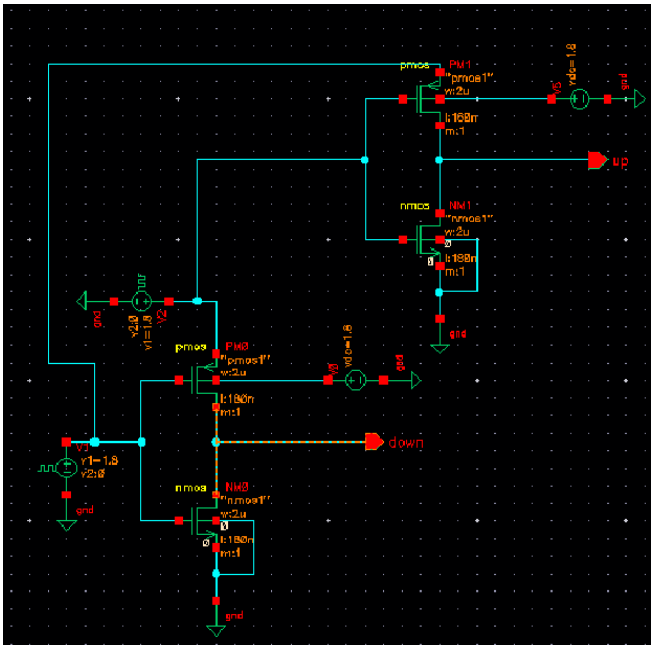

Fig 7 Circuit diagram of the proposed PFD

Inputs(Fclk and Fvco) and outputs(Up and down) of the proposed logic at 5 GHZ is as shown in below fig 8. Outputs are verified according to the state machine diagram.

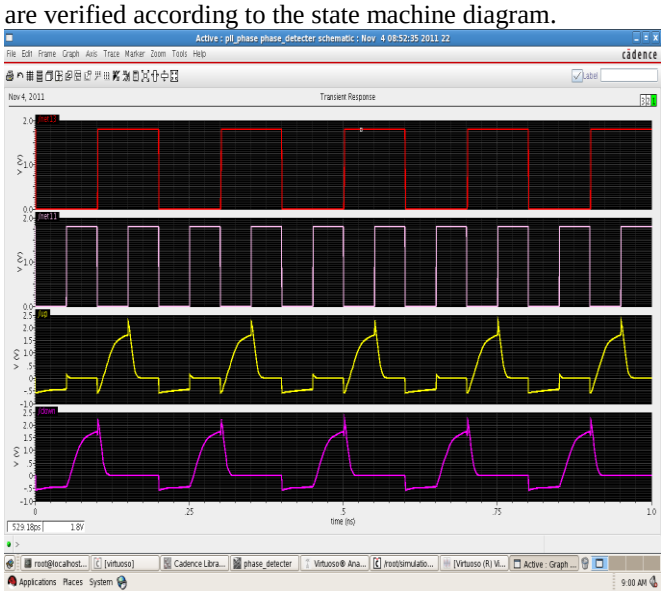

Fig 8 Input and output waveforms of the proposed PFD

V. FREQUENCY ANALYSIS

The maximum operation frequency is defined as the shortest period with correct UP and DN signals together with the inputs have the same frequency and 90 degree phase difference [7]. A comparison of maximum operation frequency between conventional PFD, TSPC-PFD and proposed PFD is shown in Figure 9. The comparison shows the variations of the maximum operation frequency with supply voltage. At 1.8V voltage supply the maximum operation frequency of the conventional PFD is 500 MHz, for MPt-PFD is 1.5 GHz and proposed PFD is 4.5Ghz .This indicates that proposed PFD is reliable in high speed applications.

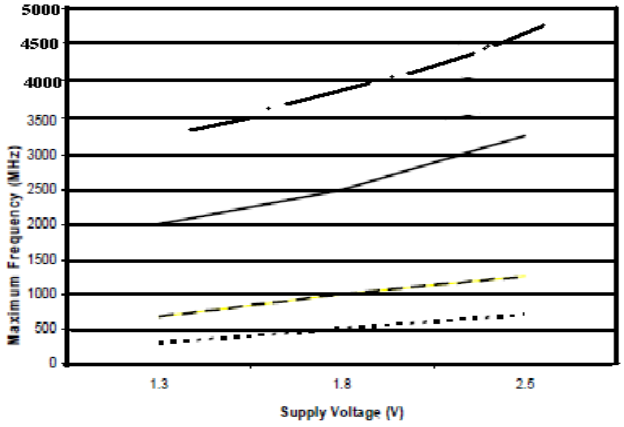

Fig 9 Maximum operation frequency function of supply voltage for various PFDs

Figure10 shows a longer simulation done on proposed PFD. The input CLK frequency is 500 MHz with Fclk leading Fvco by 20ps; this will result in having UP signal as we can see from the graph. This PFD were able to operate at much higher frequency 5GHZ is the highest frequency the PFD will operate at. Even at the phase difference of 20ps between Fclk and Fvco the proposed PFD is able to detect the difference which is depicted in fig10.

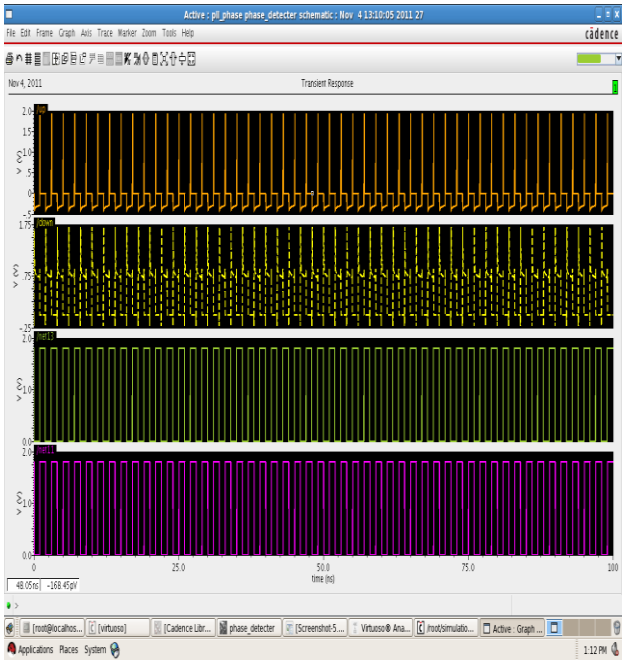

Fig 10 Simulation results of the proposed PFD with a delay of 20ps

VI. TEMPERATURE ANALYSIS

Parametric analysis is done on PFD on variable temp the range is from 10 degrees to 100 degrees the analysis response is depicted in fig11. This indicates that proposed PFD is invariant with temperature. The delay of the proposed architecture is 19.71ns and is depicted in fig 12 This indicates that dead zone of the proposed architecture is approximately 20 ns and is much superior when compared with the conventional PFDs.

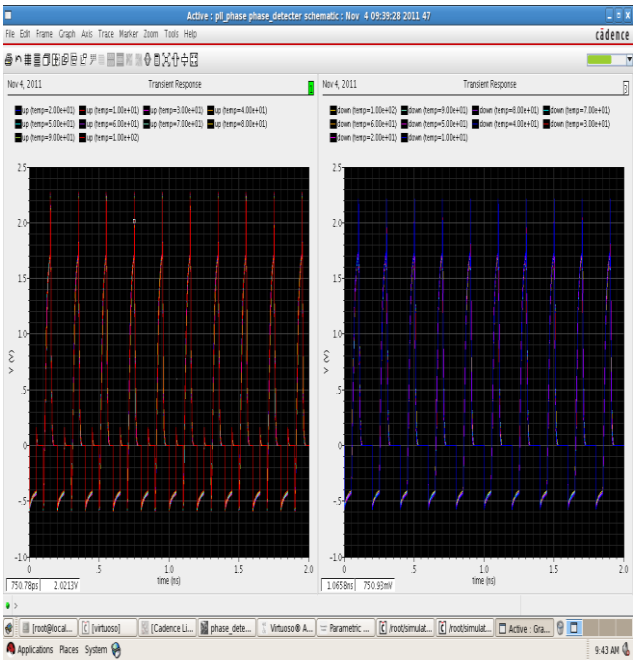

Fig 11 PFD output waveforms of parametric analysis for temperature ranging from 10 degrees to 100 degrees

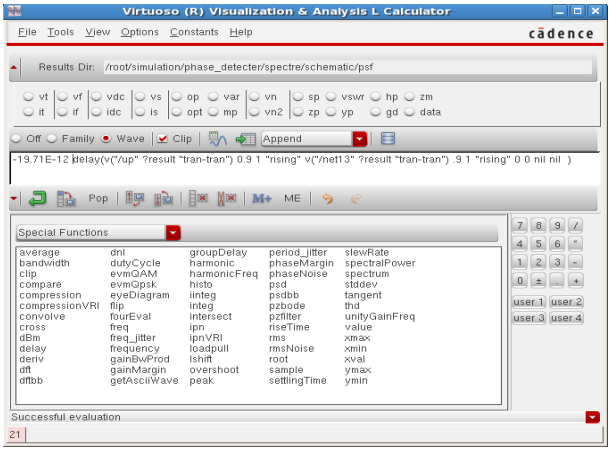

Fig 12 Delay output

Figure 13 shows the graph of the power measurement

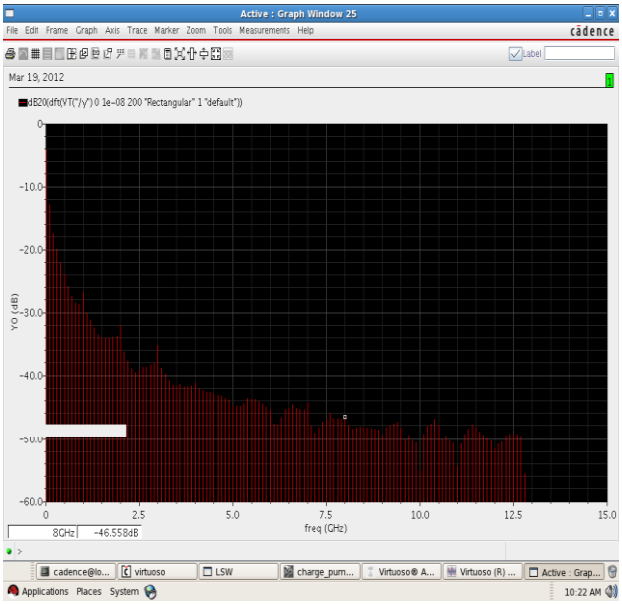

Fig13. Power measurement

TABLE 2.PERFORMANCE COMPARISON BETWEEN DIFFERENT PFD TOPOLOGIES

Sl noPFDs	No of transistor	Power consumption	Maximum operating frequency	Dead zone
Conventional	48	33.5uW	500MHz	100 ps
T PFD	16	10uW	1.5GHZ	65ps
Proposed	4	8uW	5GHz	20ps

VII. CHARGE PUMP

Charge Pump is the circuit that translates the UP and DOWN signals from the PFD to control voltage that will control the VCO. As shown in Fig.14, charge pump consist of two switched current sources implemented using NMOS and PMOS diode connected load. Charge pump is switched on and off by the PFD output signals UP and DOWN. This charge pump consists of two switched current sources that pump charge into or out of the loop filter according to the PFD output. When the reference leads the feedback signal, the PFD detects a rising edge on the reference frequency and it will produce an UP signal. This UP signal from the PFD will turn the UP switch (PMOS) on, and it will cause the CP to inject current into the loop filter, increasing Vout. When the feedback leads the reference signal, the PFD detects a rising edge on the feedback signal and will produce a DOWN signal. This DOWN signal from the PFD will turn the DOWN switch (NMOS) ON, and the CP will sink current out of the loop filter thus, decreasing Vout The current through the UP switch(PMOS), and the current through the DOWN switch(NMOS), need to be equal in order to avoid any current mismatch. The minimum charge pump current is limited by the switching speed requirements. Fig.15 shows the complete simulation result of phase detector with charge pump. It shows that the capacitor is charging only when the UP is high, and will be stable if the UP and DOWN both are low and vice versa.

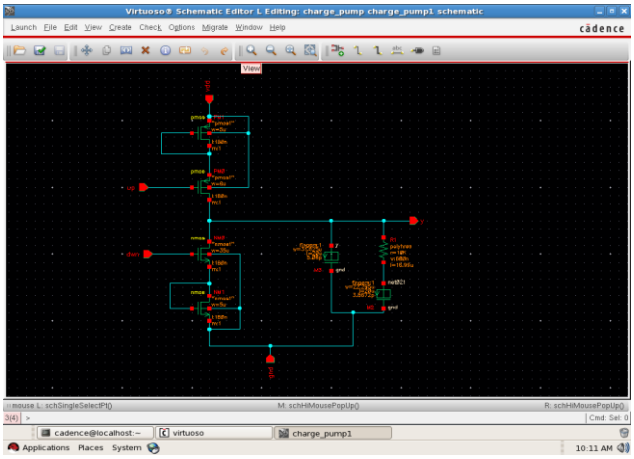

Fig 14 Circuit diagram of charge pump

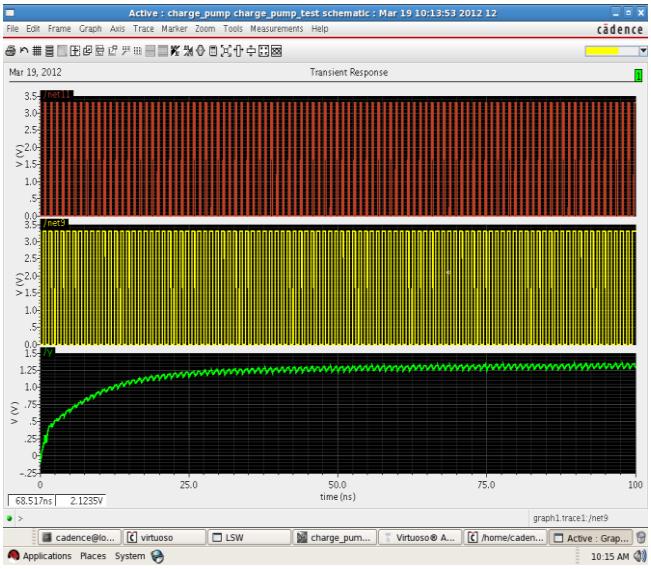

Fig 15 Input and output waveforms of charge pump

VIII. LAYOUTS

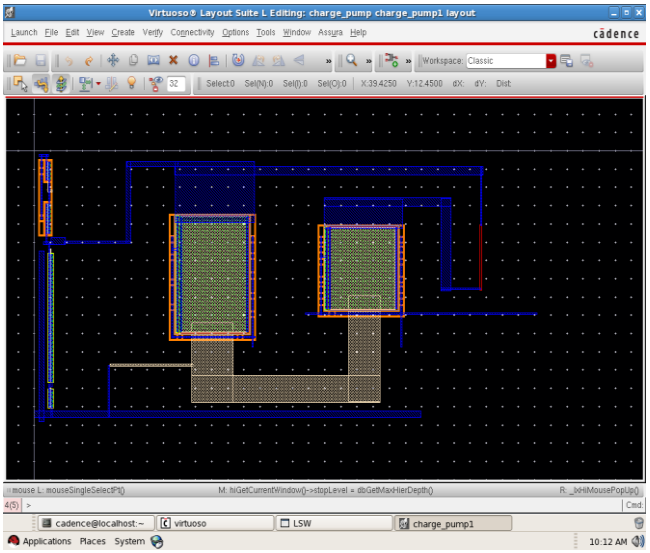

Fig 16 Layout of charge pump

Both phase frequency detector and charge pump are implemented using cadence virtuoso 0.18um. Layout of phase frequency detector and charge pump are depicted in fig 16 and Fig 17.

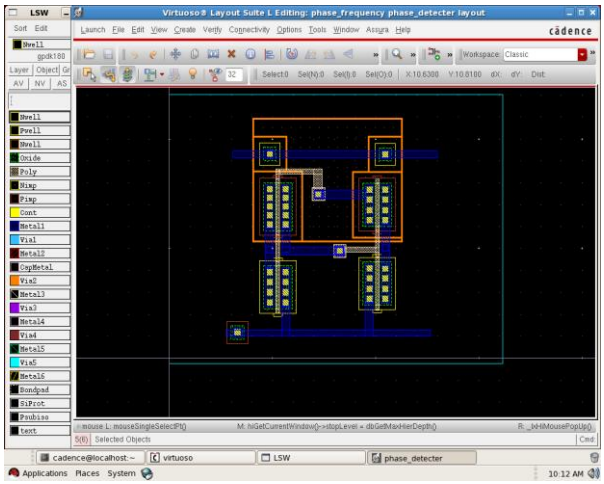

Fig 17 Layout of phase frequency detector

IX. CONCLUSIONS

This paper presents new PFD and charge pump design implemented using cadence 0.18 μ*m* CMOS process. PFD is composed of 4 transistors, and preserves the main functionality of a conventional PFD. The circuit operates at a frequency of 5 GHZ with dead zone of 20ps

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