Modeling and Simulation of Triple Metal Cylindrical Surround Gate MOSFETs for Reduced Short Channel Effects

Santosh Kumar Gupta, S. Baishya

Abstract*— Due to the continuous scaling of the MOS transistors it has become absolute necessary to investigate for the new transistor architectures for better control of SCEs and HCEs. In literature triple metal and double metal gate structure has been proposed to reduce the SCEs and HCEs due to scaling of the MOS transistors. The double metal and triple metal structures screen the effect of drain voltage change on the source/channel barrier reducing the SCE. The triple metal gate structure however induces an electrical junction on source and drain side which works as ultra shallow source/drain junctions. Since the surround gate structures have been found to have best control over the channel a cylindrical surround gate structure with triple metal was recently proposed by Cong Li et al. In this paper we present the physically based analytical model for the surface potential of triple metal cylindrical surround gate MOSFET. The model takes into account for the drift-diffusion currents and continuity equations. In the latter part of the paper some 2D simulation results of triple metal gate MOS transistor has been shown. The device has also been explored for the suitable channel doping in terms of subthreshold slope, DIBL, transconductance etc.

Index Terms*— Cylindrical Surround Gate MOSFETs, Surface Potential, TCAD, Short Channel Effects, Analog.

I. INTRODUCTION

SOI has been in use by many leading manufacturers in the last decade due to the reasons it provide higher density, no substrate leakage current, resistance to latch-up, higher speed, reduced parasitic capacitance and thereby improving performance[1]. But these devices suffer from the hot electron effect which increases the gate leakage current. Due to the scaling of the channel length, short channel effects (SCEs) such as the threshold voltage roll off due to charge sharing between drain/source and channel, Drain Induced Barrier Lowering (DIBL) due to the variation of the source/channel barrier by the drain voltage and hence an increase in the OFF state leakage current. Therefore reduction of hot electron and short channel effects plays major role in scaling the SOI MOS devices. There have been many possible solutions proposed in the literature [2-6]. To reduce the hot electron and short channel effects double metal and triple metal double gate MOSFETs, have been proposed. There are a large number of papers available dealing with the double metal and triple metal double gate MOSFETs [8-12] but the advantages of triple metal cylindrical MOSFETs are yet to be explored fully.

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In this paper we have proposed physics based surface potential model for TMCSG [14-17] by solving the 2-D Poisson's equation [3, 7] in cylindrical coordinates. The symmetric behavior of cylindrical channel along with the continuity equations has been taken into considerations for the derivation of the model. This model is verified with the potential extracted from the Sentaurus TCAD's [13] device simulator.

II. MODELING OF TMCSG MOSFETs

To have simple model we have neglected the presence of interface charge. The device under consideration is having the channel length and diameter such that the quantum mechanical effects are also negligible. If the channel is doped uniformly with p-type($N_A\ \mathrm{cm}^{-3}$) impurity. Then, the 2D poisons equation in the cylindrical coordinates is given by

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial(\phi(r,z))}{\partial r}\right)+\frac{\partial^2(\phi(r,z))}{\partial z^2}=\frac{qN_A}{\varepsilon_{Si}} \quad (1)$$

Where $\phi(r,z)$ is the potential in the channel and ε_{Si} is the permittivity of silicon, q is the unit charge in coulombs. Let us assume parabolic potential profile in the vertical direction of the channel.

$$\phi(r,z)=c_1(z)+c_2(z)r+c_3(z)r^2 \quad (2)$$

Where $c_1(z)$, $c_2(z)$ and $c_3(z)$ are constants to be determined. For the calculation of the above constants following boundary conditions are considered.

1. Surface potential is a function of z only.

$$\phi(R,z)=\phi_S(z) \quad (3)$$

Where $r=R$ is the radius of the cylindrical channel.

2. The electric field in the center of the silicon pillar is zero by symmetry.

$$\left.\frac{\partial\phi(r,z)}{\partial r}\right|_{r=0}=0 \quad (4)$$

3. The electric field at $r=R$ (i.e. silicon-oxide interface) is continuous.

$$\left.\frac{\partial\phi(r,z)}{\partial r}\right|_{r=R}=\frac{C_f}{\varepsilon_{Si}}\left[V_{GS}-\phi_s(z)-V_{FB}\right] \quad (5)$$

Where $C_f=\varepsilon_{ox}\Big/R\ln\left(1+\frac{t_{ox}}{R}\right)$, t_{ox} is thickness and ε_{ox} is the permittivity of the silicon dioxide respectively.

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4. The electric field at the source end is

$$\phi(0,0)=\phi_s(0)=V_{bi} \quad (6)$$

Where V_{bi} is the built in potential of source-channel junction.

5. Potential at the drain end is

$$\phi(L_1+L_2+L_3,0)=\phi_s(L)=V_{bi}+V_{ds} \quad (7)$$

Where L_1, L_2, L_3 are the lengths of M_1, M_2 and M_3 respectively.

Solving (3) – (5) constants $c_1(z)$, $c_2(z)$ and $c_3(z)$ are found as:-

$$c_1(z)=\phi_S(z)\left[1+\frac{C_f R}{2\varepsilon_{Si}}\right]-\frac{C_f R}{2\varepsilon_{Si}}\left[V_{GS}-V_{FB}\right]$$

$$c_2(z)=0$$

$$c_3(z)=\frac{C_f}{2R\varepsilon_{Si}}\left[V_{GS}-\phi_s(z)-V_{FB}\right]$$

Therefore, the 2-D potential in the cylindrical channel is

$$\phi(r,z)=\phi_S(z)\left[1+\frac{C_f R}{2\varepsilon_{Si}}\right]-\frac{C_f R}{2\varepsilon_{Si}}\left[V_{GS}-V_{FB}\right]+\frac{C_f}{2R\varepsilon_{Si}}\left[V_{GS}-\phi_s(z)-V_{FB}\right]r^2 \quad (8)$$

Substituting this value of $\phi(r,z)$ into Poisson's equation (1) , We get:-

$$\frac{d^2\phi_S(z)}{dz^2}-\lambda^2\phi_S(z)=\beta \quad (9)$$

Where $\lambda^2=2C_f/\varepsilon_{Si}R$ and $\beta=qN_A/\varepsilon_{Si}-\lambda^2(V_{GS}-V_{FB})$, V_{FB} is the flat band voltage, V_{GS} is the applied gate to source potential.

In conventional Surround Gate (SG) MOSFET, the gate is made of only one material, but in the triple metal cylindrical surround gate (TMCSG) MOSFET structure, we have three gates with different work functions and doping densities under them. The middle gate has the higher workfunction than the other two side gates. Applying (9) to this device, we get

$$\frac{d^2\phi_{S1}(z)}{dz^2}-\lambda^2\phi_{S1}(z)=\beta_1 \quad \text{for } 0\le z\le L_1 \quad (10)$$

$$\frac{d^2\phi_{S2}(z)}{dz^2}-\lambda^2\phi_{S2}(z)=\beta_2 \quad \text{for } L_1\le z\le L_1+L_2 \quad (11)$$

$$\frac{d^2\phi_{S3}(z)}{dz^2}-\lambda^2\phi_{S3}(z)=\beta_3 \quad \text{for } L_1+L_2\le z\le L_1+L_2+L_3 \quad (12)$$

Where $\phi_{S1}(z)$ and $\phi_{S3}(z)$ are the surface potentials under the side gates (M_1 and M_3) on source and drain side respectively, and $\phi_{S2}(z)$ is the surface potential under the main gate (M_2). Solving (10), (11) and (12), we obtain the surface potential for each section as follows-

$$\phi_{S1}(z)=Ae^{\lambda z}+Be^{-\lambda z}-\frac{\beta_1}{\lambda^2} \quad (13)$$

$$\phi_{S2}(z)=Ce^{\lambda z}+De^{-\lambda z}-\frac{\beta_2}{\lambda^2} \quad (14)$$

$$\phi_{S3}(z)=Ee^{\lambda z}+Fe^{-\lambda z}-\frac{\beta_3}{\lambda^2} \quad (15)$$

Solving for A, B, C, D and E, we get:-

The potential at source side

$$\phi_{S1}(z)\big|_{z=0}=V_{bi} \quad (16)$$

The potential at the drain side

$$\phi_{S3}(z)\big|_{z=L_1+L_2+L_3}=V_{bi}+V_{ds} \quad (17)$$

The potential at the interface of two adjacent gates is continuous.

$$\phi_{S1}(z)\big|_{z=L_1}=\phi_{S2}(z)\big|_{z=L_1} \quad (18)$$

$$\phi_{S2}(z)\big|_{z=L_1+L_2}=\phi_{S3}(z)\big|_{z=L_1+L_2} \quad (19)$$

The electric field at the interface of two adjacent gates is continuous.

$$\left.\frac{d\phi_{S1}(z)}{dz}\right|_{z=L_1}=\left.\frac{d\phi_{S2}(z)}{dz}\right|_{z=L_1} \quad (20)$$

$$\left.\frac{d\phi_{S2}(z)}{dz}\right|_{z=L_1+L_2}=\left.\frac{d\phi_{S3}(z)}{dz}\right|_{z=L_1+L_2} \quad (21)$$

Solving above equations we get

$$A+B=V_{bi}+\frac{\beta_1}{\lambda^2} \quad (22)$$

$$Ee^{\lambda(L_1+L_2+L_3)}+Fe^{-\lambda(L_1+L_2+L_3)}=V_{bi}+V_{ds}+\frac{\beta_3}{\lambda^2} \quad (23)$$

$$Ae^{\lambda L_1}+Be^{-\lambda L_1}-Ce^{\lambda L_1}-De^{-\lambda L_1}=\frac{\beta_1}{\lambda^2}-\frac{\beta_2}{\lambda^2} \quad (24)$$

$$Ce^{\lambda(L_1+L_2)}+De^{-\lambda(L_1+L_2)}-Ee^{\lambda(L_1+L_2)}-Fe^{-\lambda(L_1+L_2)}=\frac{\beta_2}{\lambda^2}-\frac{\beta_3}{\lambda^2} \quad (25)$$

$$Ae^{\lambda L_1}-Be^{-\lambda L_1}-Ce^{\lambda L_1}+De^{-\lambda L_1}=0 \quad (26)$$

$$Ce^{\lambda(L_1+L_2)}-De^{-\lambda(L_1+L_2)}-Ee^{\lambda(L_1+L_2)}+Fe^{-\lambda(L_1+L_2)}=0 \quad (27)$$

On solving the above equations we get the constants A, B, C, D, E and F as follows-

$$C=\frac{\delta_1-\delta_2 q}{p-rq} \quad (28)$$

$$D=\delta_2-Cr \quad (29)$$

$$A=\left(\frac{\beta_1-\beta_2}{2\lambda^2}+C\right)\exp(-\lambda L_1) \quad (30)$$

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$$B = \left(V_{bi} + \frac{\beta_1}{\lambda^2} \right) - A \quad (31)$$

$$E = C \exp(\lambda L_2) - \frac{\beta_2 - \beta_3}{2\lambda^2} \quad (32)$$

$$F = \left(V_{bi} + V_{ds} + \frac{\beta_3}{\lambda^2} \right) - E \exp(2\lambda L_3) \quad (33)$$

Where $p = \exp(\lambda(L_2 + L_3))$,

$q = \exp(-\lambda(L_2 + L_3))$,

$$\delta_1 = \left(V_{bi} + V_{ds} + \frac{\beta_3}{\lambda^2} \right) + \frac{(\beta_2 - \beta_3)\cosh(\lambda L_3)}{\lambda^2}$$

$r = \exp(-2\lambda L_1)$, and

$$\delta_2 = \left(V_{bi} + \frac{\beta_1}{\lambda^2} \right) - \frac{(\beta_1 - \beta_2)\cosh(\lambda L_1)}{\lambda^2} \exp(-\lambda L_1)$$

Minimum surface potential $(\phi_{S\min})$ of the silicon cylinder will be under the gate having the highest work function. So, $\phi_{S\min}$ lies under the main gate (M_2) being the highest work function metal in our structure. Hence $\phi_{S\min}$ is calculated from (14) as:-

$$\phi_{S\min} = 2\sqrt{CD} - \frac{\beta_2}{\lambda^2} \quad (34)$$

And the minimum potential occurs at

$$z_{\min} = \frac{1}{2\lambda} \ln\left(\frac{D}{C} \right) \quad (35)$$

The threshold voltage is defined as the value of V_{GS} at which the minimum surface potential $\phi_{S2,\min}$ equals $2\phi_F$. Hence we can determine the value of the threshold voltage as the value of V_{GS} by solving (34).

III. DEVICE FOR TCAD SIMULATION

The three dimensional view of the structure used for the TCAD simulation along with the device parameters and mesh is shown in Fig.1. The structure has been generated using the Sentaurus Structure Editor (SentaurusSE) of Sentaurus TCAD [13]. The extremely shallow source/drain regions are realized using triple gate structure which reduces the source drain extension resistance. Here we have taken the main and side gate lengths of source side and drain side (L_1 and L_3 respectively) to be equal to 50 nm each, since it has been found that this configuration offers the optimum results. The main gate and side gate work functions have been chosen to be Gold (4.8 eV) and Titanium (4.33 eV) respectively. To obtain the extremely shallow junctions under the side gate regions the work function of the side gates have been chosen to be lower than the main gate work function. The gate silicon di-oxide thickness has been taken to be 2 nm. Since decreasing the gate oxide below this increases the gate tunneling current. The source and drain are doped with a concentration of $5\times10^{19}\ cm^{-3}$ (n-type, Arsenic). The diameter of the silicon pillar (channel region) used for our simulations has been taken to be 20 nm. The channel is uniformly doped with a concentration of $1\times10^{16}\ cm^{-3}$ (p-type, Boron). The channel is lightly doped so as not to degrade the carrier mobility. The meshing has been done using simple mesh to have better convergence.

In section V the triple metal Cylindrical surround gate MOSFET has been characterized for the different operating voltages. For this purpose a 2D structure has been simulated with the above mentioned parameters. In the latter part of the section the effect of doping in TMCSG has been explored. For this the transconductance (g_m), gate voltage for maximum transconductance $(v_{g,gm})$, drain induced barrier lowering (DIBL) and subthreshold slope (SS) has been extracted for different channel doping.

IV. MODEL VERIFICATION

Figure 2 shows the extracted surface potential of TMCSG MOSFET for different VDS values keeping VGS=0.0 V. It can be observed from the figure that the potential under the main gate M2 is unchanged due to the change in VDS. It clearly shows the advantage of the structure to overcome the SCEs.

Figure 3 compares the surface potential predicted by our model with that extracted from the 3D-device simulations. Here the gate voltage has been kept constant to VGS=0.0 V and the VDS has been varied from 0.0 V to 1.5 V. This is evident from the plot that the model is in good agreement with the simulation results.

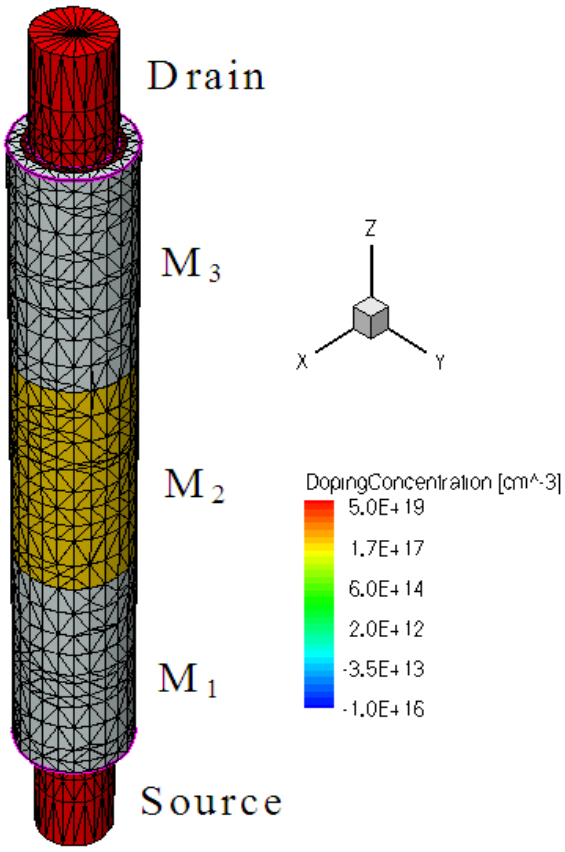

Figure 1. Three dimensional view of the triple metal cylindrical surrounding gate MOSFET with meshing and doping concentrations. The gate M_2 is made of Gold (Workfunction 4.9 eV) and M_1, M_3 is made of Titanium (Workfunction 4.7 eV)

V. 2D SIMULATION OF THE TM-CSG MOSFET

Further we simulated the TMCSG MOSFET for the better understanding of various device parameters. In this section we discuss about the variation of different physical parameters along the channel which are important for understanding the device working.

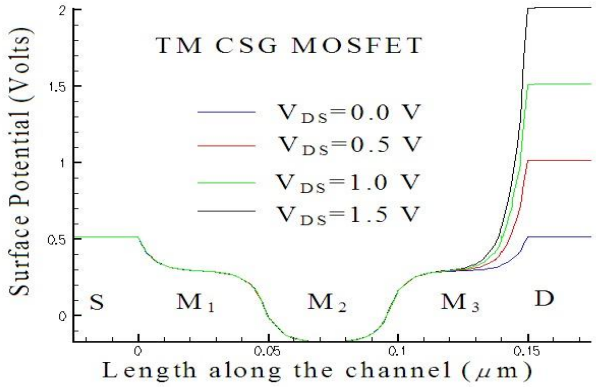

Figure 2 Surface potential variation as extracted from the TCAD simulation for the Triple metal cylindrical surround gate MOSFET for different values of V_{DS} and V_{GS}=0.0 V.

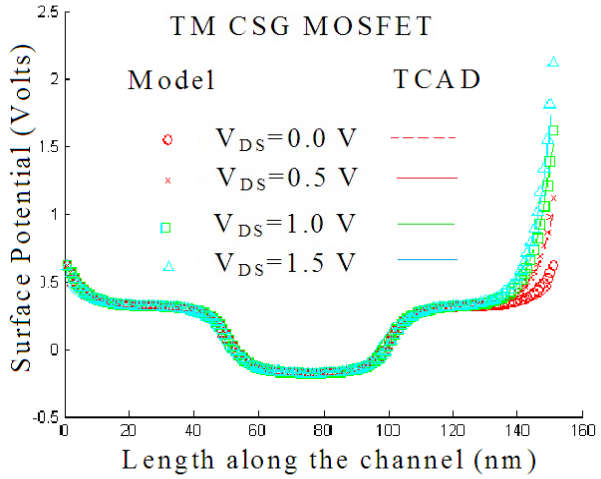

Figure 3 Surface potential as predicted by our model and that obtained from the simulation of the TMCSG MOSFET. The length of M1, M2 and M3 are 50nm each. Source and Drain are doped with $5\times10^{19}\ cm^{-3}$ (n-type, Arsenic) and channel is doped with $1\times10^{16}\ cm^{-3}$ (p-type, Boron).

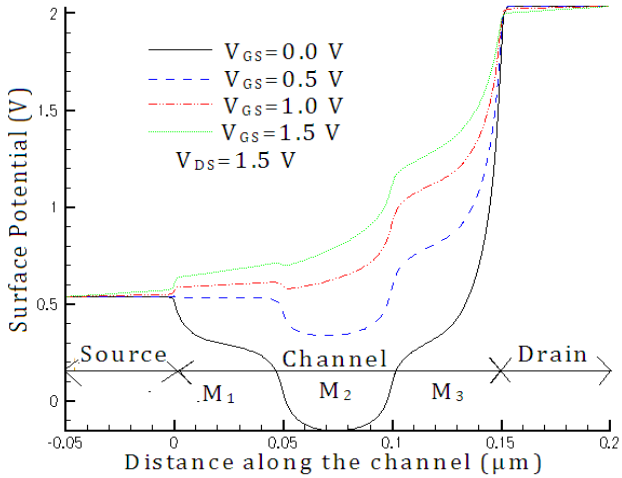

Figure 4 Surface potential variation for constant VDS=1.5 V and different values of VGS.

Figure 4 shows the variation of surface potential for fixed V_{DS}=1.5 V and different values of V_{GS}. The potential under the metal M_1, M_2, and M_3 changes as the gate voltage increases from 0 to 1.5 V.

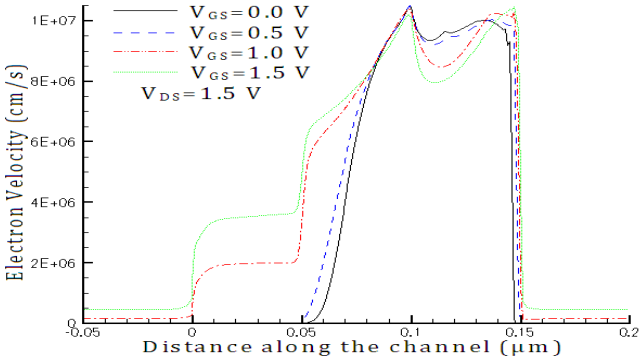

Figure 5 Electron velocity at the at the surface along the channel for constant VDS=1.5 V and different values of VGS

Figure 5 shows the variation of electron velocity along the channel. It can be observed that the velocity of electron near the drain (under M_3) does not changes much as compared to V_{GS}=0 V and V_{GS}=1.5 V whereas the injection velocity near the source of the electrons (under the M_1) has improved a lot.

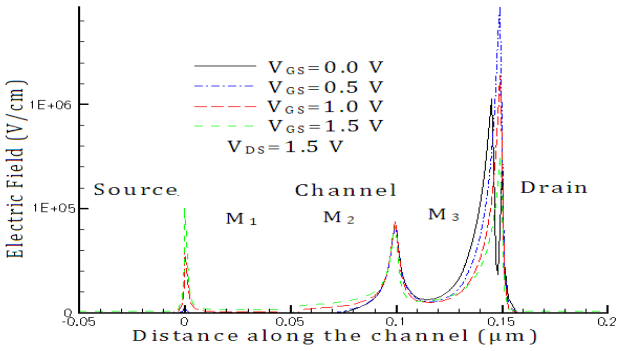

Figure 6 Electric field at the SiO2/Si interface along the channel for constant VDS=1.5 V and different values of VGS

Figure 6 shows the electric field along the channel and Fig. 7 shows the distribution of surface electron density under the gate metals M_1, M_2 and M_3.

Figure 8 and 9 shows the electron and hole mobility respectively. It can be observed that the electron mobility is large under the metal M_1 as compared to the metal M_3. The hole mobility under the metal M_2 is smaller as compared to the gate metals M_1 and M_3.

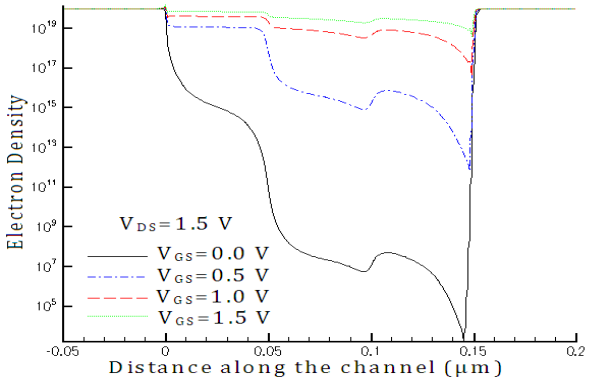

Figure 7 Electron density at the surface along the channel for constant VDS=1.5 V and different values of VGS

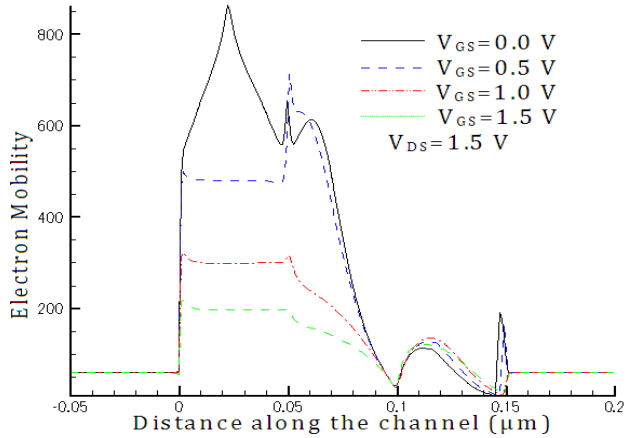

Figure 8 Electron mobility at the surface along the channel for constant VDS=1.5 V and different values of VGS

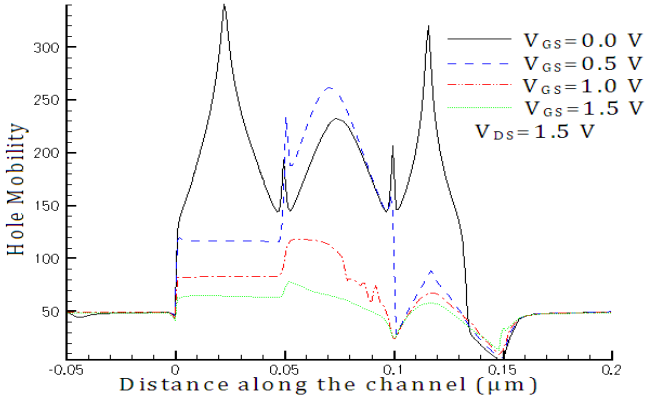

Figure 9 Hole mobility at the surface along the channel for constant VDS=1.5 V and different values of VGS

Hole velocity (Fig. 10) is highest near the drain side under the gate metal M_3 whereas it is lowest near the source side (under metal gate M_1).

In the Fig. 12 it can be observed that the electric field throughout the channel is almost uniform for the case V_{GS}=1.5 V and V_{DS}=1.5 V. The electron density (Fig. 13) is largest near the source region whereas it is lowest near the drain side. In the center of the channel the electron density is lower as compared to other regions.

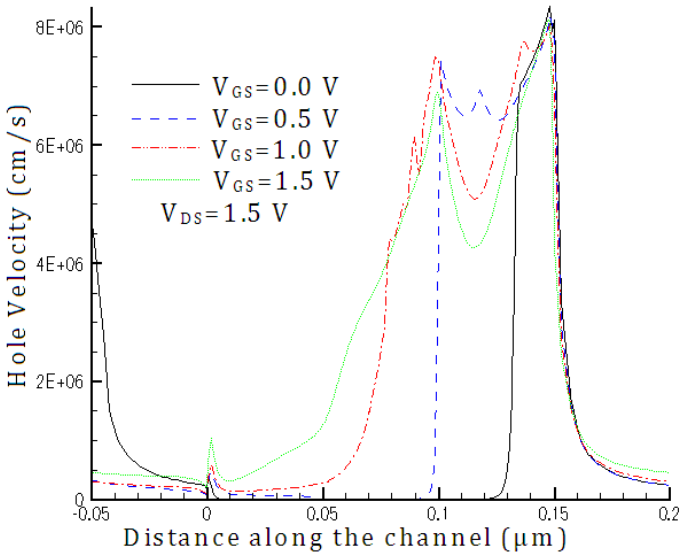

Figure 10 Hole velocity at the SiO2/Si interface along the channel for constant VDS=1.5 V and different values of VGS

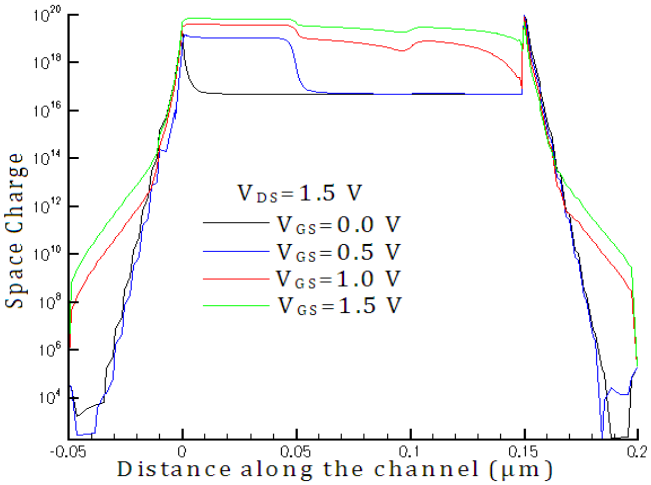

Figure 11 Distribution of surface space charge along the channel

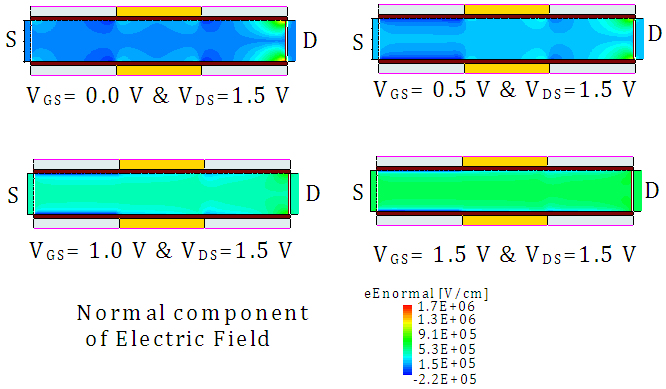

Figure 12 Electric field (normal component-vertical to the current flow direction) variation through the channel (cross-sectional view) for different values of VGS and VDS

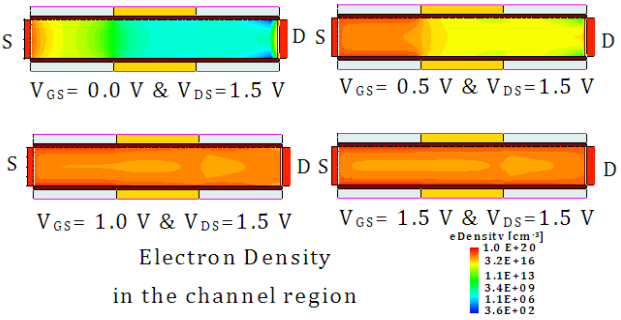

Figure 13 Electron density variation through the channel (cross-sectional view) for different values of VGS and VDS

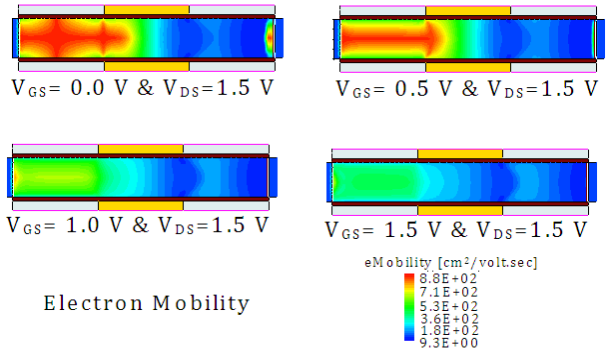

Figure 14 Electron mobility variation through the channel (cross-sectional view) for different values of VGS and VDS

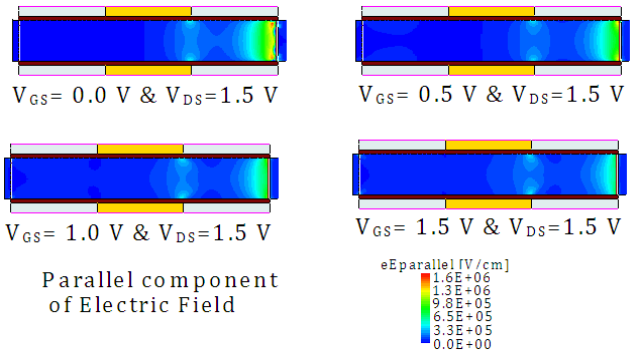

Figure 15 Electric field variation through the channel (cross-sectional view) for different values of VGS and VDS

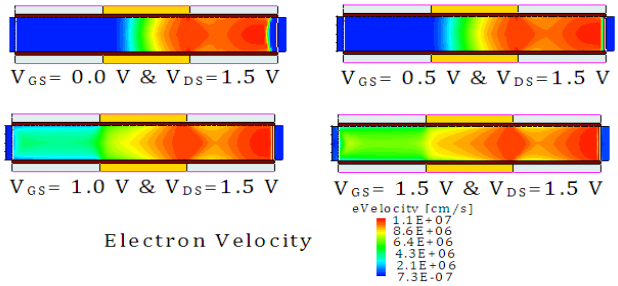

Figure 16 Electron velocity variation through the channel (cross-sectional view) for different values of VGS and VDS

Electron mobility (Fig. 14) is highest near the source side in the middle of the channel and is lowest near the drain side. As the gate voltage is increased the mobility is lowered due to increase in the perpendicular component of the electric field (Fig. 15) and increased electron scattering.

Figure 16 and 17 shows the variation of the electron and hole velocity through the channel respectively. As can be observed that the electron (hole) velocity is largest under M_3 and in the middle of channel (volume inversion). Due to this there is less surface scattering happening and the electron mobility is enhanced at the surfacel.

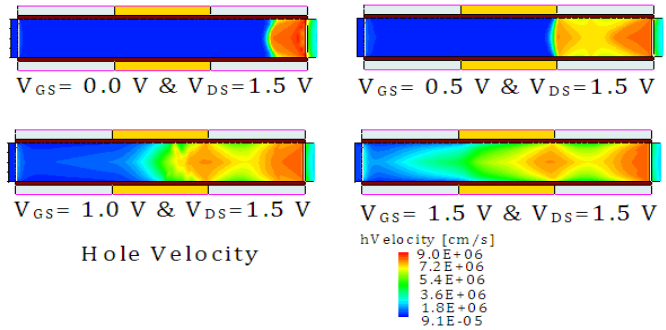

Figure 17 Hole velocity variation through the channel (cross-sectional view) for different values of VGS and VDS

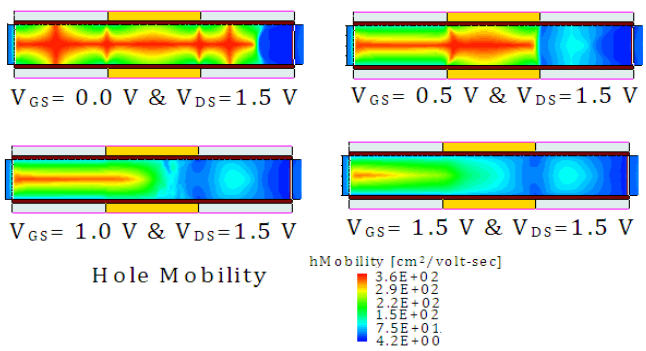

Figure 18 Hole mobility variation through the channel (cross-sectional view) for different values of VGS and VDS

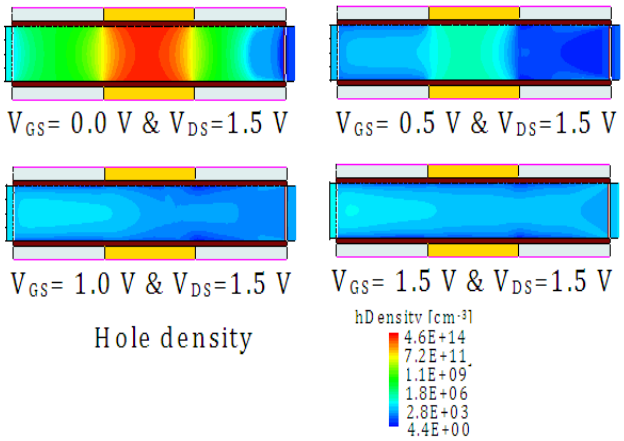

Figure 19 Hole density variation through the channel (cross-sectional view) for different values of VGS and VDS

Figure 18 shows the hole mobility variations. It can be observed from the figure that the hole mobility is large in the middle of the channel near the source side. Hole density variations are shown in the Fig. 19. The hole density can be seen to be decreasing with the increase of gate potential due to the formation of inversion layer.

The TMCSG MOSFET is now investigated for the effect of channel doping. The transconductance (g_m), gate voltage for maximum transconductance $(v_{g,gm})$, drain induced barrier lowering (DIBL) and subthreshold slope (SS) has been extracted to see the effect of doping on SCE and analog performance.

The transconductance is defined as

$$g_m = \frac{dI_D}{dV_G} \tag{36}$$

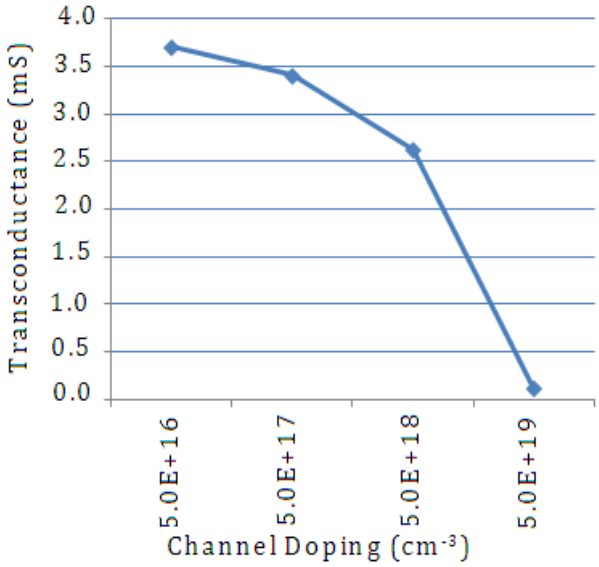

Figure 20 Variation of transconductance w.r.t. the channel doping

From the Fig. 20 it can be observed that the maximum transconductance decreases as the channel doping in TMCSG is increased.

This strengths the fact to use the lightly doped channels. The maximum value of transconductance occurs at relatively lower gate voltage for lightly doped channels.

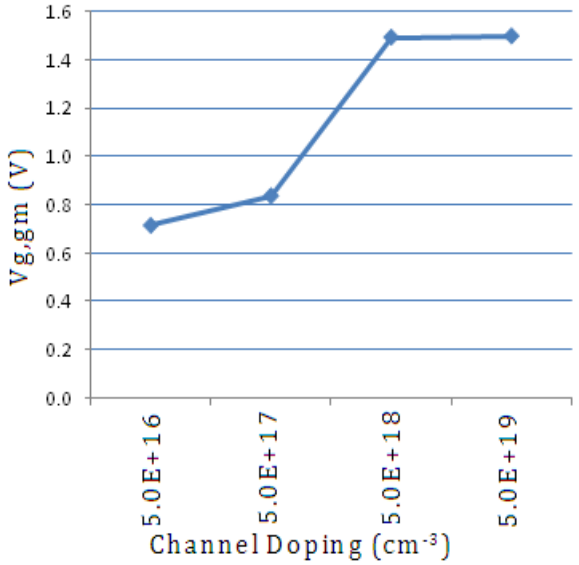

Figure 21 Variation of Vg,gm w.r.t. the channel doping

$V_{g,gm}$ is the gate voltage at which the maximum transconductance is obtained. Figure 21 shows the variation of $V_{g,gm}$ as a function of channel doping. As can be observed, the maximum transconductance is obtained at relatively lower gate voltage for lower channel doping. Hence, this may be used for low voltage applications.

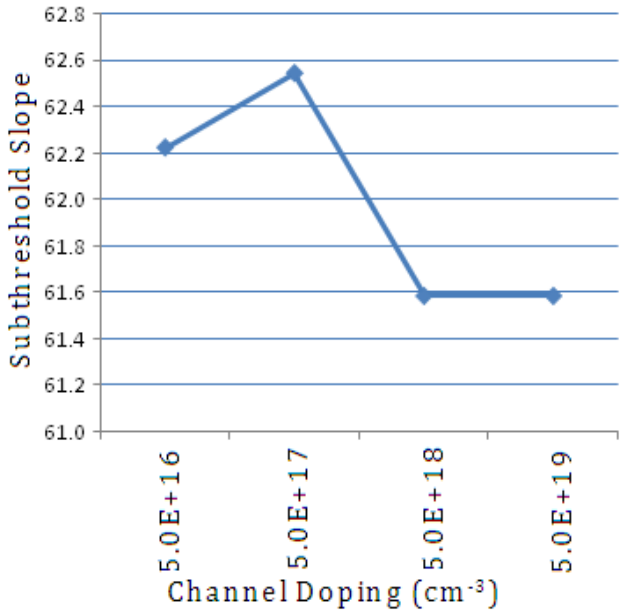

Figure 22 Subthreshold slope variation w.r.t. the channel doping

The Subthreshold Slope (SS) is defined as the inverse of required gate voltage for per decade increment in drain current.

$$SS = \frac{dV_G}{d\log(I_D)} \tag{37}$$

Subthreshold slope seems to be lower at higher channel dopings but other characteristics (e.g. mobility etc.) deteriotes at such higher dopings hence even for better SS it is not preferred.

The Drain Induced Barrier Lowering (DIBL) is defined as the change in threshold voltage due to the change in drain voltage. Generally the drain voltages chosen are 0.05 – 0.1 V (V2) and 1.0 to 1.5 V (V1).

$$DIBL = \frac{V_{TH}\big|_{V_{DS}=V_1} - V_{TH}\big|_{V_{DS}=V_2}}{(V_2 - V_1)} \tag{38}$$

Figure 23 shows the Drain induced barrier lowering (DIBL) for the TMCSG.

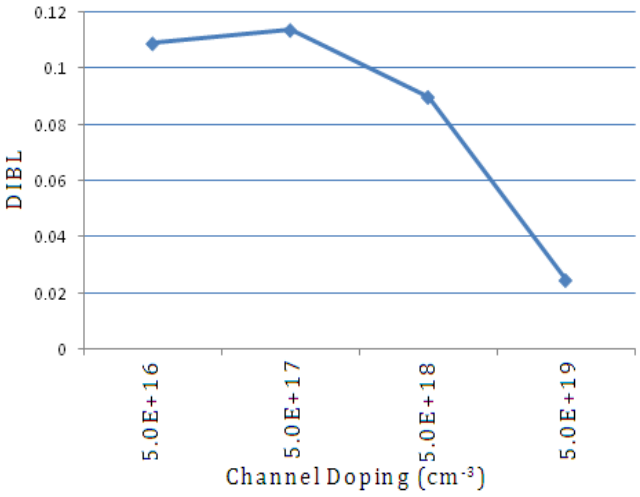

Figure 23 DIBL variation w.r.t. the channel doping

VI. CONCLUSION

A physics based surface potential model for the novel triple metal cylindrical surround gate MOSFET was derived and found to be in good agreement with the TCAD simulation results of the TMCSG. This device has also shown to reduce the SCEs which mean these can be a potential candidate to substitute the conventional MOSFETs due to aggressive scaling. We have also observed that the maximum value of transconductance occurs at relatively lower gate potential which encourages this device to be used for low voltage applications as well. The channel doping optimizations shows that lightly doped TMCSG may be a potential candidate for better analog performance at lower operating voltages simultaneously giving better immunity to the SCEs.

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