Back-Gate Biasing of the DG Transistors

Soumen Biswas, Sarosij Adak

Abstract*—DG-MOSFET programmable logic circuits have noteworthy features such as the ease of re-programming techniques and fewer transistors used in an IC package. Dynamic and reconfigurable threshold logic gates based on DG-MOSFETs are explored. Multiple functions are obtained on a single Boolean static logic circuit built with DG-MOSFETs. Our proposed work is to reconfigurable static and dynamic Boolean logic gates, as well as threshold logic gates designed with DG-MOSFETs. For reconfiguration in these circuits, a systematic back-gate biasing approach is utilized.

***Index Terms*—CMOS integrated circuits, double-gate (DG) transistors, logic circuits,**

I. INTRODUCTION

Reconfigurable architectures are of great interest to system designers because they offer a way of achieving power and performance efficiency by matching specific algorithmic constructs with an appropriate architecture [1]. The reduced fan-out, power handling capacity, gain, and reliability of deep-submicrometer (DSM) and nanoscale devices will have a number of consequences for reconfigurable systems. The double-gate (DG) transistor is a promising device applicable to DSM due in particular to its inherent resistance to short-channel effects and potentially ideal subthreshold performance. Typically, the two gates would be operated together as this offers the best switching performance. However, accessing the two gates separately creates opportunities for innovative circuit design [10].In the final stretch of the CMOS downscaling trend, projected to reach the 22-nm limit by 2010 [1], double-gate (DG) MOSFET architectures on system-on-insulator (SOI) substrates are expected to replace the traditional bulk device structures [2], [3]. While multi-gate SOI structures are idealfor digital performance, they will be also strong contenders for analogue RF applications in lucrative wireless communications market due to their ability to effectively handle gigahertz modulation, to minimize parasitics via low-loss substrate and to cross-modulate double gates through thin silicon body. However, the actual potential of DG-MOSFETs have not been assessed in detail and there is a clear gap in the literature with regards to analog circuit applications [4]. Hence, it is imperative to explore this gap, surveying and exploiting unique features of DG-MOSFETs especially for specific RF signal processing tasks [5], [6].

Manuscript received on April 26, 2012.

Soumen Biswas, Department of Electronics and Communication Engineering, Institute Of Engineering and Management, Kolkata, India, +91-8100894340, (e-mail: phoenix.soumen@gmail.com).

Sarosij Adak, Department of Electronics and Communication Engineering, Dream Institute of Technology, Kolkata, India, +91-8900449166, (e-mail: sarosij_adak@rediffmail.com).

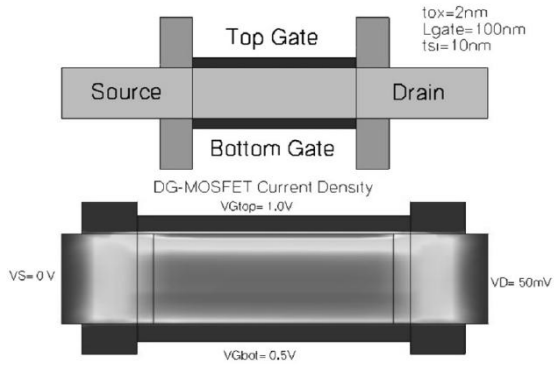

Fig. 1: DG-MOSFET device structure (top) used in this work has the gate length L = 100 nm, body thickness tsi= 10 nm, and oxide thickness tox = 2 nm, which reflect typical values for digital applications. DESSIS device simulator is used in the mixed-mode simulation mode [13] and drift–diffusion approximation is employed to reduce the computational cost. Current density distribution at an asymmetric bias condition is shown above, where the top channel is fully switched on.

A particularly attractive possibility for analog circuit applications is the tunability of DG-MOSFETs' front-gate functionality via bottom (back) gate bias [7], [8]. This has a number of important implications for circuit design: 1) increased functionality out of a given set of devices; 2) reduction of parasitics and layout area; 3) higher speed operation and lower power consumption with respect to equivalent conventional circuits. Although several works that utilizes DG-MOSFETs in RF mixing applications have been published so far [7]–[9], the tunability of the DG-MOSFETs have been largely ignored by the analog designers. Most of DG-MOSFETs [10], [11] concentrate on the individual device figures of merit such as gm/Id characteristics, power [10] and cutoff frequency [11] and linearity [5], showing its superiority in terms for low power, speed, and signal integrity. In this brief, however, we focus on the circuit applications, exploring simple analog circuit blocks built using DG-MOSFETs, in which bottom gate are used to tune the circuit performance.

II. BACK GATE BIAS METHOD

A. Threshold Voltage

The threshold voltage, commonly abbreviated as Vth, of a MOSFET is usually defined as the gate voltage where an inversion layer forms at the interface between the insulating layer (oxide) and the substrate (body) of the transistor. The formation of the inversion layer allows the flow of electrons through the gate-source junction. The creation of this layer is described next.

Published By:
Blue Eyes Intelligence Engineering
& Sciences Publication

In an n-MOSFET the substrate of the transistor is composed of p-type silicon, which has positively charged mobile holes as carriers. When a positive voltage is applied on the gate, an electric field causes the holes to be repelled from the interface, creating a depletion region containing immobile negatively charged acceptor ions. A further increase in the gate voltage eventually causes electrons to appear at the interface, in what is called an inversion layer, or channel. Historically the gate voltage at which the electron density at the interface is the same as the hole density in the neutral bulk material is called the threshold voltage. Practically speaking the threshold voltage is the voltage at which there are sufficient electrons in the inversion layer to make a low resistance conducting path between the MOSFET source and drain.

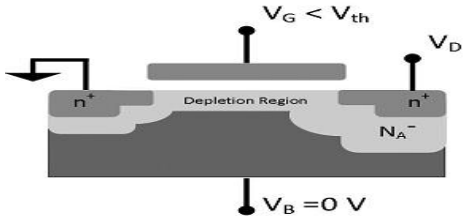

Fig. 2: Depletion region of an nMOSFET biased below threshold.

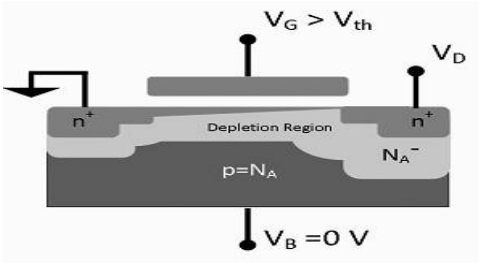

Fig. 3: Depletion region of an nMOSFET biased above threshold with channel formed.

In the figures, the source (left side) and drain (right side) are labeled n+ to indicate heavily doped (blue) n-regions. The depletion layer dopant is labeled NA− to indicate that the ions in the (pink) depletion layer are negatively charged and there are very few holes. In the (red) bulk the number of holes p = NA making the bulk charge neutral. If the gate voltage is below the threshold voltage (fig. 2), the transistor is turned off and ideally there is no current from the drain to the source of the transistor. In fact, there is a current even for gate biases below threshold (sub-threshold leakage) current, although it is small and varies exponentially with gate bias.If the gate voltage is above the threshold voltage (fig. 3), the transistor is turned on, due to there being many electrons in the channel at the oxide-silicon interface, creating a low-resistance channel where charge can flow from drain to source. For voltages significantly above threshold, this situation is called strong inversion. The channel is tapered when VD > 0 because the voltage drop due to the current in the resistive channel reduces the oxide field supporting the channel as the drain is approached. In modern devices the threshold voltage is a much less clear-cut parameter subject to variation with the biases applied to the device.

B. Body Effect

The body effect describes the changes in the threshold voltage by the change in V_{SB}, the source-bulk voltage. Since the body influences the threshold voltage (when it is not tied to the source), it can be thought of as a second gate, and is sometimes referred to as the "back gate"; the body effect is sometimes called the "back-gate effect".

C. Principle of the method

The following is the design equation of threshold voltage V_T of a MOSFET in CMOS circuits:

$$V_T = V_{T0} \pm \gamma\left(\sqrt{|-2\phi_F + V_b|} - \sqrt{2|\phi_F|}\right), \quad (1)$$

where VT0 is the zero-biased threshold voltage, c is the body-effect coefficient, Vb is the back-gate bias, and 2| Φ/F| is the surface potential. The increase or decrease in VT depends on the magnitude of Vb ± reverse or forward biased. In dc voltage transfer characteristics of a CMOS inverter, the transition region adjustment at the midway between the high- and low-logic levels depends primarily on the W/L ratios of n- and p-channel MOSFETs. A better control of the transition region can be obtained by electrically adjusting the threshold voltage of MOSFETs since the turn-on and turn-off points on voltage transfer characteristics depend on the threshold voltage of MOSFETs. The back-gate bias could be used more effectively in the design of ternary logic circuits, where an additional design parameter is needed [12]. Three types of ternary operators are defined by [11].

$$\overline{X}_C = \begin{cases} C & \text{if } X = 1, \\ 2 - X & \text{if } X \neq 1. \end{cases} \quad (2)$$

C in Eq. (2) takes the value of logic 2 for PTI, logic 1 for STI and logic 0 for NTI which corresponds to higher (1), middle (0) and lower levels (1), respectively. Figs. 4-6 show the schematics of STI, PTI and NTI, respectively. In Fig. 1, for STI, a CMOS transmission gate is connected to the common drain output of a CMOS inverter. In Fig. 5, for PTI, a p-MOSFET is connected to the output of a CMOS inverter. In Fig. 6 for NTI, an n- MOSFET is connected to the output of a CMOS inverter. The substrate bias connection in MOSFETs of the CMOS inverter is used to apply forward or reverse bias voltage, Vb, for the control of threshold voltage according to Eq. (1) and to adjust the transition region in dc voltage transfer characteristics.

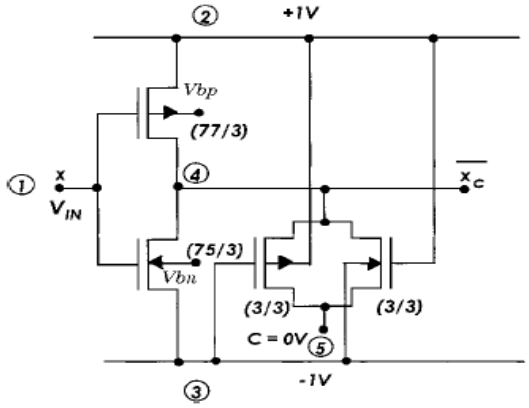

Fig. 4: Simple ternary inverter

Published By:
Blue Eyes Intelligence Engineering
& Sciences Publication

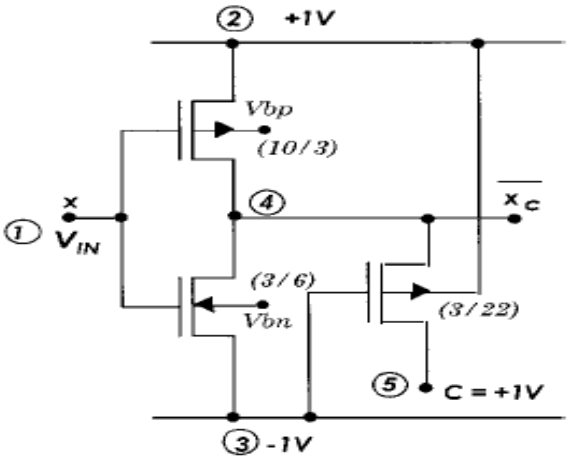

Fig. 5: Positive ternary inverter

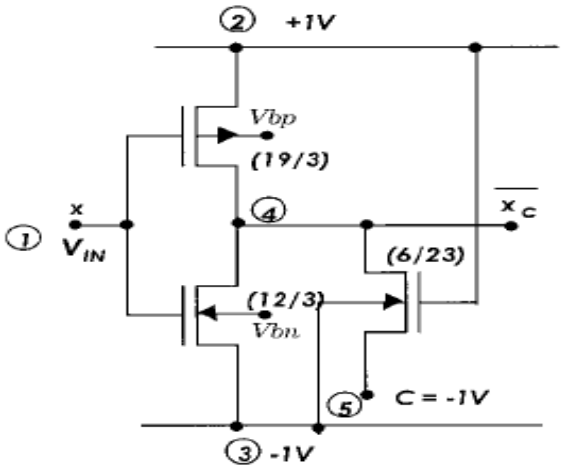

Fig. 6: Negative ternary inverter

The circuit diagrams in Figs. 4-6 for STI, PTI and NTI, respectively, can be implemented in standard dual well CMOS processes using the p-substrate. These wells can be held either at the same potential or at different potentials. Thus, the use of a standard dual well CMOS process would allow us to apply different back-gate biases in MOSFETs of ternary logic circuits. This would also eliminate the problem of the p-substrate becoming common for all n-MOSFETs in a typical n-well CMOS process. Part of the circuits in Figs. 1-3 uses either a transmission gate or a pass transistor, where the substrate for the p-MOSFET is connected to the most positive potential, and the substrate for the n-MOSFET is connected to the most negative potential.

III. DEVICE STRUCTURE AND MODELING

DG-MOSFETs considered in this work are chosen to facilitate the mixed-mode circuit design methodology, which seeks to integrate analog circuits on the same substrate as digital building blocks with a minimal overhead to the fabrication sequence. This implies using DG-MOSFETs with a minimal body thickness (tsi ≤ nm), oxide insulator thickness (tox ≤ nm) and gate length (L ≤ 100 nm), and the maximum ION/IOFF ratio optimized normally for minimum switching delaypower product [12]. It is also assumed that both gates have been optimized for a symmetrical threshold VT = ±0.25 using a dual-metal process. A generic DG-MOSFET structure based on these design guidelines and in agreement with experimentally demonstrated devices is given in Fig. 7(a). 2-D simulations of this structure are accomplished using

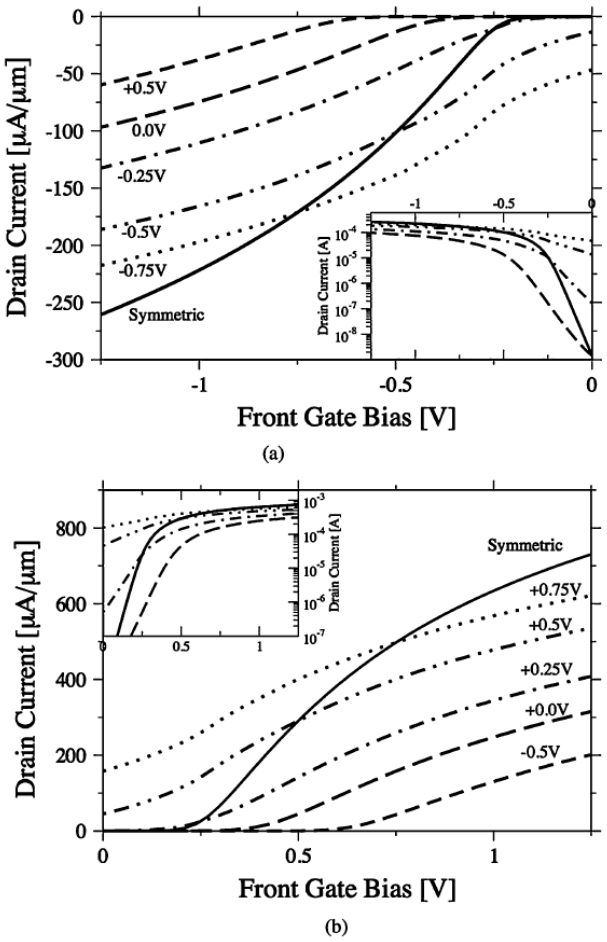

Fig. 7: Simulated characteristics of DG-MOSFETs used in this work. For both the (a) pMOSFET and (b) nMOSFETs, we provide ID − VGtop plots for different back gate bias conditions labelled and VDS = 1.0 V. For comparison symmetric (Vbg = Vfg) drive is also included in the plots. Insets show the same data in semi-log scale, revealing the well-known degredation of subthreshold slope in asymmetrically driven DG-MOSFETs [14].

DESSIS [13] in drift-diffusion approximation for carrier transport, which is sufficient for the low-power circuit-configurations explored here. Fig. 7(b) shows a typical current-density distribution in an asymmetrically biased n-type DG-MOSFET, where the higher bias of top gate induces a more conductive channel.

With the device structure fixed, we can tailor its analog performance by the use of bottom-gate bias. This is best illustrated in Fig. 7(a) and (b), where the drain current through n- and p-type DG-MOSFETs driven from top-gate is studied as a function of the bottom gate bias. While the threshold of individual DG-MOSFETs can be modified using this approach, it must be pointed out that the resulting independently driven devices (IDDGs), [see Fig. 8(a)] are always inferior to symmetrically driven counterparts (SDDGs) in terms of transconductance and subthreshold performance,

under equal geometry and bias conditions [14]. Thus, bottom-gate tunability comes with a reduction in intrinsic DG-MOSFET performance, a price well justified by the variety of circuit possibilities, as explored below. However, in SDDG, and both of them over conventional devices, as recently discussed by Reddy et al. [7]

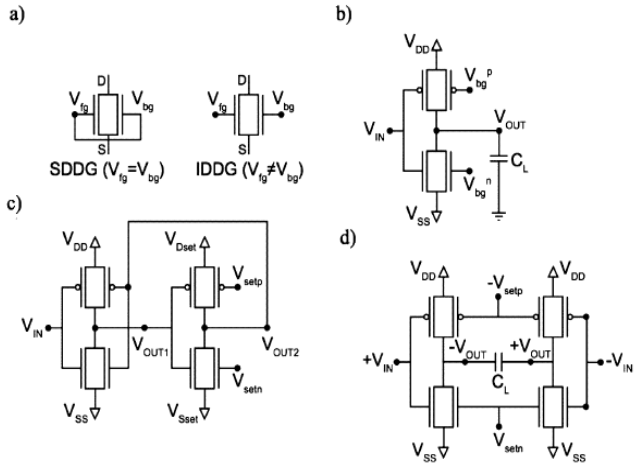

Fig. 8: (a) DG bias conventions SDDG and IDDG refer to symmetrically and
independently driven double-gates, respectively. The main analog circuit blocks considered in this work incorporates (b) a simple CMOS analog amplifier, (c) a Schmitt trigger, and (d) an OTA-C integrator in which various IDDG configurations are employed to tune main performance metrics.

IV. RECONFIGURABLE THRESHOLD LOGIC GATES

Threshold logic gates have been considered the most powerful processing elements exhibiting logic and arithmetic functions. Various research efforts have been conducted through academic and industrial research projects since the concepts of threshold logic were introduced. The threshold logic gates typically used in neural networks are capable of performing a miscellaneous set of functions with primitive ideas of summing and comparing the weighted inputs with a preset reference threshold value. They have been employed in various applications from microprocessors to sensors and field-programmable gate arrays (FPGAs), including commercial products such as MIPS R2010, SUN Sparc V9, CMOS fingerprint sensor, and other experimental chips containing a 64-bit multiplier stage from IBM. However, the impact of threshold logic in industry has been relatively insignificant because the realizations using MOSFETs are not as straightforward as Boolean CMOS logic gates. The DG-MOSFETs grant new possibilities to efficiently realize TLG circuits for reconfigurable logic architectures. In addition to reducing the number of transistors, DG-MOSFETs can also bring novel functionalities to the TLG not only via threshold (T) but also via weights, furthermore expanding its flexibility. The threshold logic gates presented in this thesis include novel circuits with dynamically programmable weights.

V. CIRCUIT ARCHITECTURE OF A VARIABLE WEIGHT THRESHOLD LOGIC GATES

The approach is to build variable-weight threshold logic gates using independent back-gate biasing of DG-MOSFETs [16]. The resulting circuit schematic is given in Fig. 19. Also, the number of transistors in the threshold bank is reduced from using symmetrically driven DG-MOSFETs (SDDG). The new topology and the device sizes are justified for optimal performance, also shown in Fig. 9 .

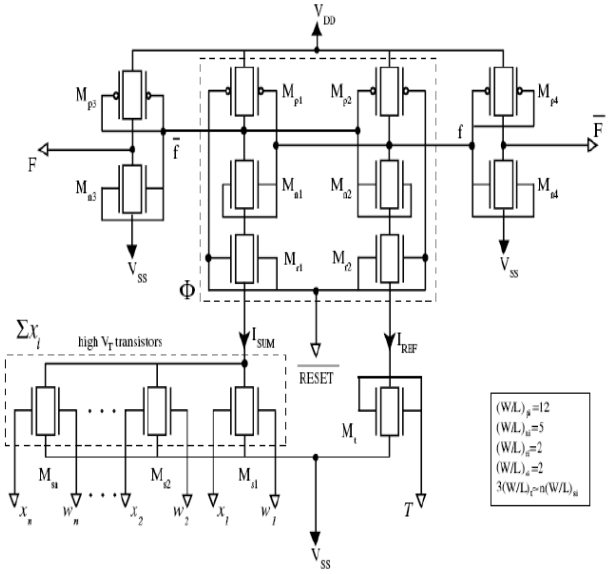

Fig.9: Circuit architecture of a variable weight threshold logic gate [16]

This novel variable weight DG-TLG circuit provides easy access to setting the weights by applying a small analog voltage at back-gates associated with a given voltage. The size of SDDG transistor (Mt) at the threshold-setting bank must be sufficiently large so a single SDDG transistor can generate the required level of reference currents for all cases. Typically, we find that the size of this single threshold setting transistor (Mt) can be as small as a third of the input transistors (Msi), i.e. the ratio of SDDG/IDDG drain currents

at the same bias conditions [16]. The high- VT transistors (Msi) at the inputs and programmable weights bank are used to prevent the current leakage from the parallel channel of double-gate transistors when only one channel of the transistor is turned on, i.e. the transistor will only be turned on under the condition when wi >0 [16]. The high-VT double-gate transistors in this thesis are modeled by the modification of gate metal work functions, as indicated by the device model parameters.

To provide a scale for adjustable weights versus back-gate biasing voltages, a systematic bias study is needed first [16]. In this study the drain current of an IDDG input transistor is recorded at low drain bias conditions typically found at the onset of an evaluation period. The recoded currents are then normalized with respect to a pre-defined reference level corresponding to the weight of one. The resulting range of the mathematical weights is found to vary between 0 and 3, by applying -0.5V and 1.5V to the back-gate, respectively.

We assumed in Fig. 10 that a biasing voltage of +0.5V obtains the unity weight, with weights as large as 5 obtained for larger Vds bias cases [16]. To accurately determine the relation between mathematical weights and back-gate voltages, the dependence of mathematical weights on Vds must be carefully considered. The typical Vds voltages for the input transistors are strongly related to the actual circuit architecture and the number of transistors being turned on, as shown in Fig. 10.

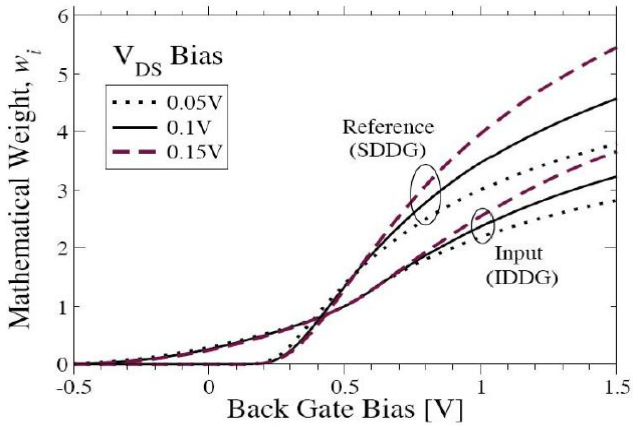

Fig.10: Mathematical weights by back-gate biasing with associated Vds biases [16]

Few examples are provided to illustrate the operation and feasibility of the variable weight DG-TLG circuit. First, the weight programming is clearly demonstrated by a simple simulation found in Fig. 11. It indicates that the back-gate biases at 0.2V, 0.5V, and 0.85V produce corresponding weights of 0.5, 1, and 2, respectively [16].

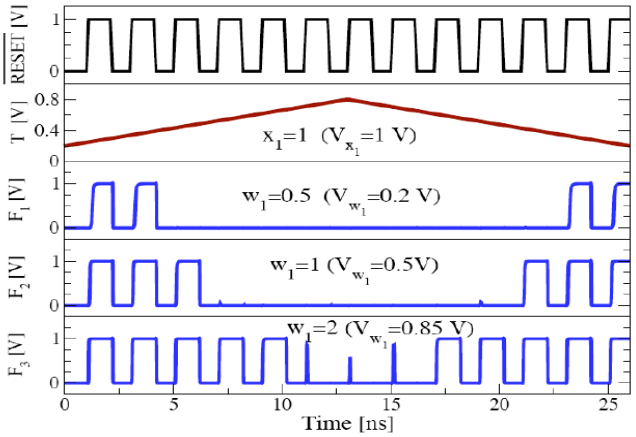

Fig.11: Verification of weight programming by back-gate biasing [16]

Having verified weight-programming capability of the circuit, a four-input variable weight DG-TLG using simulations are illustrated. The three sets of weight vectors are [1, 1, 1, 1], [2, 0, 0.5, 1.5] and [1.2, 1.2, 1.2, 1.2], and are produced with the applied back-gate bias voltages of [0.5V, 0.5V, 0.5V, 0.5V], [0.85V, -0.5V, -0.19V, 0.68V], [0.58V, 0.58V, 0.58V, 0.58V], respectively. Fig. 12 shows that three different functions with three distinct sets of weights are correctly implemented under the same varying T sweepings. For instance, the third function F3=1.2x1+1.2x2+1.2x3+1.2x4 switches at a much higher threshold as compared to the first case F1=x1+x2+x3+x4. Also, the second case with F2=2x1+0x2+0.5x3+1.5x4 shows almost identical switching characteristics as the first case F1, since they have the same combined weights.

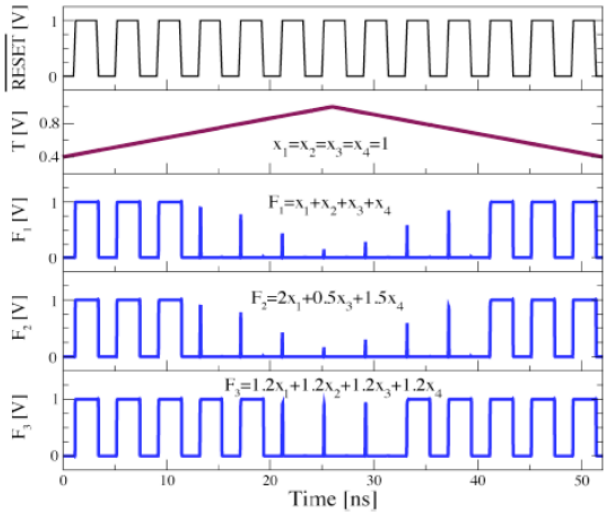

Fig.12: Verification of threshold programmability in resulting logic functions [16]

VI. DG TLG ARCHITECTURE WITH BACK-GATE BIASING

The back-gate biasing changes weights of each transistor associated with the input at the front gate. The typical range of the back-biasing voltages is needed for practical weights and can be found from the plot in Fig. 14 and Table 1. These weights have been calculated by normalizing simulated currents with the IDDG current level at both gates held at 1.0V. The calculated weights have Vds biasing dependency in Fig. 14. It must be noted that to have zero current at wi=0 or xi =0 case, the input transistors must have high-VT (>1.0V) in Fig. 13. Therefore, only when both inputs are active high simultaneously (wi =xi =1) will the IDDG transistor be able to conduct current. The identical half-sized double-gate transistors located in the front of the circuit are biased for contributing half weights in the computation block.

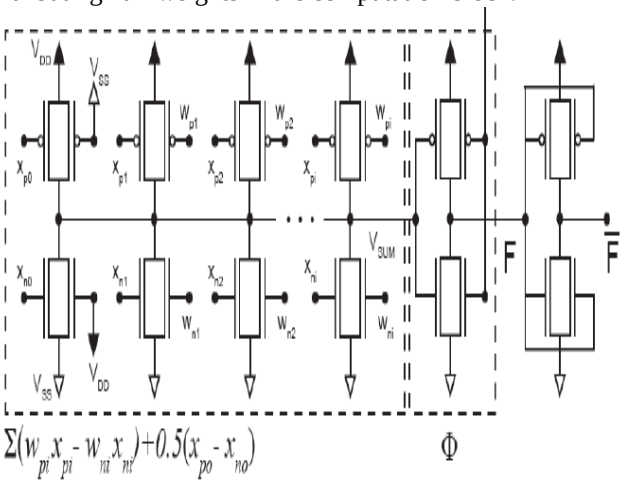

Fig.13: Circuit Schematic for DG dynamic weight threshold logic gates
(p0 :W = 0.27µm,n0 :W = 0.1µm , pn :W = 0.54µm,nn :W = 0.2µm)

Published By:
Blue Eyes Intelligence Engineering
& Sciences Publication

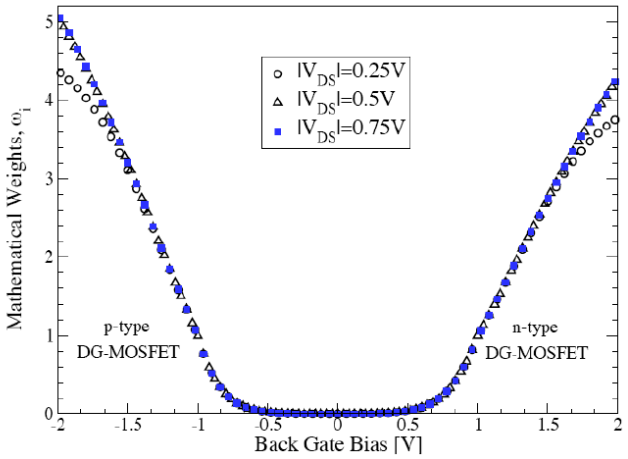

Fig. 14 Associated weights with corresponding back-gate biasing voltages.

Bias Voltages (V) (N-DG/P-DG)	Math. Weights
0.87/-0.9	0.5
1/-1	1
1.15/-1.12	1.5
1.29/-1.24	2
1.43/-1.35	2.5
1.58/-1.46	3

Table.1: Associated mathematical weights with reference biasing voltages.

Table.1 provides a list of reference biasing voltages for associated mathematical weights. To verify the circuit performance and functionality, a SPICE simulation is conducted.

VII. CONCLUSION

The most important breakthrough in designing logic gates presented here is the reconfiguration of circuits using the back-gate biasing of the double-gate transistors. For reconfiguration in these circuits, a systematic back-gate biasing approach is needed. The Boolean logic gates implemented utilize the back-gate biasing either to alter the logic functionality or reduce the overall number of transistors or the silicon area, whereas threshold logic gates utilize back-gate biasing to reduce the number of inputs and/or to provide additional reconfigurability by adjusting the threshold level or input weights. To obtain the desired functionality, however, noise margins in both cases must be optimized, which is more difficult for the latter case. This is because the threshold logic circuits produce many intermediate signal levels in the summing block, and a comparator must identify these signal levels to decide proper binary outputs. Despite the complications with noise margins, threshold logic gates designed with DG-MOSFETs exhibit great potential for flexible functionality and reconfiguration without losing any performance over their SOI counterparts.

REFERENCES

1. S. Hauck, “The roles of FPGAs in reprogrammable systems,” Proc. IEEE, vol. 86, no. 4, pp. 615–638, Apr. 1998.
2. B. Yu, H. Wang, A. Joshi, Q. Xiang, E. Ibok, and M.-R. Lin, “15-nmgate length planar CMOS transistor,” in Tech. Dig. IEDM , 2001, p. 937.
3. H.-S. P.Wong, “Beyond the conventional MOSFET,” in Proc. 31st Eur. Solid-State Device Research Conf., 2001, p. 69.
4. P. Beckett, “Low-power spatial computing using dynamic threshold devices,” in Proc. IEEE Int. Symp. Circuits Syst., 2005, p. 2345.
5. S. Kaya and W. Ma, “Optimization of RF linearity in DG-MOSFETs,” IEEE Electron Devices Lett., p. 308, 2004.
6. G. Pei and E. C.-C. Kan, “Independently driven DG MOSFETs for mixed-signal circuits—I: Quasi-static and nonquasi-static channel coupling,”IEEE Trans. Electron Dev., vol. 51, no. 12, pp. 2086–2093, Dec.2004.
7. M. V. R. Reddy, D. K. Sharma, M. B. Patil, and V. R.Rao,“Power-area evaluation of various double-gate RF mixer topologies,” IEEE Electron Devices Lett., vol. 26, p. 664, 2005.
8. L. Mathewet al., “CMOS vertical multiple independent gate field effect transistor (MIGFET),” in Proc. IEEE SOI Conf., 2004, p. 187.
9. S.Varadharajan and S. Kaya, “Study of dual-gate SOI MOSFETs as RF mixers,” in Proc. Int. Semiconductor Dev. Res. Symp. (ISDRS), Dec. 7–9, 2005, p. 7.
10. J. M. Rabaey, A. Chandrakasan and B Nikolic, “Digital integrated circuits”, Second Edition, Prentice Hall, 2003.
11. K. Bernstein and N. J. Rohrer, “SOI circuit design concepts”, Kluwer Academic Publishers, 2000.104
12. A. Marshall and S. Natarajan, “SOI design: analog, memory and digital techniques”, Kluwer Academic Publishers, 2002.
13. “ISE TCAD Suite,” Synopsis, Mountain View, CA, 2006 [Online]. Available: http://www.synopsis.com
14. S. Mukhopadhyay, H. Mahmoodi and K. Roy, “A Novel High-Performance and Robust Sense Amplifier Using Independent Gate Control in Sub-50-nm Double-gate MOSFET,” IEEE Trans. Very Large Scale Integration Systems (VLSI), vol. 14, no.2, pp. 183-192, Feb. 2006.
15. S. L. Hurst, “Threshold logic”, Mills & Boon Ltd. London, 1971.
16. S. Kaya, H. F.A. Hamed, D.T. Ting and G. Creech, "Reconfigurable Threshold Logic Gates with Nanoscale DG-MOSFETs, "Solid-State Electronics, vol. 51, no.7, pp. 1301-1307, Oct. 2007.
17. Y. Taur, “Analytic solutions of charge and capacitance in symmetric and asymmetric double-gate MOSFETs,” IEEE Trans. Electron Devices, vol. 48, no.12, Dec. 2001.

AUTHORS PROFILE

Soumen Biswas received the B.E. degree in Electronics and Communication Engineering from Acharya Institute of Technology under Visveswaraiya Technological University(VTU), Belgaum, Karnataka, India in 2009 and M.Tech degree in Electronics and Communication Engineering from Institute of Engineering and Management under West Bengal University of Technology (WBUT), Kolkata, WB, India in 2011.

Sarosij Adak received the B.Sc degree in Physics from Calcutta University, WB, India in 2007. Also received M.Sc in Electronics and M.Tech in Electronics and Communication Engineering from Vidyasagar University and Institute of Engineering and Management under WBUT , India in 2009 and 2011 respectively**.** He has joined Dream Institute of Technology as Asst. Prof. at Kolkata on November 2011.

.