# Comparative Analysis of Low Power and High Performance PTM Models of CMOS with HiK-Metal Gate Technology at 22nm

**Shobha Sharma**

***Abstract:- This paper analysis the low power and high performance models of PTM with Hi-K metal gate cmos technology by using them in an cmos inverter at 22nm technology node.The characteristics are compared with cmos bulk technology as well. This analysis gives an insight into leakages when the input voltage is sweeping from minimum to maximum voltage.The aim of HiK metal gate technology is to reduce the leakage at sub 32nm node and is a good alternative to cmos bulk technology having high leakage and power dissipation as seen in this paper's comparative analysis. All the simulation is done with hspice simulator at 22nm technology node with PTM models of Arizona state university.***

***Index Terms:- 22nm cmos, body biasing,Scaling issues,ptm models***

## I. INTRODUCTION

Miniaturization is a way of having high performance and low power CMOS circuits. The most correct method of scaling [1,2] is shown in table 1 [4], increases the density and performance without increase in the power consumption, if the area is kept constant[1]. So with scaling, power consumption as well as the cost of production decreases. With miniaturization, the clock frequency increases but the hurdle was the increase in the power consumption [2]. The ITRS update states the same[3]. One of the bottlenecks in scaling is the increase in cost of lithography, difficulty in the search of new technologies and very tiny MOSFETS and larger sensitivity. The gate length shrinkage trend is delaying due to down turn of finances in the semiconductor industry. The Clock frequency kept increasing till 3.2 GHz and even decreased to 1 to 2.5 GHz with multi core Scheme. There are draw backs of increase of power consumption with increase in clock frequency and thus the heating of the device/circuit or system made out of circuits and devices. Fig. 1 shows the trend of clock frequency for local onchip clock frequency. It is forecasted in itrs that the local onchip clock frequency would keep increasing and SRAM at 6GHrtz is already reported [7].

Manuscript received on April 26, 2012.

**Shobha Sharma**, ECE, Indira Gandhi Institute of Technology of GGSIP university,delhi INDIA, (E-mail:hobhaa_sharma16@yahoo.co.in_.

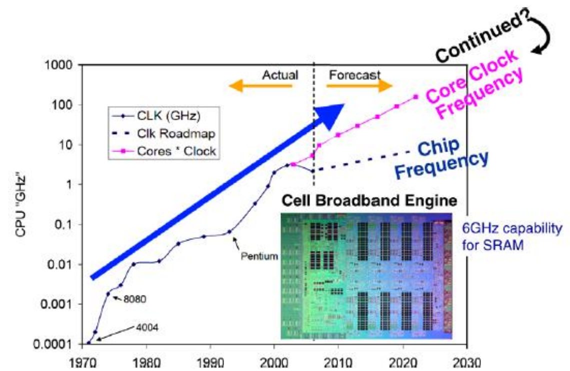



**Fig 1**

With the decrease in supply voltage, the power consumption also decreases. And to decrease the supply voltage, the threshold voltage has to be reduced. With decrease in threshold voltage, the subthreshold off leakage current increases. Then Fig. 2[4] below show the trend of Ids with Vg., with drain to source voltage and threshold voltage.

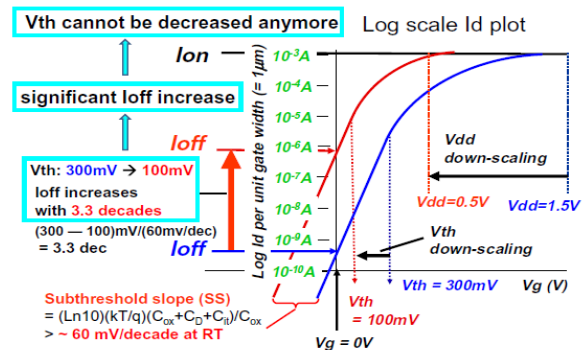



**Fig. 2 leakage current Vs Vdd and Vgate**

The improper down scaling results in off stage leakage current and results in threshold voltage variations due to short channel effect. The variation in the device parameter s in general is another hurdle with advanced technology node. And the trend is to opt for better alternative with respect to technology such as insulator, metal gate high k technology etc. There are reports on use of La2O3 below 0.5nm thickness of tox[8], where saturation is happening.The majour issues as we go for sub 32nm technology is the leakage and power dissipation and is the reason to look out for other technology alternatives apart from traditional CMOS bulk. And it is necessary to analyze these technology models at a targeted technology, 22nm in this case , to know the extent of leakage, power dissipation and or reductions on these while using other technology. Following section gives an insight into 22nm

circuit functionality at CMOS High-K metal gate technology with low power (LP), high performance(HP) and CMOS bulk technology .

## II. SIMULATION RESULT AND DISCUSSION

### *A. Voltage transfer curve with Low power and high performance PTM models of High K metal gate with normal body biasing.*

The w/l of nmos of cmos inverter (Fig. 1)is 44nm/22nm and that of pmos is 132nm/22nm,with load capacitance 20ff. In transient analysis the rise time and fall time of input pulse are 0.3ns each.

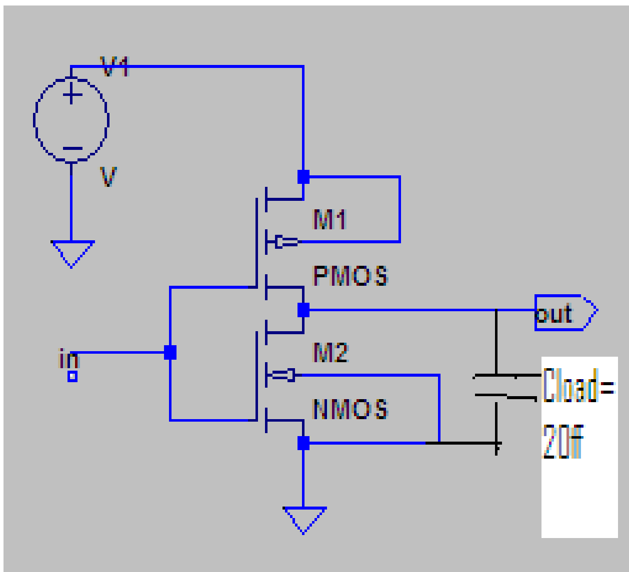
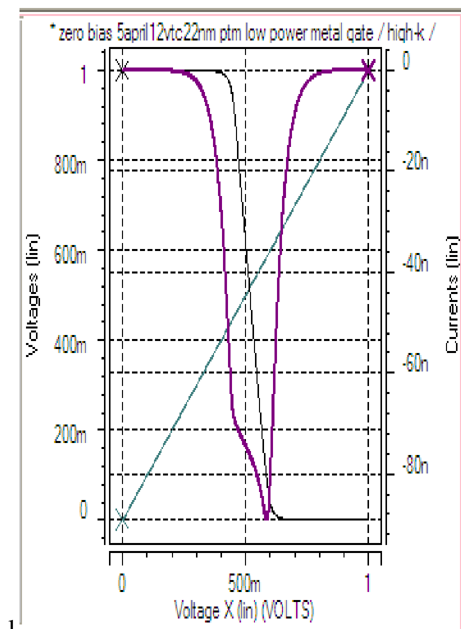



**Fig.1cmos inverter under analysis with two models of PTM**

Fig. 2 Shows the VTC of low power ptm model with maximum short circuit current to be 8.9193Xe-8 A. The comparison with high performance model can be made with Fig. 3 showing the short circuit current to be 17.399Xe-6A. Fig. 4 and 5 show the expected results (to some extent ) of gate current.




1

**Fig. 2 Low power 22nm VTC with normal biasing**

The gate current is not totally zero in 22nm technology node. With vin=0v the gate current of Pmos is maximum, and that of nmos is zero whereas gate current of nmos increases as Vin seeps through half of Vdd to maximum Vdd. See Table I showing the comparison between low power and high speed models of the same inverter.

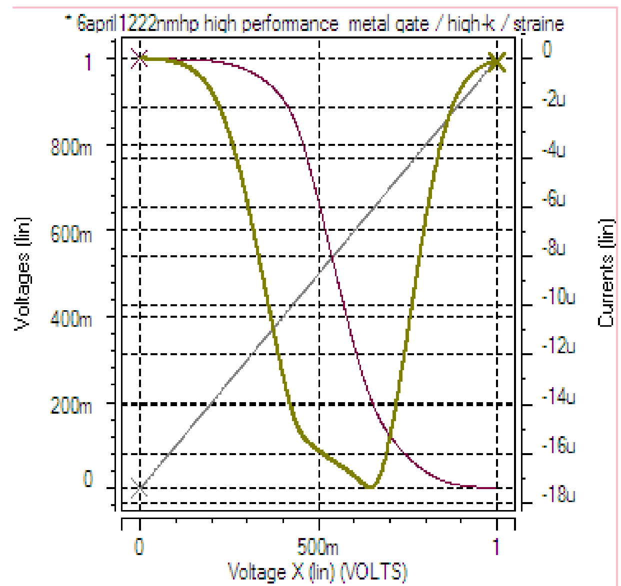



**Fig. 3 High performance 22nm VTC with normal biasing**

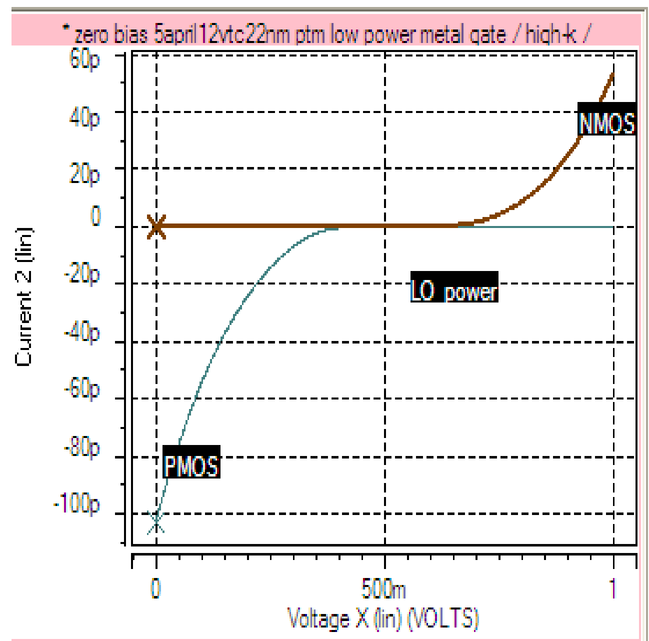



**Fig. 4 Gate current of low power inverter with vin sweep from 0v to 1v**



*Published By:*
*Blue Eyes Intelligence Engineering*
*& Sciences Publication*

International Journal of Soft Computing and Engineering
IJSCE
www.ijsce.org
Exploring Innovation

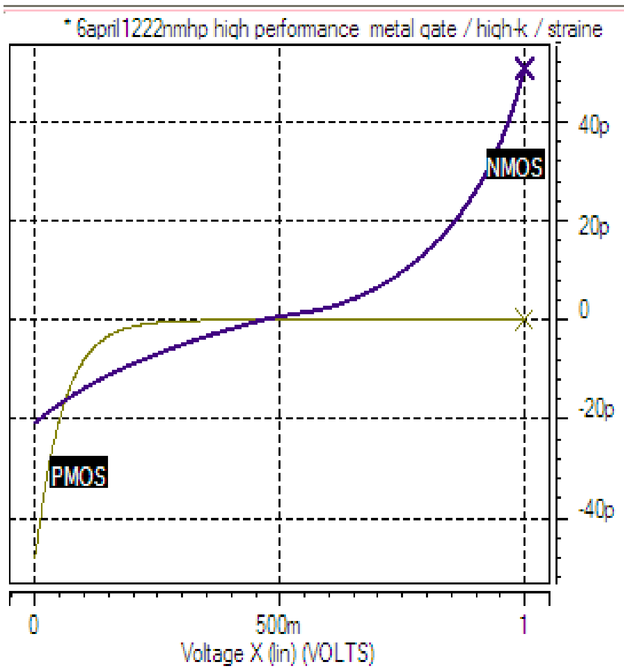



**Fig.5 Gate current of high performance model cmos HiK-metal gate inverter with vin sweep from 0v to 1v.**

Fig. 5 shows the gate current flowing into gate terminal of nmos transistor with high perfomance model, even when Vin is zero.The same current flows into the device with vin sweeping towards maximum supply votage. So comparatively pmos has less leakage characteristics at 22nm Hi K metal gate technology.

### *B.* 22nm BULK CMOS characteristics

Fig.6 below shows the various currents through various terminals of an CMOS 2nm bulk technology-β version(PTM model of Arizona State University, USA).
In the Fig.6 m1→is pmos and n1→ is an nmos. Also 1,2 ,3 denotes drain,gate and source of a transistor.

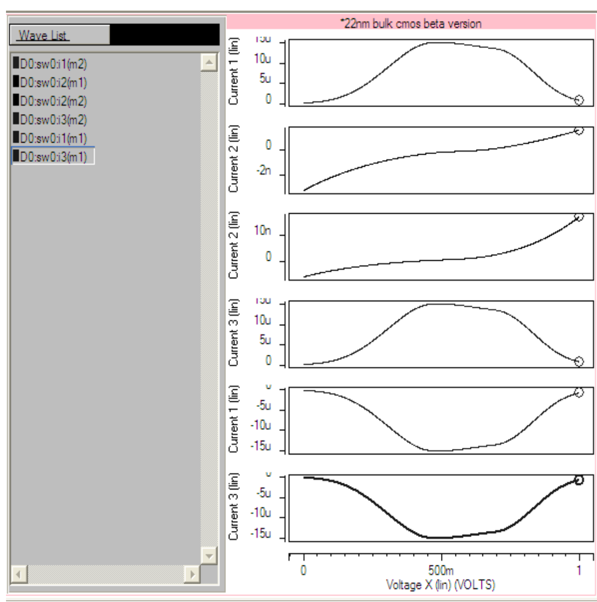



**Fig. 6 drain(i1), gate (i2)and source currents (i3)of pmos(m1) and nmos(m2)**

The table I below helps in analyzing the cmos inverter's behavior in High –K metal gate technology with Low power and High performance models as well as CMOS bulk technology. There is a obvious trend with respect to gate threshold voltage and the currents at supply terminal, gate terminal etc. The device in High-K meta K gate technology has lower currents including the leakages at various ports due to high K of dielectric material being used and can easily be seen by comparing them with CMOS bulk technology.

## III. CONCLUSION

Analysis of the two predictive technology low power and high performance models at High-K metal gate CMOS technology is done at 22nm technology node. The comparative analysis shows result that the Low power models to be used for low leakage applications and for faster performance the HP models are the best.The analysis gives the indication on leakage currents at 22nm node and is useful in designing any circuit with them. The comparison table with cmos bulk inverter shows the greater leakages at 22nm node.

## ACKNOWLEDGMENT

I am thankful to my guide Prof. Ashwani Kumar for all the necessary support. Also thankful to Principal IGIT. And thankful to Honorable Vice Chancellor of Guru Gobind Singh Inderprasth University for providing the researchable atmosphere in the campus.

**TABLE I**
**Comparison table I of 22nm Voltage Transfer Curves of HiK-metal Gate CMOS inverter with low power(LP) and high performance (HP)model and cmos bulk model**

| Sr. No | parameter | Hi-K_MGLP inverter(Amp or V) | Hi-K MG HP inverter(Amp or V) | Cmos BULK |
|---|---|---|---|---|
| 1 | Nominal supply voltage | 0.95 | 0.8 | -- |
| 2 | Temp | 25°C | 25°C | 25°C |
| 3 | Vdd(volts) | 1 | 1 | 1 |
| 4 | Cload | 20ff | 20ff | 20ff |
| 5 | Vth Nmos | 0.68858 | 0.50308 | 0.5118 |
| | vthPmos | -0.63745 | -0.4606 | -0.372 |
| 6 | Rdsw | 230 Ω | 145 Ω | 130 Ω |
| 7 | Max Current thru Vin=0v port(amp) | 100p | 64P | 6n |
| 8 | Max Current thru Vin=1v port | 60p | 52p | 19.5n |
| 9 | Max Current thru Vdd port | 8.9193Xe-8 | 17.399Xe-6 | 15xe-6 |
| 10 | Max PMOS $I_{gate(A)}$ @vin=0V | 102.8572P | 47.9784P | 3n |
| 11 | Min PMOS $I_{gate}$ (A)@vin=1V | $\approx 0$ | $\approx 4.996f$ | 1n |
| 12 | Max NMOS $I_{gate}$ @vin=1V | 53.5080P | 50.5924P | 20n |
| 13 | Min NMOS $I_{gate(A)}$ @vin=oV | $\approx 0$ | $\approx 5.7732f$ | 5n |
| 14 | Vsat m/s | 170000-N and PMOS | 210000-N and P mos | 20,0000-nmos 78000-pmos |

## REFERENCES

1. Dennard A. R. LeBlanc et al, SSC 256.
2. Hiwai,ohmi microelectronics reliab 1251 42 (2002)
3. www.itrs.net
4. H lwai IEDM 2008
5. Ono et al,ieee transaction on elec devices,42 ,1510
6. www.freescale.com
7. Pille et al,Issscc Dig tech 2007, p322-323
8. Kukushima et al, iwdtf,2008
9. Kuhn et al, IEDM tech dig 2007 p471
10. Bohr et al Proceedings ICSICT 2008 p13
11. www.intel.com
12. Morita et al, Symp on VLSI circuit 2007,p256
13. Hlwai IWJT 2008
14. Zimmermann and W. Fichtner, \Low-power logic styles," IEEEJSSC, vol. 32, no. 7, pp. 1079 1090, R1997.
15. G. E. Moore et al., Cramming more components onto integrated circuits," Proceedings of the IEEE, vol. 86, no. 1, pp. 82 85, 1998.

## AUTHORS PROFILE

**Shobha** Sharma: She has done her M.E. from BITS Pilani. She is a member of IEEE USA. She has a research interest in nano VLSI and has published 7 research papers in international and national journals and conferences.