# A Novel Efficient CNTFET Gödel Circuit Design

**Peiman Keshavarzian, Mahla Mohammad Mirzaee**

***Abstract*— Carbon nanotube field effect transistors (CNFETs) are being extensively studied as possible successors to Silicon MOSFETs. Implementable CNTFET circuits have operational characteristics to approach the advantage of using MVL in voltage mode. In this paper we used CNTFETs to implement the improved Gödel basic operators. This paper presents arithmetic operations, implication and multiplication in the ternary Godel field through carbon nanotube field effect transistors (CNFETs). Consequently, in the novel Gödel circuit design, the simulation results demonstrate an improvement in the circuit parameters such as delay, power and power delay product.***

***Index Terms*— CNTFET, MVL, TVL, Gödel.**

## I. INTRODUCTION

Into an era of nanotechnology, molecular devices are becoming promising alternatives to silicon technology. Nanotechnology is a novel field of research that cuts across many fields – electronics, chemistry, physics and biology that analyzes and synthesizes structures in the nano scale ($10^{-9}$ m) such as nano particles, nanowires, Nanotubes, etc[1]. Carbon Nano Tube (CNT) has attracted attention in recent years not only for its relatively small dimensions and unique morphologies, but also for its potential of implementation in many emerging technologies[2].

CNT is one of the several cutting-edge emerging technologies within nanotechnology with high efficiency and a wide range of applications in many different streams of science and technology. Compared to binary logic, the multiple-valued logic circuits provide better performance in chip size, speed, small number of interconnections also we have simpler realization of logical functions[3].In the last decades, because of all the multiple-valued logic circuit designs benefits a considerable attention have been shown. MVL circuits have more than two logical levels and depending on the number of levels, we may have ternary (base=3) or quaternary (base=4) logic styles [3-4]. Nano-circuits based on CNTs such as CNT Field Effect Transistors (CNTFETs) show big promise of consuming less power and to be much faster than available silicon based FETs [5]. In CNTFETs, the threshold voltage of the transistor is established by the diameter of the carbon nanotubes (CNTs). Therefore, a multiple-threshold design can be achieved by employing CNTs with different diameters (which will be controlled by chirality) in the CNTFETs. A Galois field with CNTFET-based ternary circuit designs have been proposed in[5-7]. In[5-6] resistors are used to prepare a voltage division .The design technique that will be used in this paper eliminate the large resistors by employing active load with p-type and n-type CNTFETs in the ternary logic circuit[7-8].The outline of this paper is as follows. In section 2, Gödel outlines are described, in section 3 CNT field effect transistor (CNTFET) are inspected. In section 4 an improved Gödel circuit design, its implementation and its result are presented. Conclusions are demonstrated in section 5.

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## II. GODEL ALGEBRA

The geometry dependent threshold voltage of carbon nanotube FETs (CNTFETs) has been often used to design ternary logic family [9-10]. MVL circuits can reduce the number of operations necessary to implement a particular mathematical function and further, have an advantage in terms of reduced area. In comparison to the fastest binary counterpart, Chip area and power dissipation have been shown to be reduced using efficient MVL implementation [3].

BL algebras were introduced by Hajek as the algebraic structures for his basic logic. Gödel algebras is the particular cases of BL algebras and were defined as the algebraic structure for the Gödel's logic. Godel logic is built from propositional variables, Gödel's connectives (&,→) and the truth constant 0 for the logical "zero" and 1 for the logical "one". Gödel formulas are defined in the obvious way: each propositional variable is a formula; 0, 1are formulas; If we have α and β as the formulas then α & β and α → β are formulas, consequently. Further connective are defined as follows:

$$\neg \alpha = (\alpha \rightarrow 0)$$
$$\alpha \wedge \beta = \alpha \,\&\, (\alpha \rightarrow \beta)$$
$$\alpha \beta = ((\alpha \rightarrow \beta) \rightarrow \beta) \vee \wedge ((\beta \rightarrow \alpha) \rightarrow \alpha)$$
$$\alpha \equiv \beta = (\alpha \rightarrow \beta) \,\&\, (\beta \rightarrow \alpha)$$

Gödel algebras is a BL algebras which fulfills these condition:

$$(\alpha \rightarrow \beta) \wedge (\beta \rightarrow \alpha) = 1$$
$$\alpha \,\&\, \alpha = \alpha \text{ (idempotent )}$$

In general we can't prove that the deduction theorem is valid for the classical logic but in the Gödel logics this theorem is provable. If we suppose the particular cases which the truth values belong to {0, 1/ 2, 1}, then the truth table of the connectives are as follows (Table I and Table II).

| & | 0 | 01-Feb | 1 |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 01-Feb | 0 | 01-Feb | 01-Feb |
| 1 | 0 | 01-Feb | 1 |

**TableI Godel field multiplier**

**TableII Godel field implication**

| → | 0 | 01-Feb | 1 |
|---|---|---|---|
| 0 | 1 | 1 | 1 |
| 01-Feb | 0 | 1 | 1 |
| 1 | 0 | 01-Feb | 1 |

## III. CNTFET

Carbon nanotube field effect transistors is a propitious technology which have been replaced with primitive silicon devices. A field-effect transistor (FET) based on a single wall carbon nanotube (SWCNT) was successfully fabricated and demonstrated to be able to operate at room temperature in 1991 [11-12]. Carbon nanotube field-effect transistors (CNTFETs) have attracted significant interest as the next-generation devices for nanoelectronics. Fig. 1(a) illustrates one-dimensional conductor named single walled carbon nanotube (SWCNT) that can be either metallic or semiconducting depending upon the arrangement of carbon atoms defined by their Chirality, Ch (i.e. the direction in which the graphite sheet is rolled ) whose magnitude with CNT diameter (DCNT) is given by Eq. 1 and Eq. 2 respectively where 'a' is the graphite lattice constant (0.249nm) and n1, n2 are positive integers that specify the chirality of the tubes SWCNT can be supposed as a sheet of graphite which is rolled up and joined together along a wrapping vector (Eq.1) , as shown in Fig. 1(b), where a1, a2 are unit vectors [13]. The CNT is called zigzag, if n1 = 0, armchair, if n1 = n2, and chiral otherwise.

$$C_h = \sqrt{n_1.a_1 + n_2.a_2} \qquad \text{(Eq.1)}$$

$$D_{cnt} = C_h / \pi \qquad \text{(Eq.2)}$$

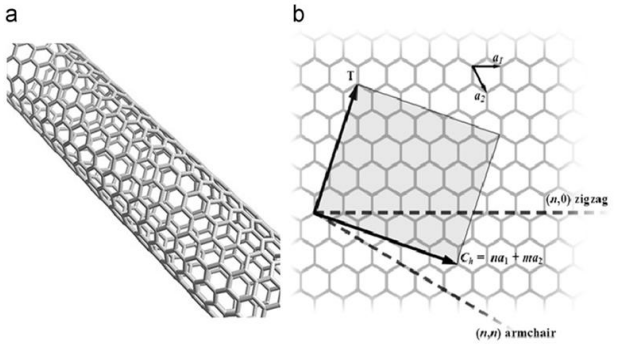


**Fig.1 (a) SWCNT (b) Graphite sheet in terms of chirality n1 and n2**

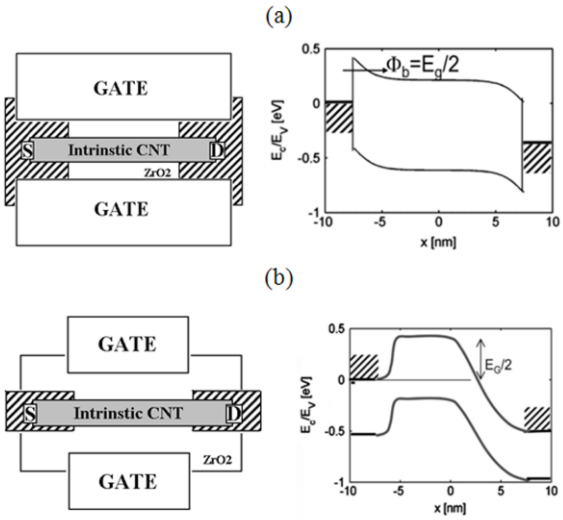


**Fig. 2 Two type of single walled CNTFETs**

There are two types of carbon-nanotube transistors that are being extensively studied. One is a tunneling device Fig .2(a) that works on the principle of direct tunneling through a Schottky barrier at the source–channel junction .The barrier width is modulated by application of the gate voltage so that transconductance of the device is dependent on the gate voltage [16] .To overcome these disadvantages associated with Schottky barrier CNTFETs, there have been attempts to develop CNTFETs which would behave like normal MOSFETs. These attempts have met significant success so far with an enormous potential. The MOSFET-like CNTFET (Fig. 2 (b)) operates on the principle of barrier height modulation by application of the gate potential. In this paper, we will consider the non-Schottky-barrier MOSFET-like unipolar CNTFET with ballistic transport as our device of interest. Hereafter in this paper the abbreviation CNTFET will be used to denote such a MOSFET-like device unless otherwise stated (Figure 2 (b) shows the band diagram of this device)[16][17][18]. The source Fermi level for a degenerately doped source can be derived from the conduction band edge. Inside the intrinsic channel, the Fermi level is in the middle of the bandgap. An important property of these CNTFETs is that the bandgap is inversely proportional to the diameter of nanotube as Eq.3 [19, 20].

$$E_g = \frac{0.84}{d(nm)} ev \qquad \text{(Eq.3)}$$

$$V_{th} = \frac{0.42}{d(nm)} ev \qquad \text{(Eq.4)}$$

As the barrier height determines the threshold potential of a FET, the threshold voltage of the CNTFETs can be expressed as Eq.4.This geometry-dependent threshold voltage has been exploited in this study to obtain CNTFETs that turn on at different voltages depending on their diameters. It is worth mentioning that the circuit realization of the ternary logic family involves dual- transistors. CNTFETs provide an opportunity to obtain two functional behaviors by using two different tube diameters.


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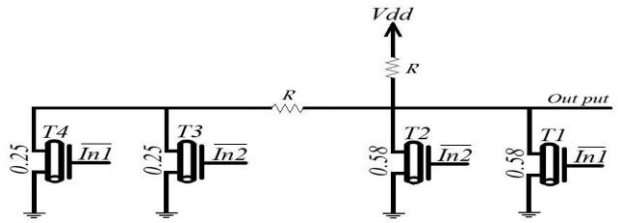
CNTFETs provide the unique opportunity of being controlled by changing the carbon nanotube diameter. Therefore, in this paper, we have used a dual-diameter CNTFET-based design for the ternary logic implementation to present TVL Godel field circuit design.

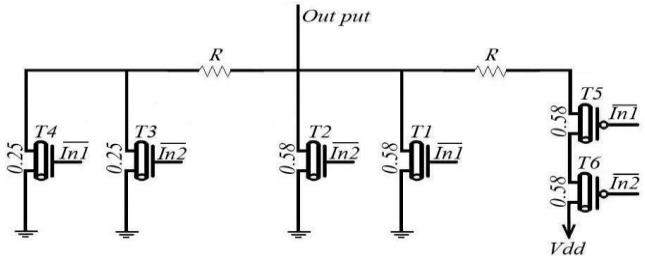
## IV. GODEL CIRCUIT DESIGN

At the first circuit design of Gödel multiplier (Fig 3(a)), we consume four N-CNTFET transistors with resistance pull up, the threshold voltage of T1and T2 are equal to 0.25 and the threshold voltage of T3 and T4 are 0.58, therefore by using two nanotube diameters we can implement this conjunction circuit design. If IN1 or IN2 are equal to zero (their voltages are less than 0.25 volts), one of the connections to the ground via T1 or T2 will be turned on, thus the output (IN1& IN2) is connected to the ground directly and (IN1&IN2) will be held at "zero". If (IN1, IN2) = { (1/2 ,1/2) , (1,1/2), (1/2,1)} , then T3 or T4 will be turned on and by a voltage division we have Vdd/2 on the output. When (IN1, IN2) = (1,1) there isn't any connection to ground, therefore we have Vdd on the output node because of the permanent active path to the highest voltage (resistance pull up).An improved Gödel multiplier circuit design also included two P-CNTFET transistors to control the permanent path to the highest voltage and to achieve better performance than the previous circuit design. When IN1 and IN2 has the voltage higher than logical "zero" (0.25 volts), T5 and T6 will connect the output to the highest voltage (Vdd). In the previous design the pull up resistance has been encountered our design with the permanent output value (Vdd ), so that to approach the expected output values we should control this permanent value by controlling all the other circuit elements, this problem deteriorate our circuit design parameters such as delay, power and also our power delay product.

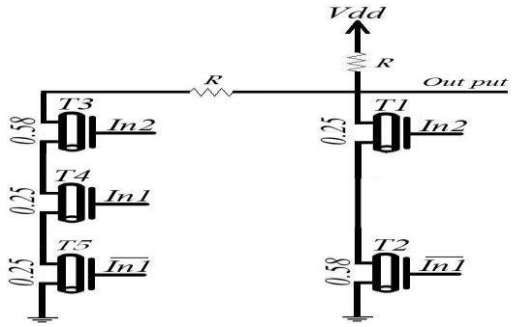
a)




b)




c)




d)

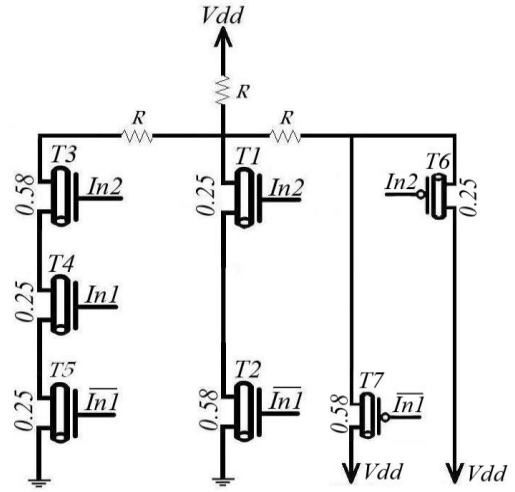



**Fig.3(a),(b) Gödel multiplier circuit design. (c),(d) Gödel implication circuit design**

The Gödel multiplier function (Fig 3(b)) , use the novel circuit designs to control all the paths by detecting each combination of inputs, even the previous permanent pull up voltage, has been controlled by using P-CNTFETs with resistive pull-ups to achieve the better performance. We approach an improvement in the circuit parameters such as delay, power and power delay product by controlling all the output paths, so we could restrict affecting persistent Vdd value to the output. Fig 3(c) illustrates the circuit characteristics of a two input implication operator (→) with IN1 and IN2 as the inputs, the output will be equal to (IN1→IN2). Consider when IN1 is "zero" and IN2 is "1/2" or "one", for this combination of inputs T1 and T2 will be turned on and the output will be connected to the ground directly, so that we will have zero at the output node. For combination of (IN1, IN2) = (1/2, 1), (T3, T4, T5) will be turned on respectively and by a voltage division, output voltage reaches to Vdd/2. In the other combination of inputs we haven't any connection to the ground and therefore pull up resistors will connect the output to Vdd directly. In the secondary implication operator circuit design (Fig 3(d)) in order to control the permanent path to the Vdd that will be affected the output values; two P-CNTFET transistors with resistive pull-ups have been utilized. When IN1 is greater than "zero", T5 will be open the connection to the Vdd also when IN2 is greater than "zero", T6 will be open the connection to the Vdd. For each combination of inputs only one predominant output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path is activated. Therefore through our circuit design structure, appropriate voltage division held the output at the expected stable voltage. A compact model of CNTFETs has been used and simulations have been carried out using HSPICE. The details of the modeling technique are available in [19-20]. In this novel ternary CNTFET circuit design technique a complementary CNTFET network can be used to accomplish impressive performance, low power consumption, avoiding the use of resistors and reduce area overhead.Fig.4 and Fig.5 show the proposed CNTFET based Godel field Circuit Designs to achieve two different threshold voltages we use two different chiralities of the CNTs {(19, 0), (9, 0)}.The diameters of transistors are 1.487nm, 0.783 nm (Eq.2). Therefore, the threshold voltages of N-CNTFETs are 0.289V, 0.559V (Eq.4). The threshold voltages of P-CNTFETs are -0.289V, -0.559V.The novel efficient Godel field circuits use novel design technique for ternary logic gates based on CNTFETs that control all the paths by detecting each combination of inputs. Even the previous permanent pull up voltage has been controlled by using P-CNTFETs without any resistors to achieve the best performance. It is obvious that omitting resistive pull-ups and controlling all the output paths so we could restrict affecting persistent Vdd value to the output and we achieve an improvement in circuit parameters such as delay, power consumption and power delay product. We add new P- CNTFETs channels to prepare the voltage division instead of resistors in both designs (Godel multiplier and implication) to appropriately activate our "Vdd to the output" path. This geometry-dependent threshold voltage has been exploited in this study to obtain CNTFETs that turn on at different voltages depending on their diameters. It is worth mentioning that the circuit realization of the ternary logic family, involve dual- transistors. CNTFETs provide an opportunity to obtain two functional behaviors by using two different tube diameters.

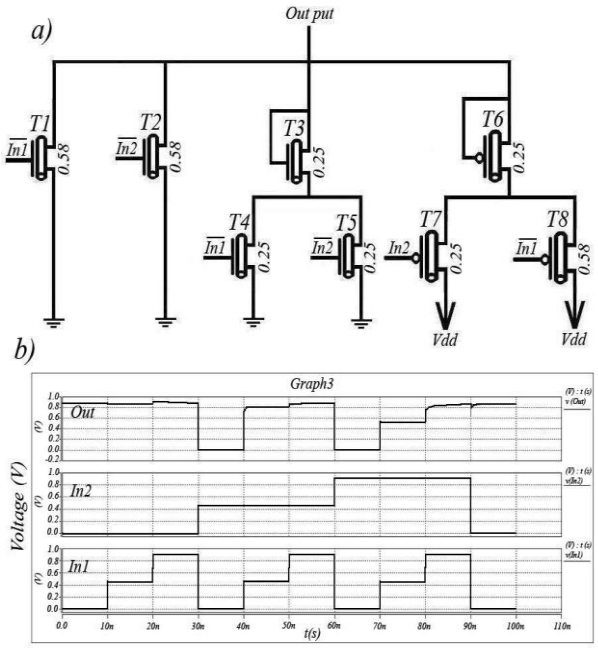


**Fig. 4(a) Novel efficient Godel field multiplier circuit (b) Simulation results sample design**

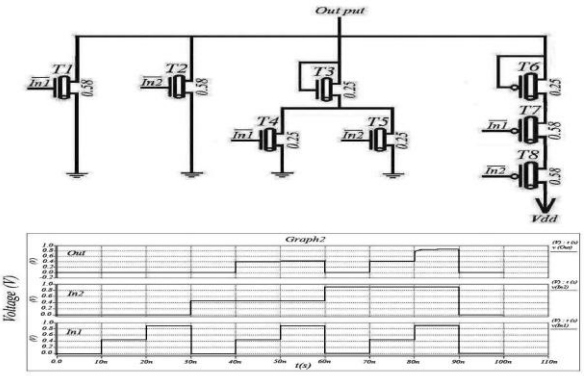


**Fig. 5(a) Novel efficient Godel field implication circuitdesign (b)Simulation results sample design**

CNTFETs provide the unique opportunity of being controlled by changing the carbon-nanotube diameter. Therefore, in this paper, we have used a dual-diameter CNTFET-based design for the ternary logic implementation. Simulation results show degradation in terms of power consumption, delay and improvement in speed. Also, we have achieved an efficient ternary Gödel circuit design. We present improved and efficient Gödel multiplier and implication as the basic operators in the multiple valued-logic, the comparison results are illustrated in table. III.

**Table . III The comparison results**

| Vdd=0.9 | Average delay($10^{-12}$) | Average power($10^{-6}$) | PDP($10^{-18}$) |
|---|---|---|---|
| Godel mul | 8.9706 | 7.9503 | 7.1319 |
| Improved GM | 13.6506 | 4.9391 | 6.7421 |
| Novel GM | 7.8359 | 3.9917 | 3.2785 |
| Godel imp | 9.5038 | 5.3598 | 5.0938 |
| Improved GI | 8.5698 | 4.432 | 3.7981 |
| Novel GI | 7.8504 | 3.0328 | 2.3808 |

In this section, the proposed designs are simulated at different supply voltage using synopsys hspice .In the all situations we measured the average propagation delay and average power consumption. In order to make trade-off between the delay and average power consumption parameters ,the PDP metric is calculated, which is the multiplication of average delay and average power consumption .In the first experiment the circuits are simulated at 0.8,0.9,1,1.2 supply voltages.when the voltage of power supply increases the simulation results shows that the propagation delay will be decrease versus increasing power dissipation.By considering the effect of parameter variations with supply voltage(Vdd) as depicted in fig.8 ,fig.9 and fig.10. It was found that for the best performance ,the supply voltage must be set around 0.9V.

Reducing the supply voltage decreases the power consumption due to proportional scaling but it also affects the circuit delay and PDP. By changing Vdd the denouements, result in that we have the best delay in Vdd = 1.2V. In addition ,Godel multiplier is 47.966% ,43.279% , and 23.606% worse than the circuit design in Vdd=1.2V , for 0.8V, 0.9V and 1V,respectively.,Godel implication is 37.595% , 21.823% and 3.623%, worse than the circuit design in Vdd=1.2V , for 0.8V, 0.9V and 1V,respectively.

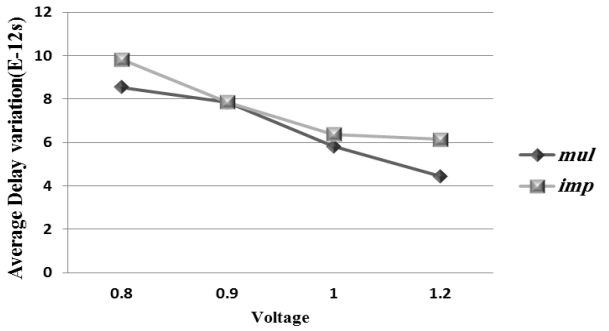


**Fig.8 Variations of delay with supply voltage for Godel field circuit**

As it was shown in fig.9 we have the best power in $V_{dd}$=0.8V. In addition , Godel multiplier is 43.755%, 64.511% and 83.630% worse than the circuit design in $V_{dd}$=0.8V,for 0.9V, 1.0V and 1.2V, respectively.,Godel implication is 44.0648%, 64.9706% and 86.0905% , worse than the circuit design in $V_{dd}$=0.8V,for 0.9V, 1.0V and 1.2V, respectively.

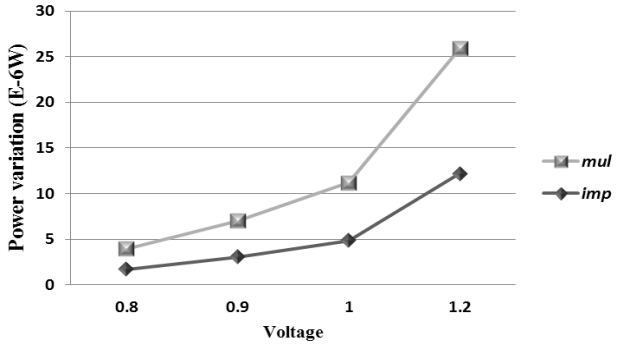


**Fig.9Variations of power with different supply voltage for Godel field circuit**

Fig.10 illustrates that we have the best PDP for implication and multiplier in Vdd=0.8V.In addition Godel multiplier is38.690%,47.897% and 68.540% worse than the circuit design in Vdd=0.8V, for 0.9V , 1.0V and 1.2V ,respectively. Godel implication is 29.928%, 45.906% and 77.710% worse than the circuit design in Vdd=0.8V, for 0.9V, 1.0V and 1.2V, respectively.

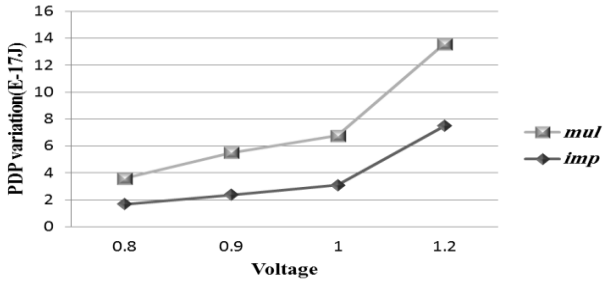


**Fig.10 Variations of PDP with supply voltage for Godel field circuit**

## V. CONCLUSION

In this paper we have presented an improved Gödel circuit design using carbon nanotube field effect transistors. We have achieved a significant improvement in delay, power and power delay product. This design controls all the three stable output voltage values by controlling the appropriate carbon nanotube field effect transistors. To achieve an improved Gödel operator's circuit designs, all the CNTFETs have been used to activate the adequate guidance path and to disable all the other paths to the output, thus we have three stable voltage values on the output node.

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