A Modified XTEA

Niladree De, JaydebBhaumik

Abstract—This paper presents a modified Extended Tiny Encryption Algorithm (XTEA). A nonlinear Boolean function called Nmix is used to replace addition modulo $2^{32}$ in the original XTEA. The proposed design has been implemented on a FPGA platform. Simulation result shows that it requires a reasonable hardware and provides an acceptable throughput. It is shown that proposed design requires less hardware compared to XTEA.

Index Terms—Extended Tiny Encryption Algorithm (XTEA), Nonlinear Mixing Function, VLSI Implementation.

I. INTRODUCTION

Security of information has become a main issue in the ever-evolving world of small mobile devices such as personal digital assistants (PDAs) and cell phones. Cryptographic algorithms and protocols constitute the central component of systems that protect network transmissions and stored data. In such small devices, the fight over high performance and low power consumption, besides security are primary targets. A great deal of assistance in creating low-power and high-speed cores, comes from the simplicity of the selected algorithm for embedding as a hardware component.

In cryptography, a block cipher is a bijective mapping from $\{0,1\}^n$ to $\{0,1\}^n$, parameterized by a key $\{0,1\}^k$. Typically, block sizes are $n \in \{64,128,256\}$ and key size $k \in \{128,192,256\}$. During encryption it takes a block of plaintext as input, and produces a block of corresponding ciphertext. The decryption algorithm takes a block of ciphertext together with the secret key, and yields the original block of plaintext. Many encryption algorithms are now available in the market and the selection of a specific one is dependent on the relatively tight constraints in small devices. The selected algorithm should be small, relatively secure, with a proven history of overcoming possible well-known attacks on it.

Advanced Encryption Standard [14] is the most popular block cipher which is used everywhere for encryption. It is mainly designed for software implementation. So it is not suitable for extremely constrained environments like Radio-frequency identification (RFID) tags and sensor networks. The Tiny Encryption Algorithm (TEA) [1] for such type of application has been proposed by Wheeler and Needham. Its successor the Extended-TEA or XTEA has been introduced in [8]. Several attacks against XTEA have been reported in [3, 4, 5, 6, 9].

A nonlinear Boolean function Nmix and its inverse I-Nmix have been introduced in [13]. In this paper a modified XTEA was proposed. Here a new nonlinear Boolean Nmix function has been used during encryption and I-Nmix is used in decryption. Whereas in original XTEA, addition modulo $2^{32}$ is used during encryption and subtraction modulo $2^{32}$ is used during decryption.

The rest of the paper is organized as follows: Next section provides a brief overview of Extended Tiny Encryption Algorithm (XTEA). Existing attacks on block cipher XTEA introduced in section 3. Modified XTEA is introduced in section 4. VLSI implementation result of proposed architecture is presented in section 5 and finally the paper is concluded in section 6.

II. BRIEF OVERVIEW OF XTEA

The Extended Tiny Encryption Algorithm (XTEA) is a block cipher that uses a cryptographic key of 128 bits to encrypt or decrypt data in blocks of 64 bits. Each input block is split into two halves $L_n$ and $R_n$ which are then applied to a routine similar to a Feistel network for $N$ rounds, where $N$ is typically 32. Most Feistel networks apply the result of a mixing function to one half of the data using XOR as a reversible function. On the other hand, XTEA uses integer addition modulo 232 during encryption and subtraction modulo 232 during decryption. Operations used in XTEA are just exclusive-or, additions and shifts for encryption.

In case of XTEA 64 bit input is divided into two 32 bits variables ($L_n$, $R_n$). The variables $L_n$, $R_n$ sub-key, have a length of 32 bits. All additions and subtractions within XTEA are modulo 232. Logical left shifts of $R_n$ by 4 bits are denoted as $R_n<<4$ and logical right shift by 5 bits as $R_n>>5$. The symbol $\oplus$ denotes the bitwise XOR operation. The constant $\delta$ has value of 9ec779b9x and ($L_n$, $R_n$) are the input of the $n$-th round, for $1 \leq n \leq 64$. The corresponding output of the $n$-th round is ($L_n+1$, $R_n+1$), where $L_n+1 = R_n$ and $R_n+1$ is computed using the following equations:

For each $i \ (1 \leq i \leq 32)$,

If $n = 2i - 1$

$$R_{n+1} = L_n \oplus (((R_n \ll 4) \oplus R_n) \gg 5) \oplus R_n) \oplus K((i-1), \delta \gg 11) \& 3$$

And if $n = 2i$,

$$R_{n+1} = L_n \oplus (((R_n \ll 4) \oplus R_n) > 5) \oplus R_n) \oplus (i, \delta \oplus K(i, \delta \gg 11) \& 3)$$

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A Modified XTEA

XTEA has a very simple key schedule: the 128-bit master key $K$ is split into four 32-bit blocks $K_0$, $K_1$, $K_2$ and $K_3$. Then, for $r = 1, \ldots, 64$, the round keys $K_r$ are derived from the following equation:

$$K_r = K_{r-1} \oplus \left( \frac{T}{2} \times 6 \times 11 \right) R_3 \quad \text{if } r \text{ is odd;}$$

$$K_r = K_{r-1} \oplus \left( \frac{T}{2} \times 6 \times 11 \right) R_3 \quad \text{if } r \text{ is even;}$$

As shown in Fig. 1, XTEA has a very simple round function.

III. EXISTING ATTACKS ON XTEA

There exist various adversary models that are classified with respect to the operations on the inputs and outputs of the cipher (i.e. plaintext, ciphertext and key) the adversary is allowed to perform. Normally, one distinguishes between such operations as reading access (known values), writing access (chosen values) and adaptive writing access (adaptively chosen values). In this section, different existing attacks on XTEA have been discussed.

Chosen plaintext attacks: The adversary can choose plaintexts to be encrypted by the cipher prior to the attack and has reading access to the corresponding ciphertexts during the attack. The most known attack of this kind is differential cryptanalysis. Biham et al. [8] developed differential cryptanalysis method to attack block ciphers. This attack is the general method of attacking cryptographic algorithms. It has exposed the weakness in many algorithms. It looks specifically at ciphertext pairs: pairs of ciphertexts whose plaintexts have particular differences and analyzes the evolution of these differences as the plaintexts propagate through the rounds of the encryption algorithm when they are encrypted with the same key. The two plaintexts (with a fixed difference) can be chosen at random as long as they satisfy particular differences. Then, using the differences in the resulting ciphertexts, assign different probabilities to different keys. As we analyze more and more ciphertexts, one key will emerge as the most probable or correct key. Differential cryptanalysis on TEA and XTEA has been reported in [5].

A 12-round impossible differential characteristic of XTEA:

Moon et al. presented an impossible differential cryptanalysis on reduced round XTEA in [4]. For sake of completeness a construction of a 12-round impossible differential characteristic of XTEA is discussed here. Let an input difference be

$$(A_{012} \oplus b_{10} 0, 0, 0, 0, 0, 0, 0) || b_{000} 0, 0, 0, 0, 0, 0, 0). (1)$$

Then the difference after round 6 must be of the form

$$(N_0, O_P, Q, R, S_{f6} || b_{10} 0, 0, 0, 0, 0, 0, 0). (2)$$

On the other hand, we can predict the difference after round 6 from the output difference of round 6, i.e., to consider the differentials in the backward direction. Similarly to the 6-round differential characteristic with probability 1, there is a backward 6-round differential characteristic with probability 1. It has the difference

$$(a_{000} 0, 0, 0, 0, 0, 0, 0, 0 || A_0 b_{10} 0, 0, 0, 0, 0, 0, 0). (3)$$

After round 12, and then it is clear that the difference after round 6 must be of the form

$$(T_U, V_0, W_1, X_2, Y_3, Z_{f6} || b_{10} 0, 0, 0, 0, 0, 0, 0). (4)$$

Combining these two differential characteristics, it can be concluded that any pair with input difference $(1)$ before round 1 and output difference $(3)$ after round 12 must have differences of the form $(2)$ = $(4)$ after round 6. But this event never occurs. Therefore, this characteristic is a 12-round impossible characteristic of XTEA.

8-Round Related Key Truncated Differential Characteristic:

An 8-round truncated differential characteristic in order to attack 23 rounds of XTEA has been reported in [6]. Here, an 8-round related key truncated differential characteristic is constructed. Let $\Psi$ be our 8-round related key truncated differential characteristic described. The following section describes the proposed modified XTEA.

IV. MODIFIED XTEA

In this section we discuss about modified XTEA. The basic operators like left shift ($<$), right shift ($>$), xor operation ($\oplus$) are same as previous version of XTEA. But, here we replaced the modulo addition and subtraction $2^32$ by a function $\text{Nmix}$ and $I$-$\text{Nmix}$ during encryption and decryption respectively. In Figure 2, the $F_{i\rightarrow j}$ and $F_{j\leftarrow i}$ function are the $\text{Nmix}$ function operating from most significant bit to least significant bit and least significant bit to most significant bit respectively.

Proposed Architecture:

Here two inputs plaintext are $Y_1$ and $Z_1$ both are 32 bits, but for the $\text{Nmix}$ and $I$-$\text{Nmix}$ we used four 8 bit parallel operations, i.e., for both LSB and MSB operation we used bitwise operation.

$\text{Nmix}$: The function $\text{Nmix}$ operates on two n-bit variables $X=(x_n, x_{n-1} \ldots x_0)$ and $K=(k_n, k_{n-1} \ldots k_0)$ and produces an n-bit output variable $Y=(y_n, y_{n-1} \ldots y_0)$, where $Y=F(X, K)$ and F is the $\text{Nmix}$ function. Each output bit of $\text{Nmix}$ is related to the input bits by the following relationship
\[ Y_i = x_i \oplus k_i \oplus c_{i-1} \]
\[ c_i = \bigodot_{j=0}^{i} x_j k \oplus c_{i-1} \oplus x_i \oplus k_{i-1} \cdot k_i \]

Where \( 0 \leq i \leq n-1 \), \( c_{i-1} = 0 \), \( x_{i-1} = 0 \), \( k_{i-1} = 0 \) and \( c_i \) is the carry term propagating from \( i \)-th bit position to \((i+1)\)-th bit position. Each output bit \( Y_i \) is balanced for all \( i \), where \( 0 \leq i \leq n-1 \).

\[ X_i = y_i \oplus k_i \oplus d_{i-1} \]
\[ d_i = \bigodot_{j=0}^{i} y_i k \oplus y_{i-1} \oplus k_{i-1} \cdot k_i \]

Where \( 0 \leq i \leq n-1 \), \( d_{i-1} = 0 \), \( x_{i-1} = 0 \), \( k_{i-1} = 0 \) and \( d_i \) is the carry term propagating from \( i \)-th bit position to \((i+1)\)-th bit position. Function \( G \) is the inverse function of the function \( F \).

**Key Schedule:** In ModifiedXTEA we used same key schedule algorithm as on. The 128 bit master key \( K \) is split into four 32 bits blocks \( K_0, K_1, K_2, K_3 \). Then for \( r = 1, 2, \ldots, 64 \), the round keys \( K_r \) are derived from the following equation:
\[ K_r = K_{r-1} \oplus (R \iff 11) \cdot K_3 \cdot if \ r \ is \ odd; \]
\[ K_r = K_{r-1} \oplus (R \iff 11) \cdot K_3 \cdot if \ r \ is \ even; \]

**V. IMPLEMENTATION RESULTS AND COMPARISON**

Every architectural module has been implemented in Verilog and simulated using Model Sim XE III 6.0a. The design has been synthesized by Xilinx ISE 7.1i tool and the target FPGA device was Spartan3 XC3S5000 which provides low-cost, high-performance logic solution for high-volume, consumer-oriented applications, is used as target device. It produces a maximum frequency of 67.37 MHz and using 1% of slices and input LUTs. Among compact architectures this described design is one of the smallest and better performance architecture. The following table shows performance characteristics of different model of XTEA.

<table>
<thead>
<tr>
<th>Design</th>
<th>Minimum period (ns)</th>
<th>Clock Cycles</th>
<th>Area (slices)</th>
<th>Frequency (MHz)</th>
<th>Throughput (Mbps)</th>
<th>Throughput/area (Mbps/slice)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modified XTEA</td>
<td>14.84</td>
<td>33</td>
<td>238</td>
<td>67.37</td>
<td>130.66</td>
<td>0.55</td>
</tr>
<tr>
<td>XTEA</td>
<td>23.21</td>
<td>33</td>
<td>320</td>
<td>43.08</td>
<td>83.55</td>
<td>0.26</td>
</tr>
<tr>
<td>Tiny XTEA-1</td>
<td>13.87</td>
<td>240</td>
<td>266</td>
<td>71.25</td>
<td>19</td>
<td>0.07</td>
</tr>
<tr>
<td>Tiny XTEA-3</td>
<td>15.97</td>
<td>112</td>
<td>254</td>
<td>66.5</td>
<td>36</td>
<td>0.14</td>
</tr>
<tr>
<td>AES 8-bit</td>
<td>14.93</td>
<td>3900</td>
<td>264</td>
<td>60.93</td>
<td>2</td>
<td>0.01</td>
</tr>
</tbody>
</table>

**Fig.-4:** Results for half-round Modified XTEA compared to different block ciphers

Proposed design gives an acceptable tradeoff between area and the throughput. The modified XTEA gives better throughput of 130.66 Mbps and requires 238 Slices.
A Modified XTEA

VI. CONCLUSIONS

The Modified XTEA architecture is well suited for devices in which low cost and low power consumption are desired. The proposed folded architecture achieves good performance and occupies less area than XTEA. This compact design was developed by thorough examination of each of the components of the Modified XTEA algorithm. The proposed implementation can be accommodated in a very inexpensive Xilinx Spartan-3 FPGA XCS5000. The encryption speed, functionality, and cost make this solution perfectly applicable for resource constrained applications in passive RFID and wireless sensor networks.

REFERENCES


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