FPGA Based SOC for Railway Level crossing Management System

R. Ramachandran, J. Thomas Joseph Prakash

Abstract- It is to develop the FPGA based, System on Chip (SOC) to implement the safety system in Railways for level crossing. For the communication RF module[1] with the coverage of large distance, that is Outdoor line-of-sight: up to 15 miles (24 km) with high gain antenna is used. RF Transceiver has many salient features[2], such as, Advanced Networking & Security, True peer-to-peer (no "master" required) communications, Point-to-point & point-to-multipoint topologies supported, Continuous RF data stream up to 9600 bps, No configuration required for out-of-the-box and Support for multiple data formats (parity, start and stop bits, etc.). An article authored by Mr. R.K. Verma, Chief Engineer, Indian Railways exposes the Corporate Safety Plan [3] of reduction of accidents on Indian Railway (IR) by the year 2012-13. In which, he stated that Collisions of the Trains can be completely eliminated. Derailments can be reduced by 60% and fire accidents by 80%. But, he has not given assurance on possible improvement in level crossing (LC) accidents, as there is no control over the circumstances that lead to such accidents. Train Actuated Warning Device (TAWD) – for sensing an approaching train two kms ahead and to sound an audio-visual warning device at level crossing gates (mainly unmanned ones), helps to reduce accidents at level crossings by giving adequate warning to road users.

LC accidents not only dominate in terms of frequency, but can be more severe in their consequences than other types of railway accidents, simply because they can involve injuries and fatalities to railway passengers, as well as, to road vehicle occupants and other users of LCs. Accidents at LCs accounting for 22% of the total accidents on IR were responsible for 49% of total fatalities during the last decade. Increasing road construction and road vehicle population create greater opportunity for LC accidents to happen. Therefore to avoid this, a well designed sophisticated security system is needed. Hence we developed a prototype system using FPGA based SOC to ensure safety, particularly at unmanned level crossing.

Key words- FPGA, SOC, Level crossing, cyclone II device, EP2C35F672C6.

I. INTRODUCTION

Nowadays**,** Field Programmable Gated Arrays (FPGA)[4,5] based technology is very popular in designing embedded system. Specifically, in recent years, with the development of FPGA, wireless communication technology, RF technology have become hot technology in the field of electronic applications [6]. The objective of the work is to develop a system on chip to transmit and receive the RF signals to the safety of public at unmanned level crossing. Instead of SOC, microcontroller can be used, but SOC is designed specifically to govern and easily synchronize with RF Transceiver. An RF transceiver is mounted on the top of the Train, and another transceiver mounted at the unmanned level crossing. The figure (1) illustrate the proposed system.

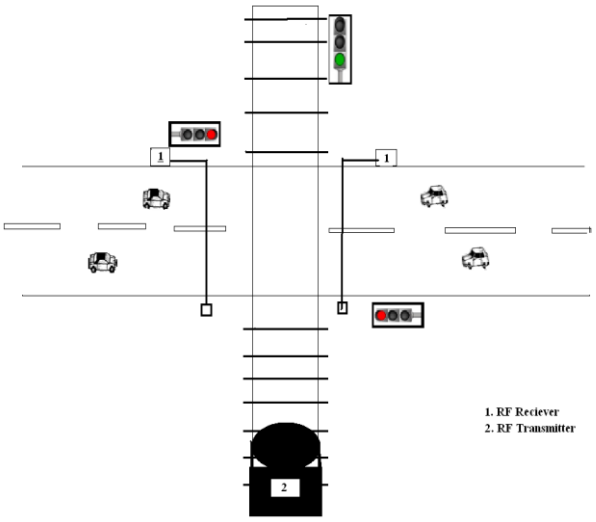

Figure 1 - Proposed system for the design of SOC with RF Transceiver.

Whenever the train arrives towards level crossing 15 Km ahead, the RF transmitter transmits the RF signal contains information bits to the receiver. Upon receiving the RF signal, SOC provides the warning signal to the Road crosser and this can also be used to activate the electromechanical system to close the gate. The gate will be open after the train was crossed the road. In the lab a prototype module was designed with a short distance RF module. In designing of SOC, FPGA architecture was chosen[7,10], because of its features like embedded hardware multipliers, increased number of memory blocks, massive parallelism capabilities, multimillion gate counts, and special low power packages can reduce the amount of memory used, computational complexity and power consumption. This paper has been organized as 1.FPGA micro Architecture, 2. Interfacing RF transceiver 3. Interfacing of Gear motor assembly, 4. Functioning of the circuit diagram, 5. Result and Discussion and 6. conclusion.

II. FPGA AN OVERVIEW

A field-programmable gate array (FPGA) is an integrated circuit. It is designed to be configured by the designer after manufacturing, hence it is field-programmable. The FPGA configuration is generally specified using a hardware description language (HDLs), such as VHDL and Verilog HDL. FPGAs can be used to implement any logical function that an ASIC (Application

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Specific Integrated Circuits) could perform. FPGA has the ability to update the functionality after transformation, partial re-configuration of a portion of the design [11] also possible and it is low cost.

In FPGAs programmable logic components are readily available known as logic blocks, and a hierarchy of reconfigurable interconnects that allow the blocks to be connected together. Logic blocks can be configured to perform any complex combinational/ Sequential functions, or merely simple logic gates like AND, OR, NOT and XOR. In most of the FPGAs, the logic blocks also consists memory elements, which may be simple one bit storage or more complete blocks of memory.

In addition to digital functions, some FPGAs have analog functions. The most common analog function is programmable slew rate and drive strength on each output pin. Another relatively common analog function is differential comparators on input pins designed to be connected to differential signaling channels. Some of mixed signal FPGAs have integrated Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs) with analog signal conditioning blocks allowing them to operate as a system-on-a-chip. In the year 2010, an extensible processing platform was introduced for FPGAs that fused features of an ARM high-end microcontroller with an FPGA IC to make FPGAs easier for designing embedded system. By incorporating the ARM microcontroller based platform into a 28 nm FPGA family, the extensible processing platform enables system architects and embedded software developers to apply a combination of serial and parallel processing to address the challenges they face in designing today's embedded systems, which must meet ever-growing demands to perform highly complex functions. By allowing them to design in a familiar ARM environment, embedded designers can benefit from the time-to-market advantages of an FPGA platform compared to more traditional design cycles associated with ASICs.[12][13][14].

2.1 FPGA micro Architecture Block Diagram

The FPGA micro Architecture Block Diagram with its functional blocks is shown in figure (2)

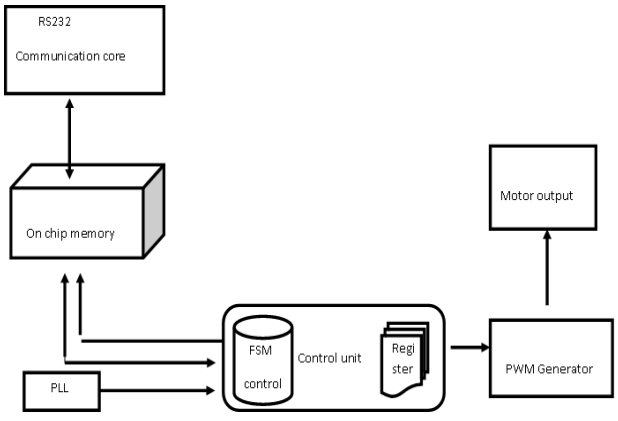

Figure 2 - The FPGA micro Architecture Block Diagram

In the FPGA micro architecture has the following functional blocks, listed below

- Finite State Machine (FSM)
- RS 232 core
- On-chip Memory Blocks
- PLL
- PWM Generator

2.2 Finite State Machine (FSM)

FSM plays a vital role in the design, has nine states (exclude RESET and END states) of action to be carried out while functioning. Such as

- Wait for RI (receiver interrupt signal)
- Read the data from RF receiver
- Forward to data processing unit
- Enable PWM signal generator unit for generate the pulse signal close the gate step by step
- Enable red signal and buzzer
- Wait for train pass information from RF transceiver
- After receive the signal enable the PWM signal open the gate
- Enable green state
- Go to first state

The figure (3) shows the state machine diagram as follows:

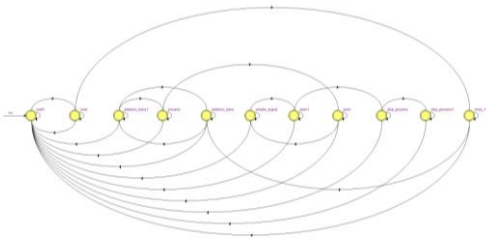

Figure 3 - State machine diagram

2.3 RS232 Core

In this functional unit the asynchronous communication is enabled. Whenever the RF Signal comes from the Transmitter, it receives and communicates with FSM at a speed of 9600 bits/sec. (baud). Figure (4) illustrates the RS-232 transmitter module

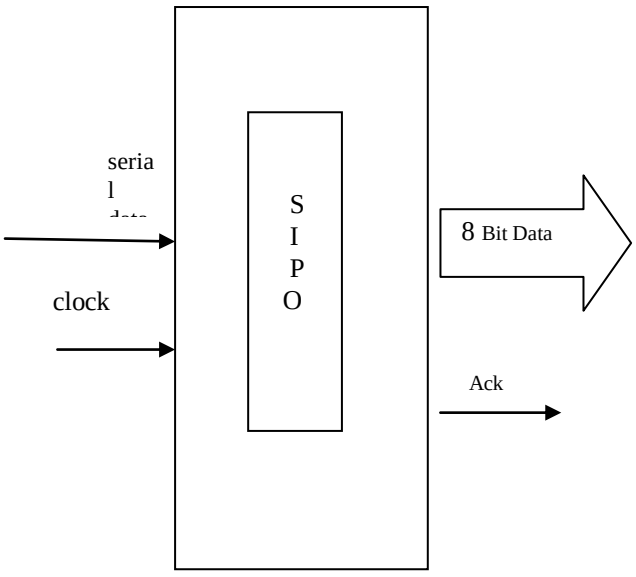

Figure 4 - RS-232 transmitter module

It works like that:

- The transmitter module takes an 8-bits data, and serializes it (starting when the "TxD_start" signal is asserted).
- The "busy" signal is asserted while a transmission occurs. The "TxD_start" signal is ignored during transmit time.

The RS-232 parameters used are fixed: 8-bits data, 2 stop bits, no-parity.

2.4 On-chip Memory Blocks

On-chip memory can be divided into number of blocks, based on the requirements. Our case, a data memory was created and used for storing of information, such as Train number, Crossed time.

2.5 Phase Lock Loops (PLL)

The PLL block provides general purpose clocking with clock synthesis and phase shifting as well as external outputs for high-speed differential I/O support The global clock network can provide clocks for all resources within the device, such as input/output elements (IOEs), FSM, and embedded memory blocks. The processor (FSM) was programmed to generate 9600 baud rate for RS232 core. The global clocking frequency is divided in the PLL. The simple calculation to get the baud rate as 9600 is

Global clocking frequency = 100MHz
PLL output = 100000000 / 2
= 50MHz
Desired frequency = 50MHz/9600
= 5208.33 Hz.

2.6 Remote System Upgrades

Remote system upgrade capability in Cyclone II [9] devices allows transformation of system upgrades from the remote location is possible. In order to upgrade the system, Soft logic either the Nios II embedded processor or user logic can be used in a Cyclone II device to download a new configuration image from a remote location. It stores the program coding in the configuration memory. The dedicated remote system upgrade circuitry initiates a reconfiguration cycle. The dedicated circuitry performs error detection during and after the configuration process. It means Cyclic Redundancy Check is possible. This check facilitates to recover from an error condition by reverting back to a safe configuration image, also provides error status information. This feature supports both in serial and parallel flash configuration.

III. INTERFACING RF MODULES

3.1 433 MHz RF Transmitter STT-433

It is low cost RF transmitter used widely in the wireless communication system. Its operating voltage ranges from 1.5 to 12V DC supply. The transmitter employs a SAW stabilized oscillator, which ensures accurate frequency control for the best range of performance. It is small size, consumes 11mA at 3V. Its minimum data rate 200 bps and maximum is 3K bps. Also it has good temperature adaptability (from -20 ^{o}C to + 60 ^{o}C).

3.2 433 MHz RF Receiver STR-433

The receiver module requires only antenna and no need of any external RF components. It is low cost device, whose operating voltage is 5V and the operating current is typically 3.5 mA and requires no external parts. Receiver frequency is about 433.92 MHz, whose sensitivity is -105dBm. Data received in the rate of 3 K bits/s.

IV. GEAR MOTOR ASSEMBLY

In our work, to open and close the gate NR-DC-ECO DC geared motor [15] is used. It is simple weightless device and easy to interface with SOC using driver circuit. The construction of the motor has the sophisticated technology. In the motor gears are fixed on hardened steel spindles. These spindles rotate between bronze plates which ensures noise free running. It is DC operated device able to work with 4 to 12 V, and its speed is 30 RPM.

V. FUNCTIONING OF THE SYSTEM MODEL

The core embedded system in FPGA works as the processor. It is used to control the communication device 433 MHz RF Receiver STR-433. RF transmitter mounted on the top of the train emits series of the bit packets containing the information about the train to be crossed. Upon the receiving RF data packets, processor save the information about the train, the time to be crossed and enables the buzzer to give the warning level crosser. Also it activates the motor to close the gate. After the train crossed over place, it stops the buzzer and run the motor in the reverse direction to open the gate. In the laboratory a prototype system was implemented successfully with RF transceiver and gear motor.

VI. RESULT AND DISCUSSION

The working model developed in the laboratory produced the output shown in the figure(5). It is the synthesized RTL view of the functional blocks.

Figure 5 – Synthesize view of the Functional blocks.

Figure(6) shows the Chip planner view of the Functional blocks. It reveals that the number of logic elements used for the functional blocks of SOC are 90/32,216 (It is less than 1%). Other utilizations are

- Total combinational functions - 90/32,216 (< 1%)
- Dedicated logic registers - 55/32,216 (< 1%)
- Total registers - 55
- Total pins - 5/475 (1%)

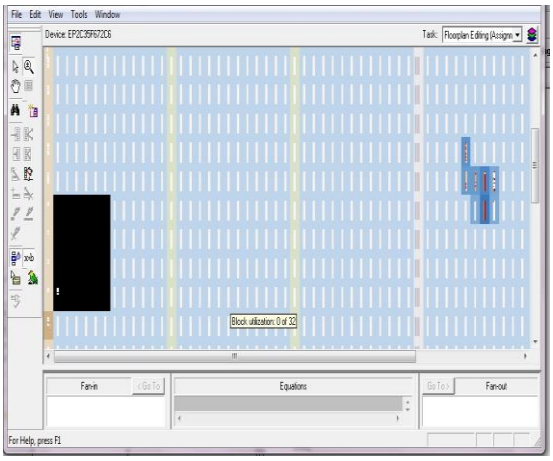

Figure 6 - Chip planer view of the Functional blocks

VII. CONCLUSION

In the laboratory a prototype system was implemented successfully with RF transceiver and gear motor. This work is more useful in railway level crossing management, as it is required to avoid the railway level crossing fatalities. Now railway level crossing fatalities are more common, in almost all countries. Design of SOC in FPGA for wireless communication system with RF transceiver embedded system, provides better wireless data transmission. It is low cost system architecture. But, if needed more such SOCs, we have to go for ASCI (Application Specific Integrated Circuits) based SOCs, because FPGA is most suitable for low volume of ICs. This project can be further developed and can be used for real time application. This prototype system was successfully implemented and tested in Altera cyclone II device EP2C35F672C6.

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