FPGA Implementation of Interference Avoidance and Hard To Intercept Frequency Agile Radar Processing

Tirumala Rao Pechetty, Raviteja Udumudi

Abstract: ***Jamming is one of the main problems for the functioning of the radar. Surveillance radar or searching radar has to overcome the jamming environment during the operation of the work. Jamming is of Diversified which includes narrow band, wide band jamming or its combination. Hence the solution for the Diversified jamming is obtained by using fast self switching frequency agility technique and its function is very effective. The detailed steps to achieve this function are described and the function is realized with FPGA using Hardware Description Language.The practical application on a surveillance radar shows that the module has good real time and anti jamming capacity. Modelsim will be used for functional simulation and results verification. Xilinx ISE will be used for synthesis; place & route and bit file generation. Xilinx FPGA board will be used for results verification.***

Keywords: Anti-jamming; Diversified jamming; Frequency agility; FPGA; Fast self switching frequencies; Interference; Self adaptive.

I. INTRODUCTION

Today RADARs are used both in military and civilian applications. In military applications RADARs play vital role in detecting the enemy aircrafts at larger distances. Jamming is a technique which is usually adopted to make a RADAR non functional. Hence a robust RADAR must be able to work even when there is jamming attach from enemy side. Many kinds of technology can be applied to modern pulse radar to meet diversified jamming; in a word, they all enhance useful echo signals and avoid or weaken interference signals in order to ensure the radar works properly to the maximum extent. Among so many anti-jamming technologies, frequency selection is widely used and also very effective. The common frequency selection method includes manual frequency modulation, frequency agility, frequency diversity, spread spectrum technology, etc. Fast self switching self adaptive frequency agility can adapt the changing of the jamming environment to a certain extent.

It analyzes jamming spectrum real time so that to control the radar transmission frequency, it make the radar signal spectrum centre locate at the weak part of the jam spectrum all the time, so as to improve the signal-interference ratio. Fast self switching frequency agility can not only deal with narrow ban aiming jam, but also control wide band block jam to a certain extent. Fast self switching frequency agility is mainly implemented by Jamming Analysis Transmission Selection (JATS). JATS was realized on a DSP chip of TMS320C25 in [8] and on a micro control unit (MCU) in [5], and is developed with FPGA in this paper. The implementation with FPGA has many merits [4], the most important of all is that FPGA can get good real time capacity, thus achieving the real frequency agility. The JATS module using FPGA is applied to perimeter surveillance radar.

II. IMPLEMENATION

In Jamming section we have Narrow band jamming and wide band jamming and also its combination also. Radar jamming refers to radio frequency signals originating from sources outside the radar, transmitting in the radar's frequency and there by masking targets of interest. Jamming may be intentional, as with an electronic warfare (EW) tactic, or unintentional, as with friendly forces operating equipment that transmits using the same frequency range. Jamming is considered an active interference source, since it is initiated by elements outside the radar and in general unrelated to the radar signals.

A. Narrow band jamming

Narrowband jamming is aiming at a communication channel. Jamming signal's frequency is the same as normal signal's frequency. Narrowband jamming use narrowband Gaussian process and it can be described as

$$j(t) = U(t) \times \cos[\omega t + \varphi(t)] \quad (1)$$

Where U(t) obeys Raleigh distribution, φ(t) phase function uniform distribution and independent with U(t) , ω is carrier frequency and it is greater than the spectrum of .Jamming power and jamming frequency are the decision factors of narrowband jamming in [14]. The jamming process is to get radar's work frequency firstly, then copy this frequency and modulate narrowband jamming signal, enlarges and launches this signal.

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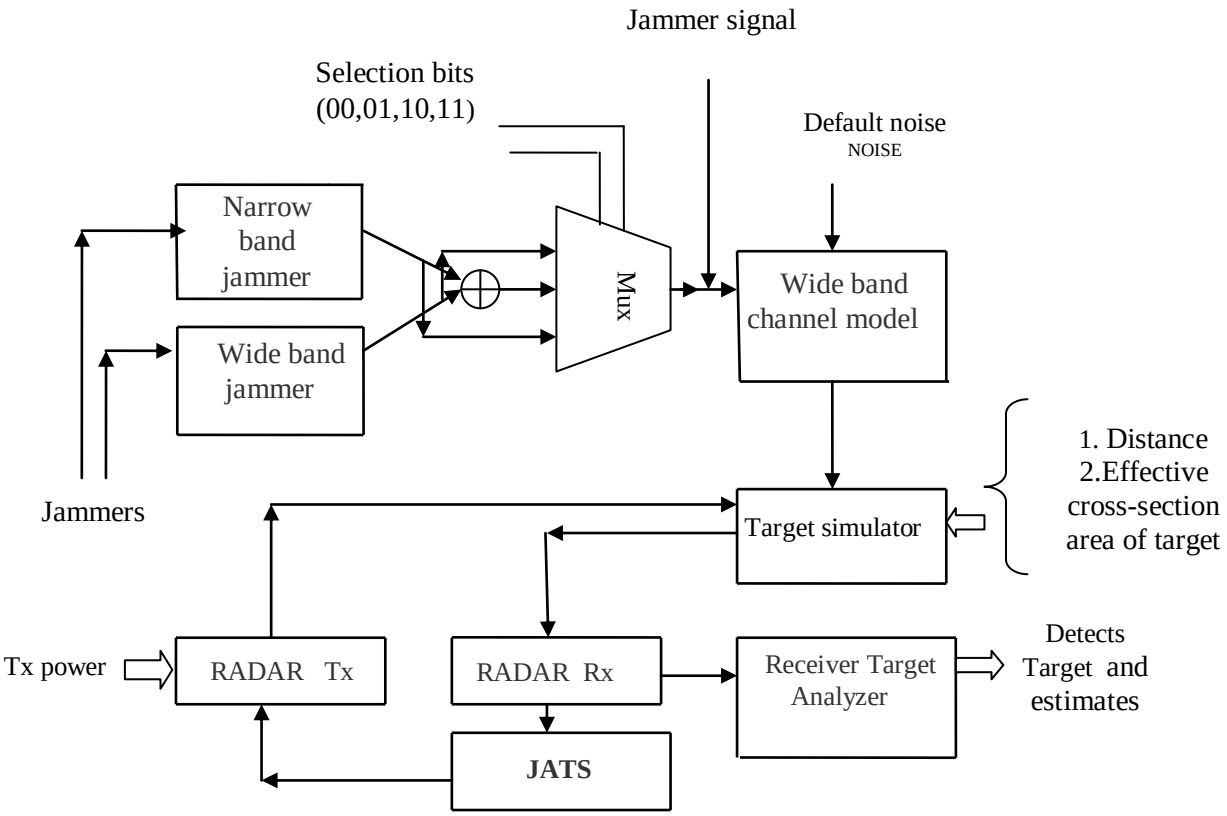

Figure 1. Frequency Agile RADAR block diagram

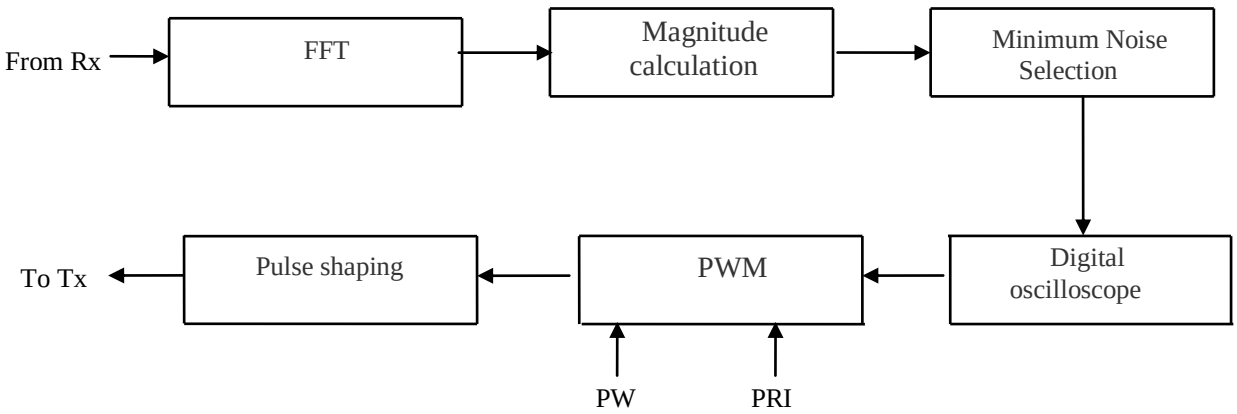

Figure 2. Jamming analysis and transmission selection

B. Wideband jamming

Wideband jamming is a common form of jamming. It adds jamming energy to the whole spectrum bandwidth of the signal. The determined parameters are jamming power in [8]. Wideband jamming is usually generated by Gaussian white noise and it probability distribution can be expressed as

$$f(x) = \frac{1}{\sqrt{2\prod}\sigma} \exp(-\frac{x^2}{\sigma^2}) \quad (2)$$

Where x is noise amplitude, σ is noise standard deviation.

The jammer section will generate four different types of noises and that noise signal is added to the radar signal. The types of noises are the wide band noise, the narrow band noise and the combination of above two. Here we take a jamming bit selector with two bit selection to generate one of the four different noises(00,01,10,11) from the jamming section.

In vhdl implementation narrow band and wide band noise signals are generated using randn look up table, of that cosine signal is attached using NCO (Numerically controlled oscillator).

To the jammer noise by default channel noise is added i.e. Additive white Gaussian noise.

C. Additive white Gaussian noise

The AWGN channel is represented by a series of outputs at discrete time event index i in [16]. Y_i is the sum of the input X_i and noise, Z_i, where, Z_i is independent and identically distributed and drawn from a zero-mean normal distribution with variance n (the noise). The Z_i are further assumed to not be correlated with the X_i in [10]

$$Z_i \approx N(0,n) \quad (3)$$

$$Y_i = X_i + Z_i \quad (4)$$

Additive white Gaussian noise is generated using randn look up table

Of these jammer noises, one is selected through multiplexer along with it default noise channel is added and given to Target simulator.

III. TARGET SIMULATOR

In target simulator the radar signal and jamming signal combined signal will detect the target distance and the cross section area of the target in [1].

Radar cross section of the target is denoted by σ and is given by σ

$$\sigma = \frac{power\ reflected\ toward\ source/unit\ solid\ angle}{incident\ power\ density/4\Pi}$$

$$\sigma = 4\prod R^2 \frac{|E_r|^2}{|E_i|^2} \quad (5)$$

Where R is the range to the target, Er is the electric field strength of the echo signal back at the radar and Ei is the electric field strength incident on the target in [1]. The echo signal will move to the radar receiver. As the noise is more than that of original signal frequency, the noise over comes the echo signal from the target, so the radar did not detect of the Target. The echo signal will move to the radar receiver. In the radar receiver the JATS will be processed.

In JATS the echo signal will processed by the FFT algorithm and find the magnitude spectrum from it will select the minimum frequency value and it shifts the radar signal to that minimum frequency. From this the radar signal can overcomes the jamming signal. This is the process of selecting minimum noise frequency and hence fast self switching frequency is achieved and implement by using hardware FPGA.

In Vhdl implementation, entity inputs are radar signal with noise, channel noise. Radar signal with noise and added channel noise, totally it is channel out in entity output, this is given to target simulator.

A. Fast fourier transform

The Fourier transform defines a relationship between a signal in the time domain and its representation in the frequency domain. Being a transform, no information is created or lost in the process, so the original signal can be recovered from knowing the Fourier transform, and vice versa in [17].The Fourier transform of a signal is a continuous complex valued signal capable of representing real valued or complex valued continuous time signals. Output of fft is given to magnitude calculation.

From the definition of DFT of size N:

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{nk} \quad (6) \qquad 0 \le k \le N$$

Where $W_N = e^{\frac{-j2\Pi}{N}}$

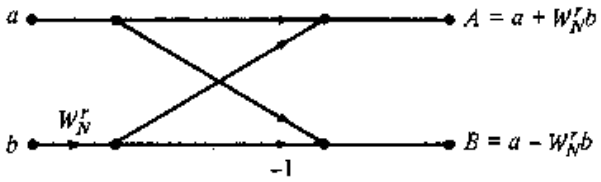

Figure 3. Basic butterfly structure

In Vhdl implementation 64 bit fast Fourier transform generation is done using Xilinx IP.

B. Magnitude Calculation

The tool allows you to view these complex valued signals as either their real and quadrature (also known as imaginary) components separately, or by a magnitude and phase representation. You may switch between these two representations at any point. Mathematically switching between the two representations for a given complex value can be expressed as

$$|X| = \sqrt{X_r^{\,2} + Y_i^{\,2}} \quad (7)$$

$$\angle X = \tan^{-1}\left(\frac{X_i}{X_r}\right) \quad (8)$$

Equivalently,

$$X_r = |X|\cos(\angle X) \quad (9)$$

$$X_r = |X|\sin(\angle X) \quad (10)$$

where $|X|$ and $|Y|$ are the magnitude and phase of the complex number, and Xr and Xi are the real and quadrature components of the complex number.

Magnitude calculation is assigned as sq_mag_out in vhdl language.

The function is sq_mag <= sq_re + sq_im;

In JATS the vhdl implementation finds out fft_max_code (maximum magnitude index) and fft_min_code (minimum magnitude index) for frequency selection.

IV. DIGITAL OSCILLOSCOPE

The digital storage oscilloscope [DSO] is now preferred type for most industrial applications. It replaces the unreliable storage method used in analog storage scopes with digital memory, which can store data as long as required without degradation. It allows complex processing of the signal by high-speed digital signal processing circuits in [3].

V. DIRECT DIGITAL SYNTHESIZER(DDS)

Direct digital synthesis (DDS) is a method of producing an analog waveform usually a sine wave by generating a time-varying signal in digital form and then performing a digital-to-analog conversion. Because operations within a DDS device are primarily digital, it can offer fast switching between output frequencies, fine frequency resolution, and operation over a broad

spectrum of frequencies in [17].

VI. PULSE WIDTH MODULATION(PWM)

Pulse-width modulation (PWM), or pulse-duration modulation (PDM**)**, is a commonly used technique for controlling power to inertial electrical devices, made practical by modern electronic power switches.

The main advantage of PWM is that power loss in the switching devices is very low. When a switch is off there is practically no current, and when it is on, there is almost no voltage drop across the switch. Power loss, being the product of voltage and current, is thus in both cases close to zero. PWM also works well with digital controls, which, because of their on/off nature, can easily set the needed duty cycle in [15].

Modelsim will be used for functional simulation and results verification. Xilinx ISE will be used for synthesis, place & route and bit file generation. Xilinx FPGA board will be used for results verification. Synthesis report is also displayed which tells device utilization parameters and timing summary. Device utilization parameters consists of percentage utilization

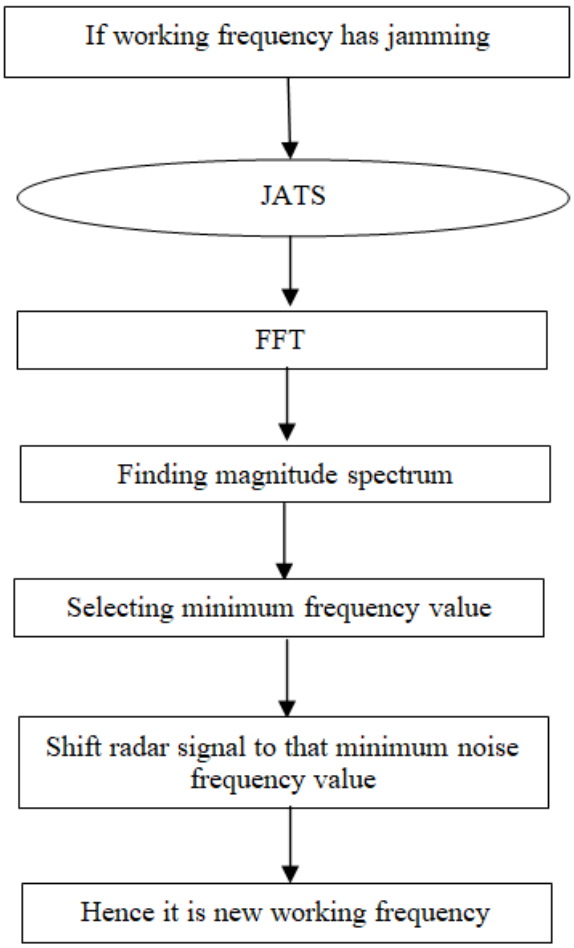

Figure 4. Jamming analysis flow chart

Simulation results

of flips flops, LUT table, i/o blocks, Rams etc. In timing summary we see delays, maximum output time after clock, minimum input arrival time before clock, maximum combinational path delay. The simulation result of the architecture with various parameters taken i.e. Jammer bits (0,1) which means narrowband jamming noise and also channel noise is added to the radar signal. This forwarded to JATS for the fft to perform and to give max code and min code. In fig.4 Min code (minimum magnitude index) corresponds to low noise frequency, its value is 24 and max code (maximum magnitude index) is 23 where noise is more. So, to this corresponding min code frequency value the radar signal is switched. Hence jamming is avoided. And also target distance is also found at 1158. In this way jamming frequency is avoided through switching and also target distance is found out. Target distance estimation value is seen. Echo found indication is given through 0 or 1. If 0 then echo not found and if 1 then echo found, therefore various parameters are observed.

VII. REALIZATION WITH FPGA

In this project an architecture to achieve self switching type agile RADAR is realized with FPGA using Hardware Description Language (VHDL) , the validity is proved by suitable test signals. The self-adaptive frequency agility module can analyze the type of jamming to select transmitting frequency to avoid the frequencies which have interference, under frequency diversity and fixed frequency, respectively. The high level blocks include jamming analysis, monitor control and receiver. We use Xilinx real time pipelined FFT core for spectrum estimation block.

VIII. SYNTHESIS RESULT

In the synthesis result we will get device utilization summary and timing summary.

In the device utilization summary, selected device is Vertex 4-vlx15sf363-12. Number of slices used for the project is 14%. Number of slice flip flops used is only 3%. Number of 4 input LUTS is 12%, Number of input, outputs used is 23. The percentage utilization shows that very fast processing is done. Hence speed factor is very importantly considered. In timing summary we see minimum period 3.703ns. Maximum output required time after clock is 7.521ns. which is in terms of nano-seconds hence very short time utilization.

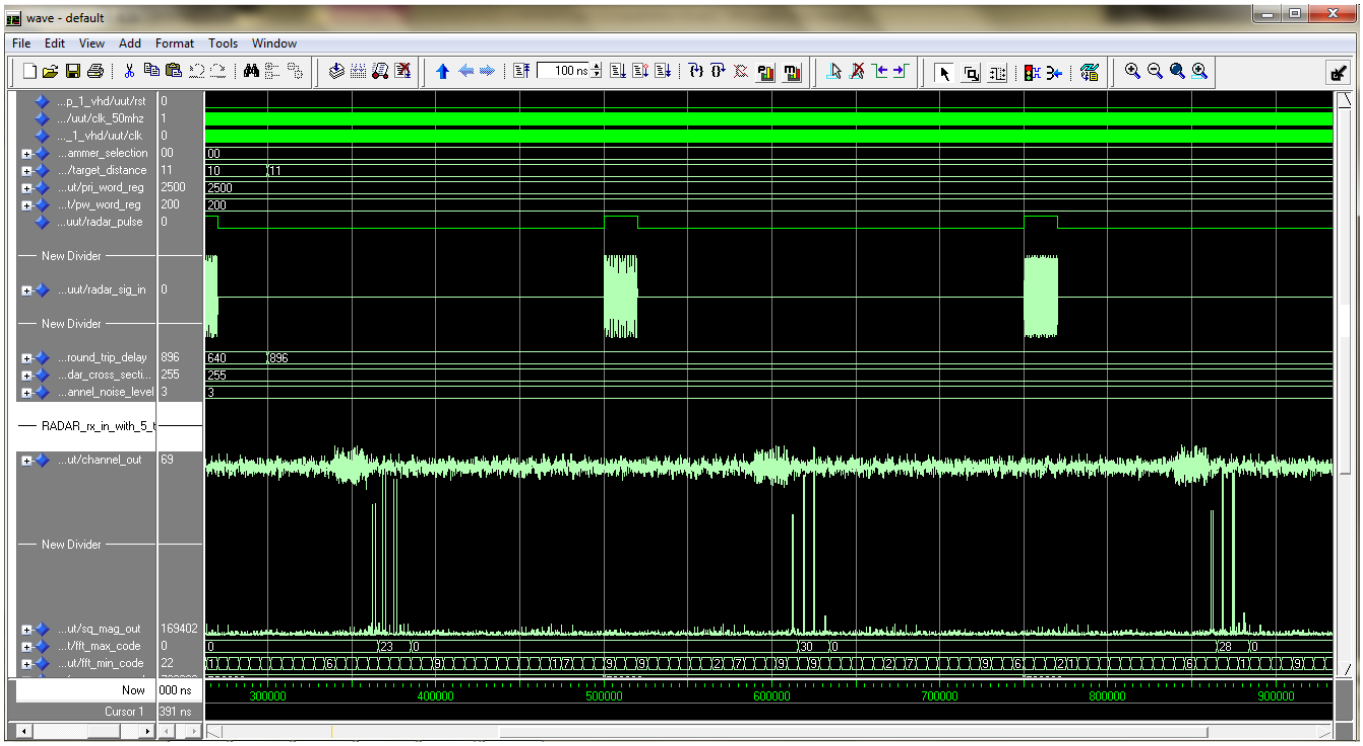

Figure 5. Simulation of upper part consists of radar pulse, jammer selection, clock, channel noise

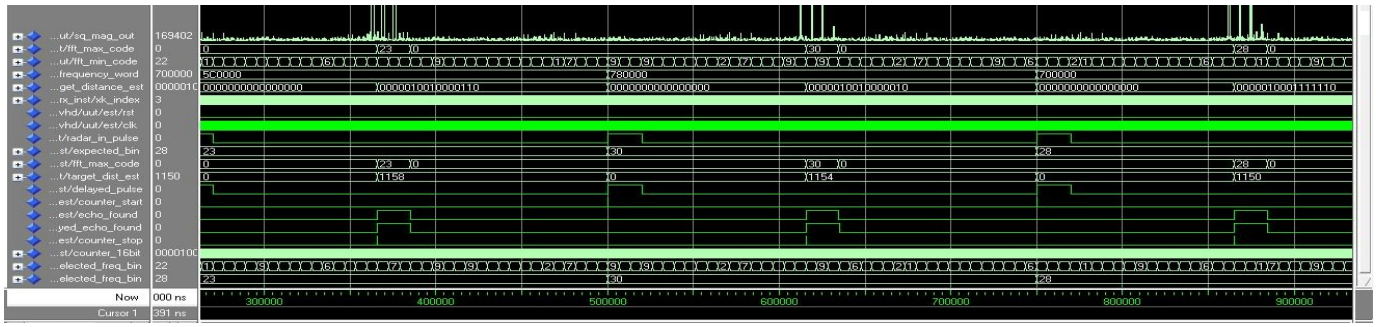

Figure 6. The lower part consists of fft max and min values, distance values

IX. CONCLUSION

Anti-jamming is an issue that must be resolved on searching radar or surveillance radar. In this paper, the jamming analysis and transmission selection module is performed under fixed frequency mode and frequency diversity mode, detailed working flow is discussed, the key steps are considered, and the function is applied to Xilinx Spartan 3E board. The frequency analysis result displays on the monitor and control terminal, which is clear at a glance. During practical application, this module acquires satisfactory real time anti-jamming effects.

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