A Study and Analysis of High Speed Adders in Power-Constrained Environment

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Abstract: An overview of the performance of 1-bit full adder in different CMOS logic styles and in depth examination of the advantages and limitations of each of them with respect of speed and power dissipation are presented. Ten 1-bit full adder circuit based on these logic styles are chosen for the extensive evaluation. These circuits were redesigned at the transistor-level in tsmc 0.18 µm technology and comparison reported here uses Mentor Graphics ELDO simulations to assess their performance. The hybrid full adder exhibits not only the full swing logic and balanced outputs but also strong output drivability. The work presented in this paper gives a quantitative comparison of the adder cell performance.

Index Terms: Full Adder, logic devices, High-speed, Very large-scale integrated (VLSI) circuit.

I. INTRODUCTION

Today, there is an increasing number of portable applications requiring small-area low-power high-throughput circuitry. Therefore, circuits with low power consumption become the major candidates for design of microprocessors and system- components. The battery technology does not advance at the same rate as the microelectronics technology and there is a limited amount of power available for the mobile systems. The goal of extending the battery life span of portable electronics is to reduce the energy consumed per arithmetic operation, but low power consumption does not necessarily imply low energy. To execute an arithmetic operation, a circuit can consume very low power by clocking at extremely low frequency but it may take a very long time to complete the operation. Therefore, designers are faced with more constraints such as high speed, high throughput, small silicon area and at the same time low power consumption. This is why building low- power, high-performance adder cells is of great interest.

Addition is one of the fundamental arithmetic operations and is used extensively in many VLSI systems. In addition to its main task, which is adding two binary numbers, it is the nucleus of many other useful operations such as subtraction, multiplication, division, addresses calculation, etc [1, 2].

In most of these systems, the adder is part of the critical path that determines the overall performance of the system and the full adder is the core element of complex arithmetic circuits. That is why enhancing the performance of the 1-bit full-adder cell (the building block of the binary adder) is considered a significant goal.

We consider ten different adders redesigned at transistor level in tsmc 0.18 µm technology and testedseparately. The adders are characterized in terms of delay, power dissipation, and voltage scalability. The power-delay product (PDP) represents a trade- off to be optimized between two conflicting criteria of power dissipation and circuit latency in transistor sizing.

The Hybrid Full Adder is proven to have the minimum power consumption and less power delay product by *Mentor Graphics ELDO* simulation. Comparing with others, the characteristics of the Hybrid full adder shows balanced outputs, making it easy for large tree structured arithmetic circuits to maximize area efficiency without unduly degrading the VLSI power and delay signal. Due to the minimum time delay of carry out, the adder core greatly improves the overall performance for a large scale of multi-bit adder.

The rest of paper is organized as followings. Section II explores the full adder designs in different logic styles. Section III describes the design of hybrid CMOS full adder. Section IV the circuits are simulated for power, delay and power-delay product performances and the results are analysed and compared.. Finally, a brief conclusion is given.

II. REVIEW OF FULL-ADDER DESIGNS

The full adder can be described as follows: Given the three 1-bit inputs A, B, $C_{in,}$ it is desired tocalculate the two 1-bit output sum and $C_{out,}$ where

$$\text{Sum} = ABCin + \overline{Carry}\ (A + B + C_{in}) \quad (1)$$

$$C_{out} = AB + (A + B)\ C_{in} \quad (2)$$

The most significant one-bit full adders suitable for low power dissipation and/or high performance are briefly reported in this section.

The complementary CMOS full adder(C-CMOS) [2,6]as shown in Fig. 1(a) is based on a regular CMOS structure with conventional pull-up and pull-down transistors and has 28 transistors. The input capacitance of a static CMOS gate is large because each input is connected to the gate of at least a PMOS and an NMOS device. The series transistors in the output stage form a weak driver. Therefore, additional buffers at the last stage are required to provide the necessary driving power to the cascaded cells. The advantage of complementary CMOS style is its robustness against voltage scaling and transistor sizing.

The Dynamic Domino [13, 15] circuits operate using a sequence of pre-charge and evaluation phases orchestrated by the system clock signal as in

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fig. 1(b). Domino gates are faster than their complementary CMOS counterparts but, on the other hand, they are more susceptible to input noise [6]. This is due to the leakage currents flowing through the PDN , which can cause an unwanted discharging of the dynamic node. To counteract this effect, a feedback PMOS transistor (the so-called keeper) is exploited [7]. Dynamic domino gates have the severe limitation of not being able to implement inverting logic functions (such as NOR, NAND, XOR) and high power consumption due to clock.

The Data Driven Dynamic logic (D3L) [13] uses a subset of the input data signals to generate precharge-evaluate operation, thus avoiding the clock distribution network as shown in fig. 1(c).The main drawback of the D3L implementation (take example of XOR gate) is the presence of the two series-connected PMOS transistors that have to be sufficiently wide to make the pre-charge phase fast enough. Wide transistors make the input capacitances large, which in turn increase the evaluation delay and the dynamic energy consumption.

The split-path data-driven dynamic logic (SP3DL) [3,16] split the PDN of the generic gate into m evaluation sub-networks: one for each product sub function as shown in fig. 1(d). In this way, the number of series-connected devices in the pre-charging PUN and the gate input capacitances are minimised. As a further advantage, the split of the PUN (PDN) also causes the split of the parasitic capacitance of the dynamic node, thus increasing the gate speed. The dynamic energy consumption can be further reduced using smaller keeper transistors.

The complementary pass transistor logic (CPL) [2,8] full adder with swing restoration is shown in Fig. 1(e). Its dual-rail structure uses 32 transistors. The basic difference between the pass-transistor logic and the complementary CMOS logic styles is that the source side of the pass logic transistor network is connected to some input signals instead of the power lines [7]. The advantage is that one pass-transistor network (either pMOS or nMOS) is sufficient to implement the logic function, which results in smaller number of transistors and smaller input load. However, pass-transistor logic has an inherent threshold voltage drop problem. The output is a weak logic “1” when “1” is passed through anMOS and is a weak logic “0” when “0” is passed through a pMOS. Therefore, output inverters are also used to ensure the drivability. CPL is not an appropriate choice for low power due to its high switching activity of intermediate nodes, high transistor count and overloading of its inputs.

A transmission- gate adder (TGA) [2] using CMOS transmission gates is shown in Fig. 1(f). It uses complimentary properties of nMOS and pMOS transistor and has 20 transistors. It is built by connecting a pMOS transistor and an MOS transistor in parallel, which are controlled bycomplementary control signals. Both the pMOS and nMOS transistors will provide the path to the input logic “1” or “0,” respectively, when they are turned on simultaneously. Thus, there is no voltage drop problem whether the 1 or the 0 is passed through it. The main disadvantage of transmission gate logic is that it requires double the number of transistors of the standard pass-transistor logic or more to implement the same circuit.

A transmission function full adder (TFA) [2,12] based on the transmission function theory is shown in Fig. 1(g). Its design based on transmission function theory and has 16 transistors.

The main disadvantage of TGA and TFA logic styles is that they lack driving capability. When TGA or TFA are cascaded, their performance degrades significantly.

14T in Fig. 1(i) [18] and 10T in Fig. 1(h) [10,11] use more than one logic style for their implementation and are called Hybrid logic design style. They generate A⊕ B and use it and its complement as a select signal to generate the outputs. They benefit from small transistor count and exploit the non-full swing pass transistors with swing restored transmission gate techniques. The problem that produces high capacitance values for the inputs is less clear in these designs. 14T is low power implementation and it is worth mentioning that TGA, TFA, 10T and 14T have lower loading of the inputs and intermediate nodes, lower-transistor count and balanced generation of SUM and C_{out} signals.

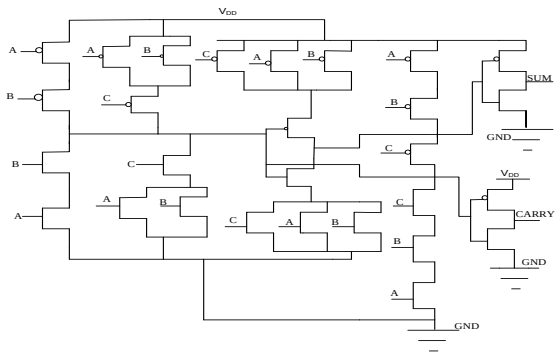


Figure 1(a): Complimentary-CMOS Adder

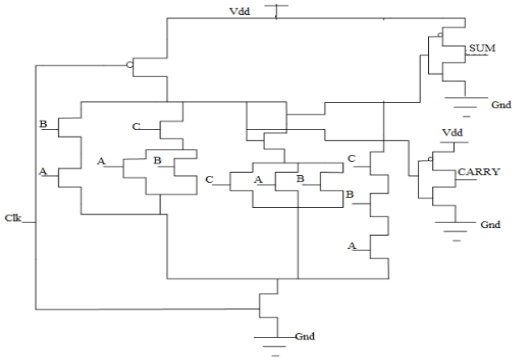


Figure 1(b): Dynamic Domino Adder

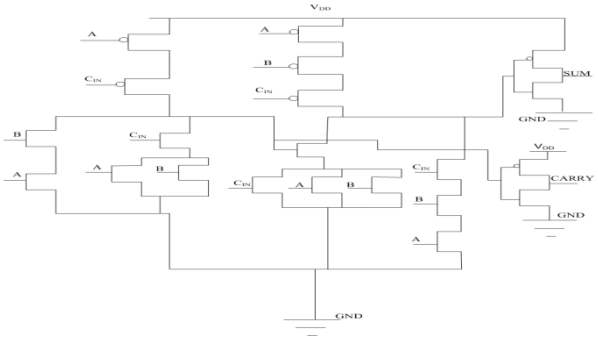


Figure 1(c): D3L Adder

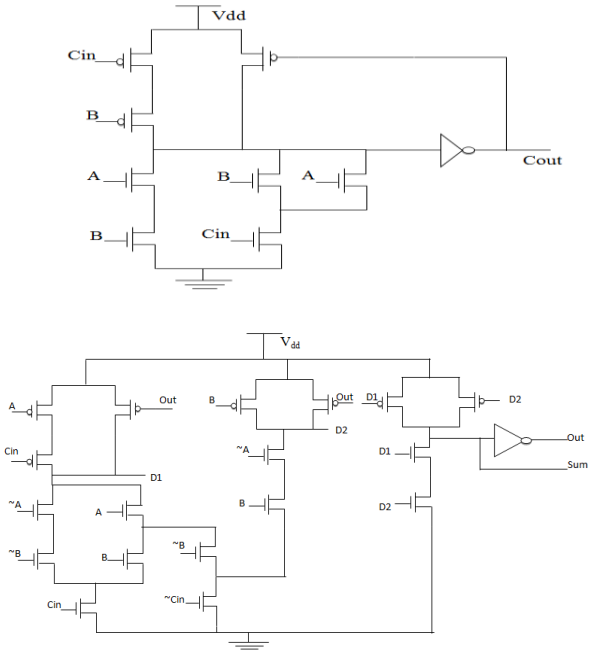


Figure 1(d): Split-path D3L Adder

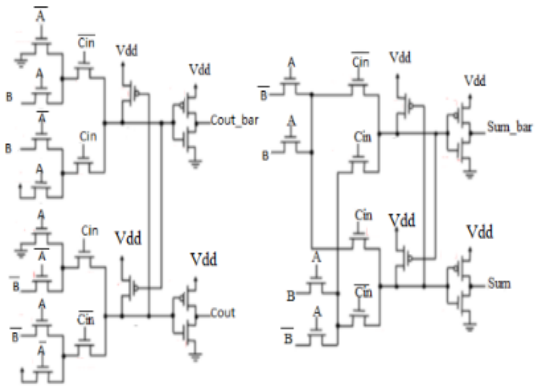


Figure 1(e):Complementary Pass Transistor Logic (CPL)

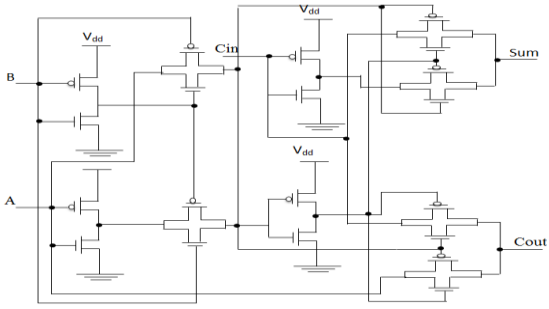


Figure 1(f):Transmission- Gate Adder (TGA)

III. HYBRID FULL ADDER

The hybrid full adder circuit can be decomposed and analyzed in three sub modules as in [2]. The logic expressions for the intermediate signals and outputs are given as follows:

Sum= A ⊕ B⊕C_{in}(3)

C_{out} = A.B + C_{in} A⊕ B. (4)

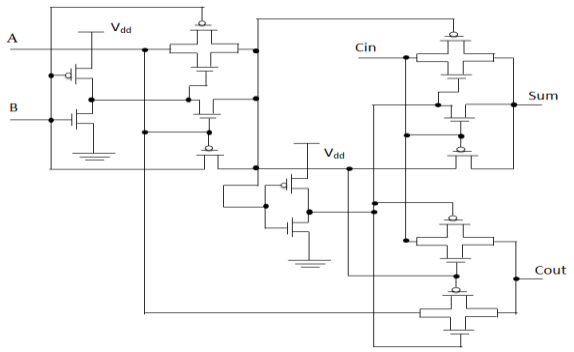


Figure 1(g):Transmission Function Full Adder (TFA)

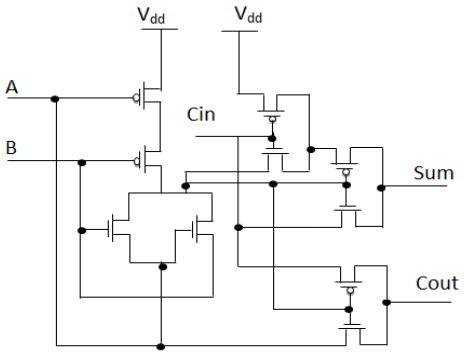


Figure 1(h):10T Adder

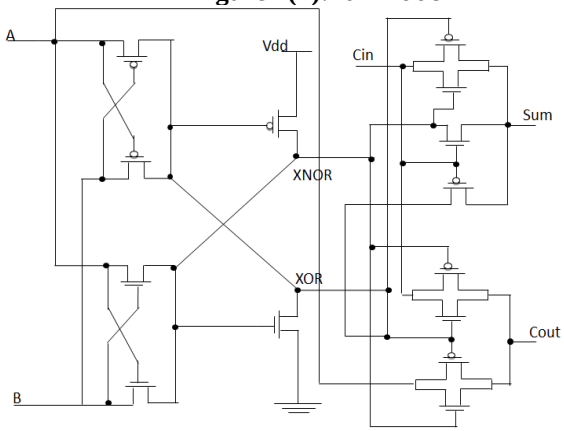


Figure 1(i):14T Adder

Module 1: XOR/XNOR

It use different sets of transistors to generate the XOR and XNOR functions separately To reduce the number of transistors, we use a similar pass transistor circuit as in [8] with only six transistors to generate the balanced XOR and XNOR functions, as shown in Fig. 2. Comparing with those designs that use an inverter to generate the complement signal, the switching speed is increased by eliminating the inverter from the critical path. The two complementary feedback transistors restore the weak logic caused by the pass transistors. They restore the non full-swing output by either pulling it up through pMOS to the power supply or down through nMOS to ground so that sufficient drive is provided to the successive modules.. However, this circuit suffers from the same threshold voltage drop problem as any other pass-transistor logic circuits. The worst-case delay happens at the transition from 01 to 00 for inputsAB .

Due to the unsatisfactory performance at low-supply voltage, we modified the circuit of Figure 2 by adding two series pMOS transistors to solve the worst-case delay problem of transition from 01 to 00 for . Two series nMOS transistors are added to solve the problem of transition from 10 to 11 for . When the state of 00 arrives, the XNOR output could obtain a strong "1" through two series pMOS pull-up transistors to the power supply, which avoid the high-impedance state as in the previous case. Similarly, the XOR output could obtain a strong "0" through two series nMOS pull-down transistors to ground when the state of transits to 11

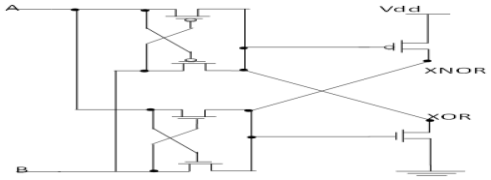


Figure 2: XOR-XNOR 6T gate

B. Module 2: XOR

Here we use a similar circuit as that of TFA and 14 T, but fully exploit the available XOR and XNOR outputs from Module 1 to allow only a single inverter to be attached at the last stage. The output inverter guarantees that sufficient drive is provided to the cascaded cell.

C. Module 3: MUX

The new circuit is based on complementary CMOS logic style, [6]. Its logic expression is given by equation (4). This circuit has inherited the advantages of complementary CMOS logic style, which has been proven in [2] to be superior in performance to all pass transistor logic styles for all logic gates except XOR at high supply voltage. Its robustness against voltage scaling and transistor sizing (high-noise margins) enables it to operate reliably at low voltage and arbitrary (even minimal) transistor size.

IV. SIMULATION RESULTS AND ANALYSIS

The investigation which includes the ten circuits C-CMOS, Dynamic Domino, D3L, sp-D3L, CPL, TFA,TGA,14T,10T and Hybrid full adder of Fig. 1 and Fig. 3has been based on simulation runs on Mentor Graphics ELDO by using a tsmc 0.18 µm technology. The supply voltage is 1.8V. By optimizing the transistor sizes of full adders considered, it is possible to reduce the delay of all adders without significantly increasing the power consumption, and transistor sizes can be set to achieve minimum PDP. All adders were designed with minimum transistor sizes initially and then simulated. Buffers are attached to the TFA, TGA, 14T and 10T circuits to enhance their driving capability.

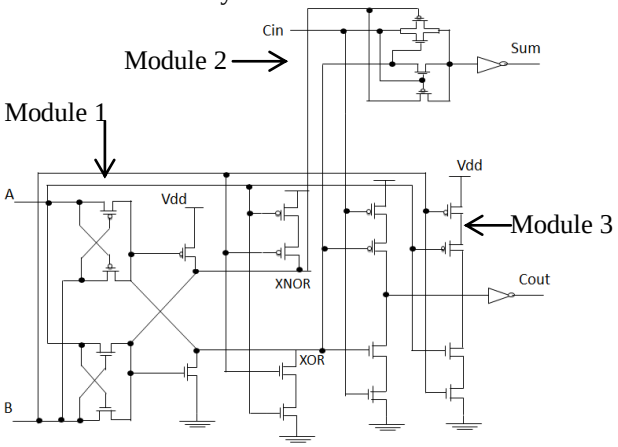


Figure 3: Hybrid full adder circuit.

The power, delay and power-delay product at supply voltage 1.8 V of hybrid, C-CMOS, Domino, D3L, sp-D3L, CPL, TFA, TGA, 14 T, 10 T are listed in Table I for comparison. Table II shows the power dissipation at the output of each full adder using different values of load capacitor. Table III shows the delay time for each full adder under different value of load capacitor. It is apparent that from the table I among the existing full adders, the C-CMOS full adder has the smallest delay.

The D3L implementation consumes less energy than the dynamic domino adder. However, this advantage is obtained at expense of the computational delay and the EDP. On the contrary sp-D3L adder shows higher power consumption then domino and D3L due to large number of individual paths between supply and ground. But overall EDP of sp-D3L is 13% and 3% is better than domino and D3L respectively.

It is clear that CPL adder consumes highest power, because of its dual-rail structure an d the substantial number of internal nodes. The additional inverters used to generate the complement inputs have also increased the power consumption. Hence the CPL topology should not be used when the primary target is low power consumption.

The smallest voltage that 10 T adder can work at 1.8V. The excessive power dissipation and long delay are attributed to the threshold voltage drop problem and the poor driving capability of some internal nodes at input combinations that create non full-swing transitions.

The speed of the 14 T decreases faster with supply voltage than other adder cells, so does its power-delay product. Because of the XOR/XNOR generation circuit of 14 T, it suffers from the same threshold voltage drop problem. The 14 T fails to function below 0.8 V.

The C-CMOS, TFA, TGA, CPL, and hybrid can work reliably at supply voltage as low as 0.8 V. Although TFA and TGA have lesser transistor count, due to the lack of drivability, additional buffers are required at each output, which increase their short-circuit power as well as switching power.

A load capacitance that was varied from 0 to 20 fF was placed at the output, and the worst case delay for each adder was observed. The 14T adder has the worst load versus delay characteristics for large capacitive loads. The 14T full adder dissipated lowest power compared to the other adders as its voltage swings ranged from 0 and V_{DD} - V_T and not between 0 and V_{DD}as seen in the TGA and CMOS adders.

Table I: Power, delay, Power-Delay Product of different adders in 0.18-µm technology

Adder type	Static power dissipation(P w)	Dynamic power dissipation(µ W)	Delay(P s)	Power-del ay product(PJ)
C-CMO S	103.930	10.935	102.780	1123.89
Domino	86.251	10.661	146.050	1557.030
D3L	181.300	7.2876	181.820	1385.040
Sp-D3L	214.241	12.510	107.872 5	1349.100
CPL	343.607	17.416	118.677 7	206.940
TGA	183.928	7.690	133.112	1023.715
TFA	185.821	4.937	149.210	736.726
10T	560.780	7.243	163.386	1143.41
14T	161.575	2.906	216.895	630.360
Hybrid	290.703	5.475	109.928	**601.860**

The PDP is quantitative measure of the efficiency of the trade-off between power dissipation and the speed, and is particularly important when low power operation is needed. Overall hybrid exhibits smaller power-delay-product than C-CMOS and works reliably at all voltage range especially at very low voltage. However, to generate Sum signal, the signal of C_{out} is used as one of the inputs, which causes the unbalanced outputs. These unbalanced outputs also lead to more spurious transitions to the cascaded stage.

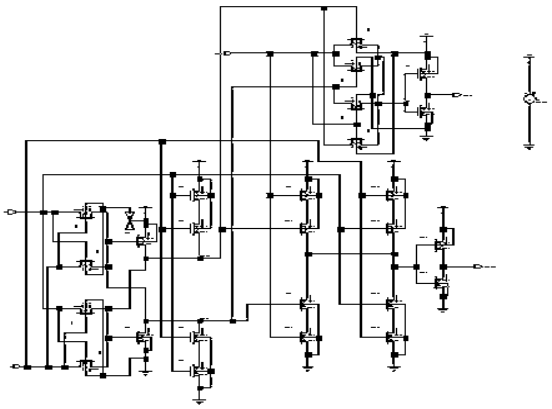
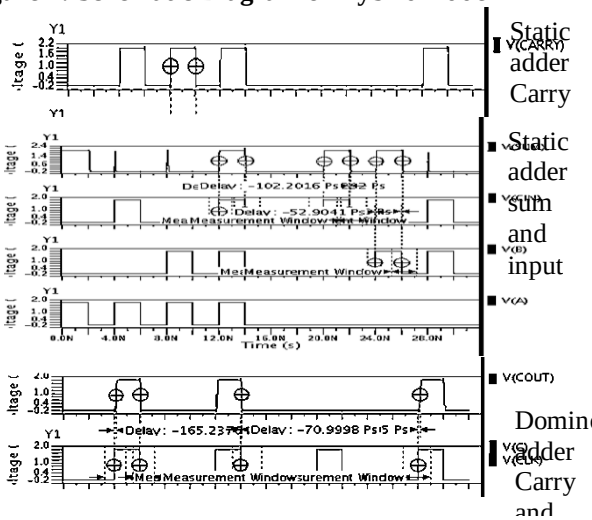


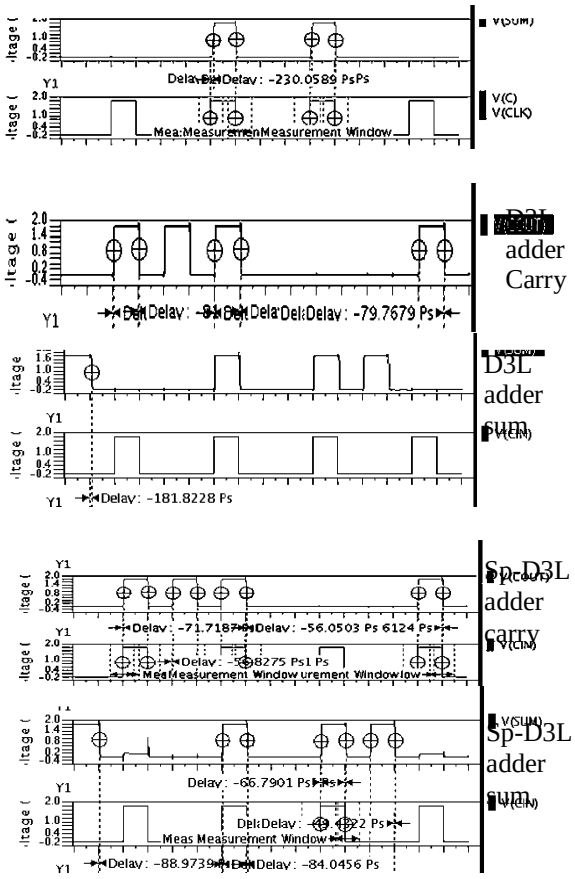
Figure 4: Schematic Diagram of Hybrid Adder



V. CONCLUSION

The quantitative overview of performance of the full adder cell has been presented. The investigation which includes the ten circuits C-CMOS, Dynamic domino, D3L, sp-D3L, CPL, TFA, TGA, 14T, 10T, Hybrid full adder of Fig. 1 and Fig. 3, has been based on simulation runs on Mentor Graphics ELDO environment by using a tsmc 0.18-mm technology. The supply voltage is 1.8V.

The hybrid full adder cell consisting of the XOR/XNOR, sum and carry out sub circuits, isdesign. The pass logic design style is used to efficiently generate the XOR and XNOR functions simultaneously and a good drivability carry out is generated by a complementary CMOS style circuit with regular layout. In addition, the last-stage inverter de-couples the output and input to improve the driving capability. Despite having higher transistor count than the recently reported designs, the hybrid circuit has shown to be highly energy efficient over a wide supply voltage range. The balanced sum and carry outputs also offer considerable flexibility in allocating the adder cells in tree structured circuit to eliminate as many cross-stage interconnections



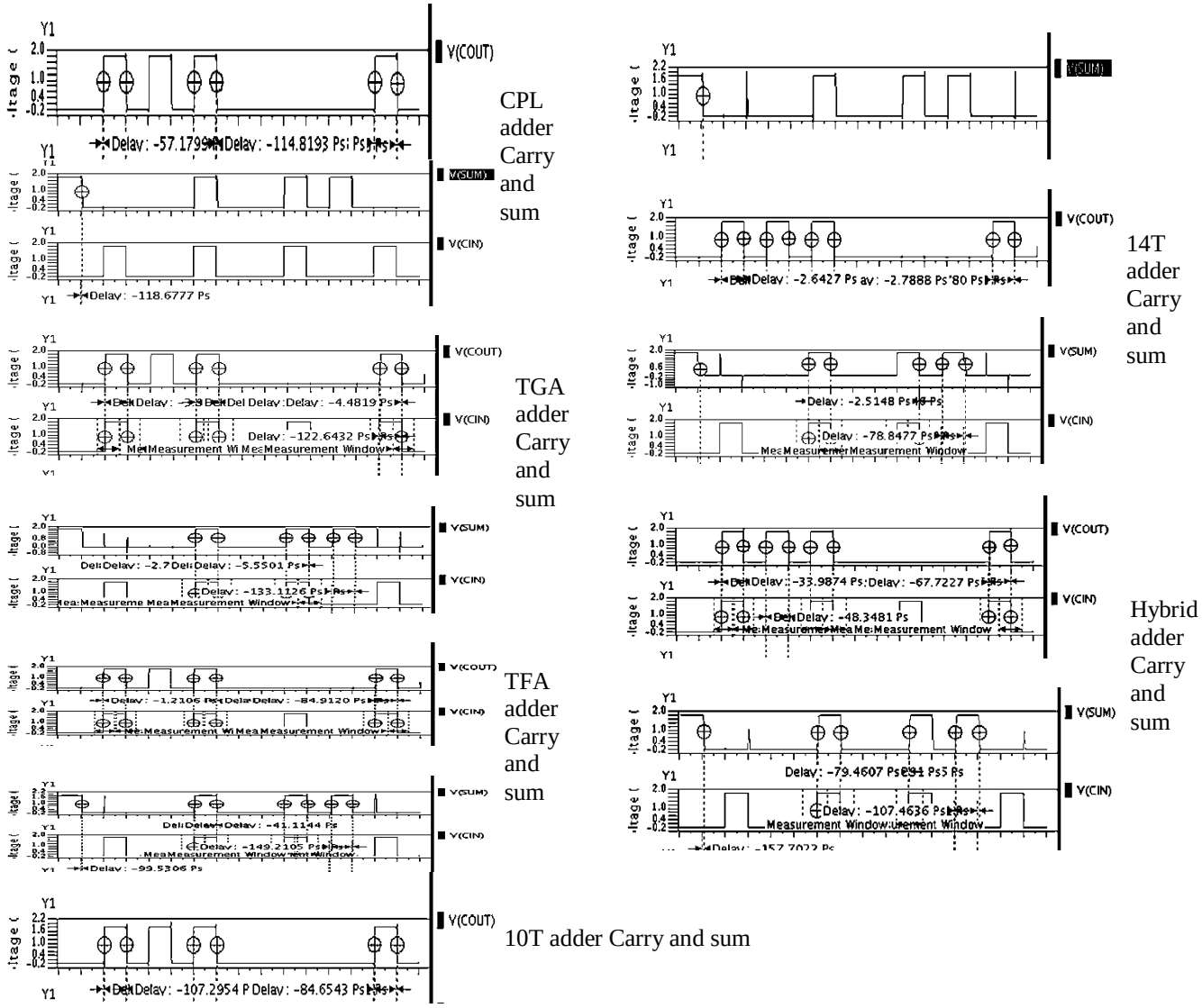


Figure.5: Comparison of output waveform of the adder cells

Table: II Dynamic Power Dissipation (µw) for each full adder in different value of load Capacitor

CL(fF)	C-CMOS	Domino	D3L	Sp-D3L	CPL	TGA	TFA	10T	14T	Hybrid
5	15.325	14.370	13.065	20.145	24.409	8.307	7.161	11.441	3.160	9.599
10	19.438	19.944	18.403	24.510	32.120	8.824	8.808	15.035	3.367	13.172
15	23.485	22.986	23.303	28.827	39.806	9.316	10.355	18.606	3.552	16.729
20	27.471	26.567	27.231	33.127	47.463	9.823	11.887	22.155	3.732	20.274

Table: III Delay for each full adder in different value of load Capacitor

CL(fF)	Delay type	C-CMOS	Domino	D3L	Sp-D3L	CPL	TGA	TFA	10T	14T	Hybrid
5	Rise time	69.131	*230.058*	145.110	142.955	129.347	166.332	187.647	136.448	130.720	107.463
	Fall time	102.789	*74.316*	222.913	147.108	147.508	118.586	140.933	163.384	201.792	157.702
10	Rise time	11.840	*302.574*	183.136	208.360	158.208	196.727	222.324	178.549	181.445	177.925
	Fall time	141.131	*98.325*	255.270	180.330	168.362	132.704	162.070	189.200	343.394	193.705
15	Rise time	136.167	*370.143*	218.050	274.54	184.251	225.849	257.819	217.692	229.059	225.966

	Fall time	164.658	*120.201*	285.517	208.360	186.609	145.943	183.353	215.241	393.790	227.489
20	Rise time	158.101	*434.830*	251.133	333.68	209.525	256.912	290.673	260.517	282.015	278.898
	Fall time	183.628	*145.369*	290.287	236.28	204.191	158.731	203.080	239.935	452.805	261.263

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