High Performance Simulator Analyzing the Efficient Cache Memory Simulation Behavior

Manoj Kumar Jain, Ravi Khatwal

Abstract*—High performance is the major concern in the area of VLSI Design. Cache memory consumes the half of total power in various systems. Thus, the architecture behavior of the cache governs both high performance and low power consumption. Simulator simulates cache memory design in various formats with help of various simulators like simple scalar, Xilinx etc. This paper explores the issue and consideration involved in designing efficient cache memory and we have discussed the cache memory simulation behavior on various simulators. Memory design concept is becoming dominant; memory level parallism is one of the critical issues concerning its performance. We have to propose high performance cache simulation behavior for performance improvement for future mobile processors design and customize mobile devices.

Keywords*— Application Specific Instruction Processors, Memory design, Simple scalar simulator, Xilinx, Micro wind, Top spice 8 Simulator etc.

I. INTRODUCTION

Memory unit is a collection of storage cells together with associated circuits needed to transfer information in and out of device. The time it takes to transfer information to or from any desired random location is always the same. The communication between a memory and its environment is achieved through data input and output lines and addresses selection lines that specify the direction of transfer. Memory levels are in the order of sequence in which information can be accessed. Various semiconductor memories have been designed for correct read/write operation. The goals of every memory system are to provide adequate storage capacity with acceptable level of performance. Cache is an essential component of high performance computers that aim to reduce latency period of various cache levels. The real benefit of cache memory is in storing the most frequently-used instructions. For low-power SRAMs, access time is comparable to a standard DRAM. In memory access method are to be used to reduce the waste element in memory or reduce cache misses in memory mapping approach. Memory needs comes from the requirement to hide the latency of accessing slower off chip memory. Simple scalar simulator is ideal for fast cache simulation if the effect of cache performance on execution time is not needed. The micro wind programs allow the design and simulate an integrated circuit at physical description level.

Top spice 8 is a native full-features mixed-mode, mixed-signal, and circuit, simulator capable of simulating circuits containing any arbitrary combination of analog device, digital function and high –level behavior blocks. Xilinx tool provide the access time of memory is the time required to select a word and read it. The cycle time of a memory is the time required to complete a write operation. The CPU must provide memory control signals in such a way so as to synchronize its internal clocked operations with the read and write operation of memory.

II. REALTED WORK

M.K. Jain et al. [1] proposed scheduler based technique for exploring register file size, number of register window and cache configuration in integrated manner. P. R. Panda, N.D. Dutt and A. Nicoulau [2] proposed scratch-pad memory architecture exploration for application specific designs processors and optimization technique for customize embedded system. Custom memory organisation can potentially and significant reduce the system cost and yield performance. Memory hierarchy is the bottleneck in modern embedded computer system as the gap between the speeds of the processors and the Memory continues growing large. X. Wang [6] design combined method for tuning two-level Memory hierarchy consider for energy consumption in embedded system. This kind of memory level hierarchy allows evaluating the instruction and data caches branches separately .S. Simon Wong and A E Gamal [7] used the 3-D integrated design for 3-D SRAM. FELI, [11] designed a set of operating system mechanisms that allocate application data to on-chip memories without any user Intervention. ELI, automatically maps data to on-chip memories using the address translation mechanism. It relies on a set of TLB counters, and dynamical migration of pages from off-chip memory to on-chip memory. We also introduce virtually tagged L0 caches to alleviate the address translation overhead. S. Petit et al. designed Petit et al designed Petit et al designed DRAM cell in embedded logic based technology (e-DRAM) and proposed a hybrid n-bit macro cell that implements one SRAM cell, and n-1 DRAM cells [13]. Liu et al. [10] designed 3-DRAM which can use high performance logic dies to implement DRAM peripheral circuits and consequently improve the speed and reduce silicon area. Most prior research on 3-D Processors –DRAM integration featured several conventional commodity 3-DRAM ram dies staked as main memory. And design 3-DRAM design for heterogeneous environment. That architecture cover more them one memory level within the entire computer hierarchy.

III. SRAM DESIGN

High performance SRAM cell superficially resembles a flip-flop [Fig.1]. A signal applied to address line by the address decoder select the cell for either read or write operation. Two data line which are used in complex way to transfer the data stored and its complement between the cell and the data drivers. 6 T CELL SRAM [Fig. 2]

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cell does not require refreshing unit. A couple of transistors is increased gradually, which in turn increases performance of SRAM cell.

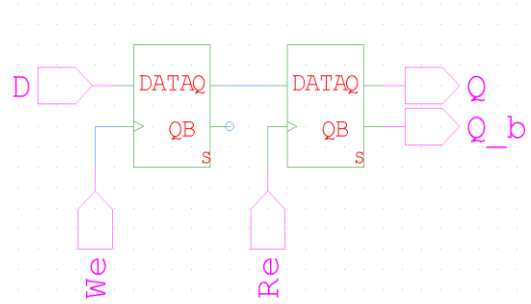

Figure 1. 1-bit SRAM Design

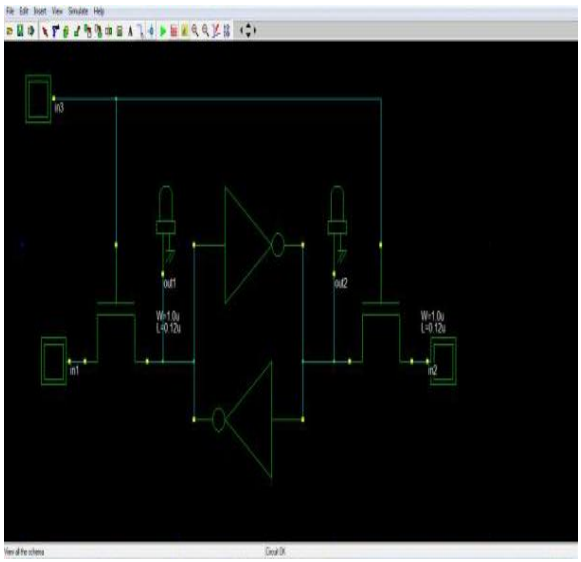

Figure 2 .design architecture of 6-T SRAM cell

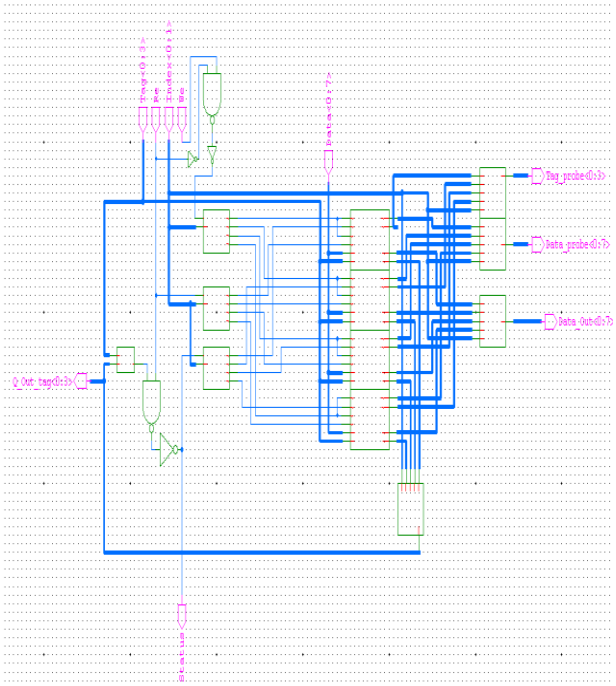

Figure 3. 12-bit cell design analysis

SRAM cell contain high transistor rate than DRAM but does not contain soft error removal mechanism. Higher quantity of transistors are used multi ported read /writes operation for excellent performance. Design tradeoffs include speed, volatility, cost, and features. All of these factors should be considered efficient cache RAM for our embedded system design. Each cache level contains tag and data part so we compare tag part and data are transfer from one cache level to another cache levels. (Fig. 3) shows the architecture level of various caches.

IV. MEMORY MAPPING IMPLEMENTATION ANALYZING WITH COMPARATOR TOOLS

Memory mapping implementation analyzing with the help of various comparator. In this case if two or more digits are equals, we compare the next lower significant pair of digits. This comparison continues until a pair of unequal digits is reached. If the corresponding digit of As 1 and that of B is 0. We conclude that A>B.If the corresponding digits of a is 0 and that of b is 1. We have been given A<B. The sequential comparison can be expressed logically by the Boolean functions.

$$(A>B)=A_3B_3'+X_3A_2B_2'+X_3X_2A_1B_1'+X_3X_2X_1A_0B_0'$$

$$(A<B)=A_3'B_3+X_3A_2'B_2+X_3X_2A_1'B_1+X_3X_2X_1A_0'B_0$$

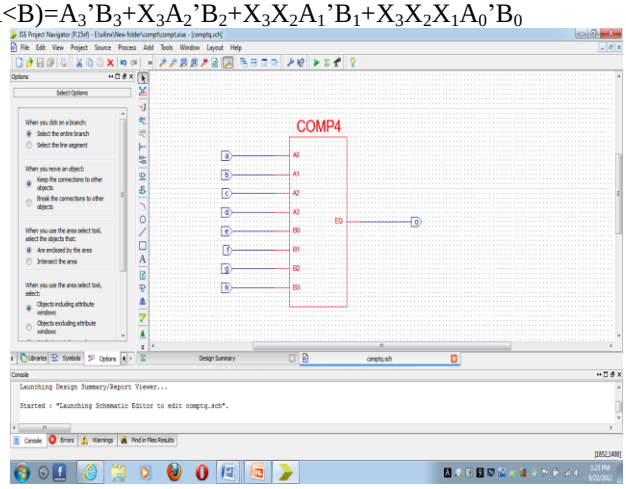

Figure 4. 4-bit comparator Circuit

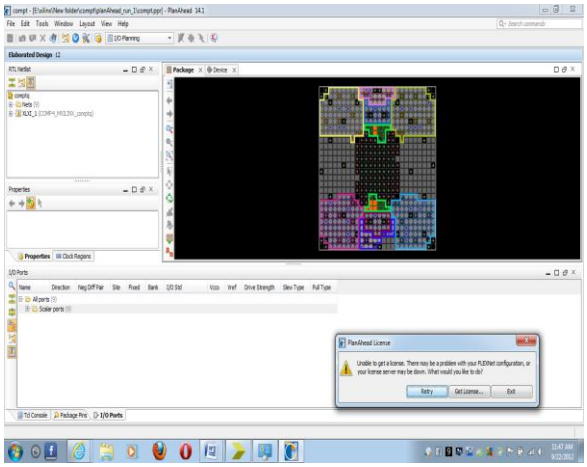

Figure 5. Synthesize design of comparator

Memory mapping is implemented by various comparators, Comparator tool is used to compare cache level to cache level mapping and mapped data from level 1 to level 2 cache and this process is continued for various cache levels.

With the help of Xilinx tool we have analyzed efficient mapping between them and 4-bit comparator design show in (fig 4 and5).

V. MEMORY OPERATION ANALYSIS

The write signal specifies a transfer in operation and read signal specifies a transfer out operation. The step must be taken for the purpose of transferring a new word to be stored into memory as follows:

1. Apply the binary address of the desired word to the address lines.
2. Apply the data bits that must be stored in memory to the data Input lines.
3. Activate the write input.

The memory unit will then take the bits from the input data lines and stores them in the word specified by the address lines. The steps that must be taken for the purpose of transferring a stored word out of memory are as follows.

1. Apply the binary address of the desired word to the address lines.
2. Activate the read input.

The memory unit will then take the bit from the word that has been selected by the address and apply them to the output data lines. The content of the selected word does not change after reading. Commercially memory components available in Integrated-Circuit chips sometimes provide the control input for reading and writing in a somewhat different configuration. Most integrated circuits provide two other controls inputs, they are input select and other determines the operations. The memory enable (sometimes called the chip select) is used to enable the particular memory chip in a multichip implementation of a large memory chip when the memory enable input is active , the read /write inputs determine the operation to be performed. When the memory enable is inactive, the memory chip is not selected and no operation is performed. Memory operations analyze with VHDL and perform waveform result in (fig. 6) with the help of micro wind simulator.

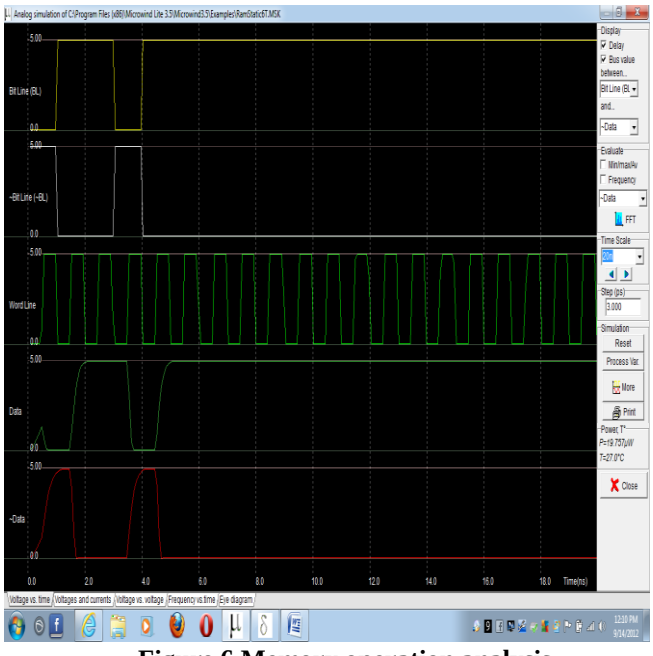

Figure 6.Memory operation analysis

VI. TEST RESULT ANALYSIS WITH VARIOUS SIMULATORS

Sim-cache: This simulator can emulate a system with multiple levels of instruction and data caches, each of which can be configured for different sizes and organizations. . Simple scalar simulator performs application specific result and show cache hierarchy structure in (table 1& figure 7).

Table 1. Cache simulation result

Benchmarks programs	Total no. Of instruction	Sim Memory Ref.	Sim elapsed time	Sim-inst-rate (inst/sec)
Calloc.c	5086757	1248274	3	1695585.6
Malloc.c	670697	162635	2	335348.5
Matrix.c	7035	3936	1	7035.00
Compress.c	8339	4292	1	8339.0
ll12.c	8076	4263	1	8076.0
ll14.c	14095	4995	1	14095.0
DIJKSTRA.c	24676	10135	18	1370

```
Cache levels can be unified by pointing a level of the instruction cache
hierarchy at the data cache hiearchy using the "dl1" and "dl2" cache
configuration arguments.  Most sensible combinations are supported, e.g.,

  A unified l2 cache (il2 is pointed at dl2):
    -cache:il1 il1:128:64:1:l -cache:il2 dl2
    -cache:dl1 dl1:256:32:1:l -cache:dl2 ul2:1024:64:2:l

  Or, a fully unified cache hierarchy (il1 pointed at dl1):
    -cache:il1 dl1
    -cache:dl1 ul1:256:32:1:l -cache:dl2 ul2:1024:64:2:l



sim: ** starting functional simulation w/ caches **
ravi
sim: ** simulation statistics **
sim_num_insn                7064 # total number of instructions executed
sim_num_refs                4008 # total number of loads and stores executed
sim_elapsed_time               1 # total simulation time in seconds
sim_inst_rate          7064.0000 # simulation speed (in insts/sec)
il1.accesses                7064 # total number of accesses
il1.hits                    6629 # total number of hits
il1.misses                   435 # total number of misses
il1.replacements             221 # total number of replacements
il1.writebacks                 0 # total number of writebacks
il1.invalidations              0 # total number of invalidations
il1.miss_rate             0.0616 # miss rate (i.e., misses/ref)
il1.repl_rate             0.0313 # replacement rate (i.e., repls/ref)
```

Figure 7. Cache simulation result

Micro wind simulator: -

The micro wind programs allow the design and simulate an integrated circuit at physical description level. The package contains a lib. of common logic and analog ICs to view and simulation. Micro wind includes all the commands for a mask editor as well as original tools never gathered before in a single module. The electric extraction of our circuit is automatically performed and the analog simulator produce voltage and current curve immediately.

With the help of micro wind simulator simulation we analyze CMOS 6-T SRAM simulation behavior in (fig 8&9).

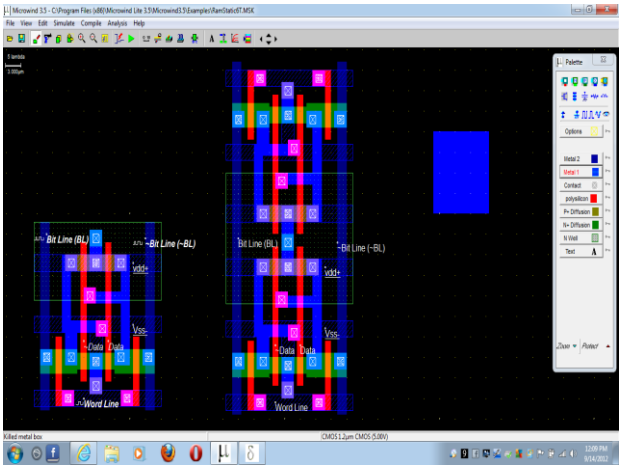

Figure 8. Circuit CMOS 6-T SRAM analysis.

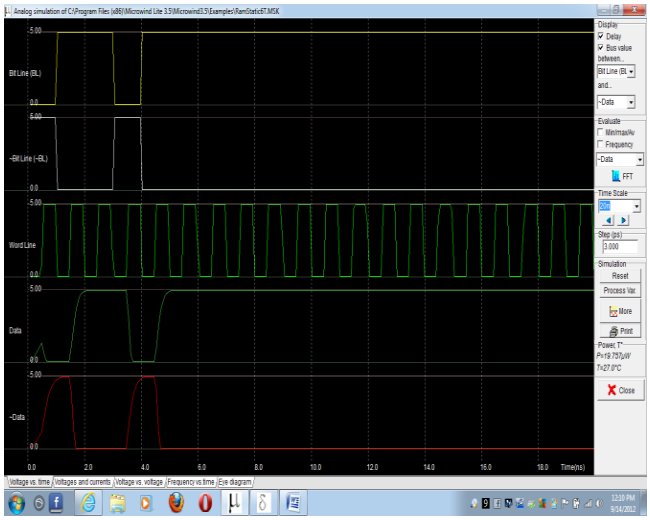

Figure 9. 6-T SRAM Schematic behavior SRAM analysis

The DSCH is used to validate the architecture of the logic circuit before the microelectronic design is started DSCH provide a user-friendly environment for hierarchical logic design , and fast simulation delay analysis, which allows the design and validate of complex logic structures. Design architecture of 6-T SRAM cell and show the schematic behavior with the help of DSCH micro wind design phase (fig 10 and 11).

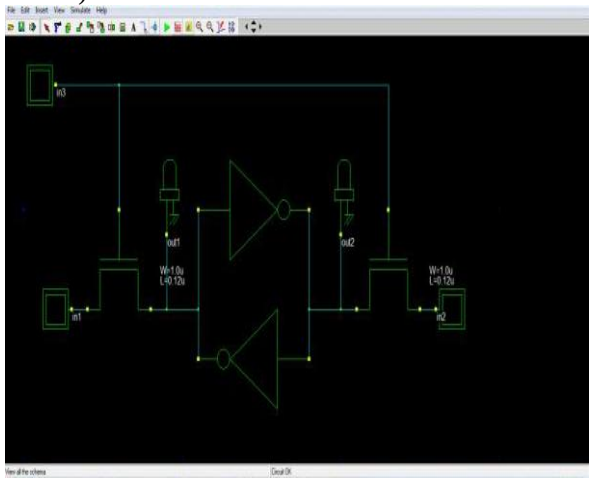

Figure 10. Design architecture of 6-T SRAM cell

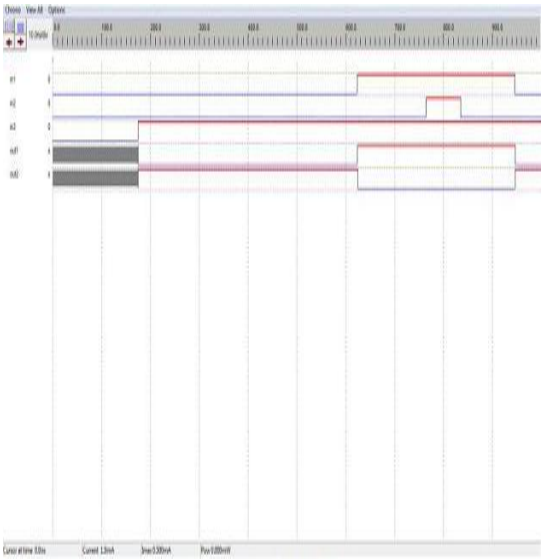

Figure 11. Schematic behavior 6-T SRAM analysis

Top spice 8 simulator:-

Top spice 8 is a native full-features mixed-mode, mixed-signal, and circuit, simulator capable of simulating circuits containing any arbitrary combination of analog device, digital function and high –level behavior blocks. With top spice we can verify and optimize our design from the system to the transistor level. Top spice offers a fully integrated environment to capture, simulate and analyze our circuit's design. Its flexible architecture allows the designer to integrate all design tools, including third party tools and model libraries, into complete CAD systems. With the help of this tool transistor level simulation analysis [fig 12 and fig13] and performed high level simulation.

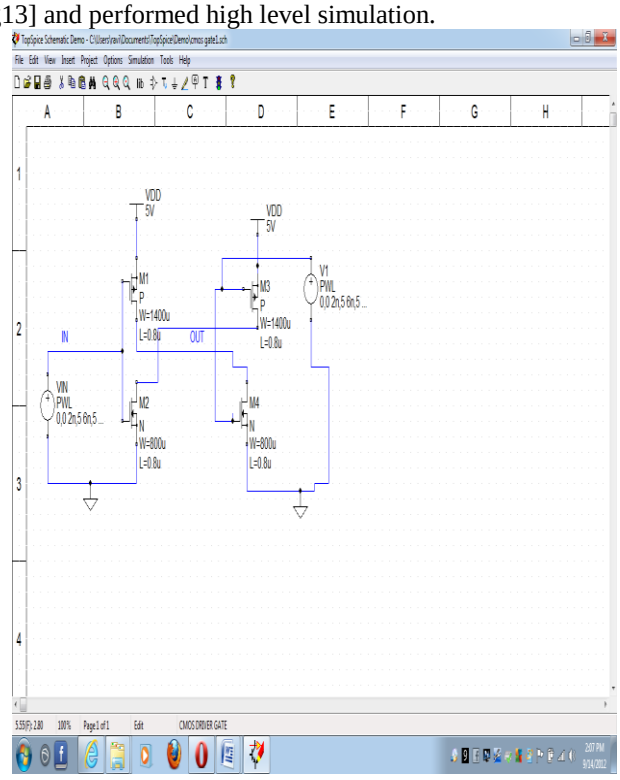

Figure 12. 4-t SRAM Circuit structure analysis

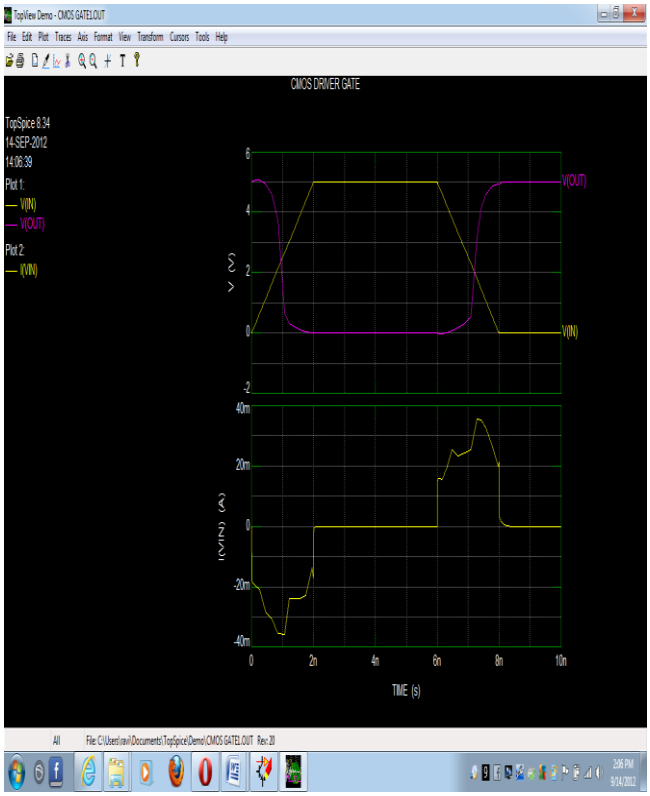

Figure 13. Schematic behavior SRAM analysis

XI. LINX TOOL

Timing waveform analysis:-

Xinix tool provide the access time of memory is the time required to select a word and read it. The cycle time of a memory is the time required to complete a write operation. The CPU must provide memory control signals in such a way so as to synchronize its internal clocked operations with the read and write operation of memory.

16-word by 8-bit static random access

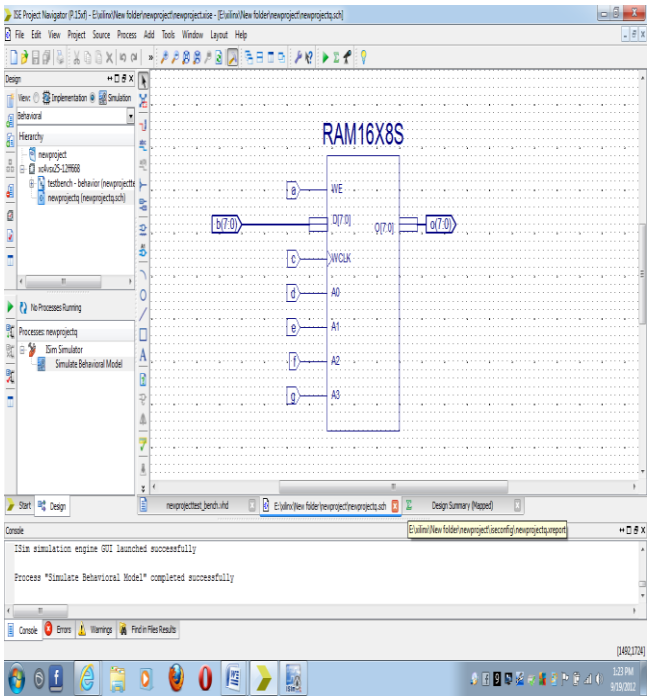

Figure 14. Design architecture of 16x8S SRAM cell

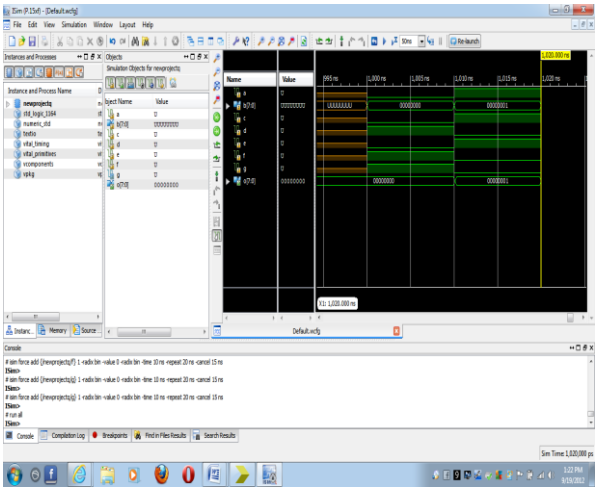

Fig 15. Schematic behavior 16x8S SRAM analysis

This element is a 16-word by 8-bit static random access memory with synchronous write capability(fig.14&15). When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on data inputs (D7:D0) into the word selected by the 4-bit address (A3:A0).

For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block. The signal output on the data output pins (O7:O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

Logic Table

Inputs			Outputs
WE (mode)	**WCLK**	**D7:D0**	**O7:O0**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	?	D7:D0	D7:D0
1 (read)	?	X	Data
Data = word addressed by bits A3A0			

64-word by 1-bit static random access memory:-

This design element is a 64-word by 1-bit static random access memory (RAM) with synchronous write capability(fig.16&17). When the write enable is set Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected.

When WE is set high, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 6-bit address (A5:A0). This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block. The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins. We can initialize this element during configuration using the INIT attribute.

Logic Table

Mode selection is shown in the following logic table

Inputs			Outputs
WE (mode)	**WCLK**	**D**	**O**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	?	D	D
1 (read)	?	X	Data
Data = word addressed by bits A5:A0			

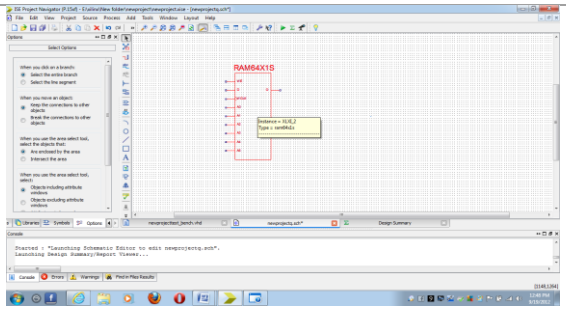

Figure 18. Design architecture of 64x1s SRAM cell

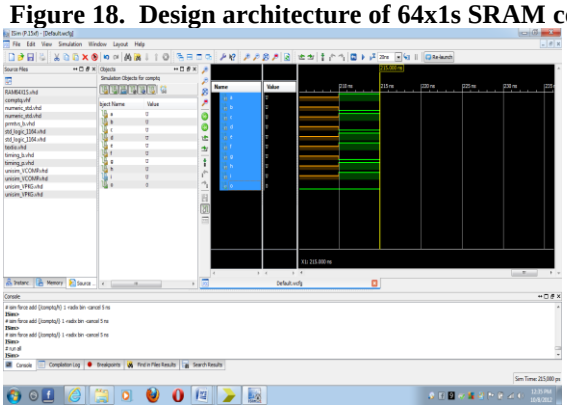

Figure 19. Schematic behavior 64x1s SRAM analysis

VII. CONCLUSION AND FUTURE WORK

In this paper presented the simulation behavior and design of cache memory. Various simulator like simple scalar, microwind, top spice 8, Xilinx toolset etc, are used for high performance and low power consumption. Simple scalar simulator simulates application specific result and show cache hierarchy structure. Micro wind simulator simulates cache RAM structure and produce efficient schematic behavior of cache RAM. High performance simulator analyzing their efficient cache memory simulation performance. Xilinx tool provide efficient timing waveform analysis and efficient schematic behavior of cache RAM. Xilinx tool used for better mapping and analysis of various cache memories. After simulation behavior analysis we have working on bypass caching mechanism for embedded system.

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