Transient Thermal Analysis of Pulsed Silicon SDR IMPATT at 35 GHz

L. P. Mishra, A. Acharyya and M. Mitra

Abstract: In this paper the transient thermal analysis of 35 GHz pulsed silicon Single-Drift Region (SDR) Impact Avalanche Transit Time (IMPATT) device is presented. A double-iterative field maximum computer method based on drift-diffusion model is used to obtain the DC and high frequency properties of the device. A transient thermal model has been developed by the authors' to study the temperature transients in pulsed Si SDR IMPATT at 35 GHz. Results show that the device is capable of delivering a peak pulsed power output of 7.40 W with 8.46% DC to RF conversion efficiency. The maximum junction temperature rise is 352.5 K for peak pulsed bias current of 1.08 Ampere with 200 ns pulsewidth and 1.0% duty cycle.

Keywords: Millimeter-wave, pulsed Si SDR IMPATTs, temperature transients, thermal analysis.

I. INTRODUCTION

Impact Avalanche Transit Time (IMPATT) devices are the most efficient solid-state source to deliver significantly high power at millimeter-wave frequencies [1-3]. Most of the current research activities for mm-wave systems are concentrated on window frequencies, i.e. 35, 94, 140, 220 GHz where atmospheric attenuation is relatively low. The performance and reliability of IMPATT devices is strongly dependent on the junction temperature of the device, since some form of material transport ultimately causes the performance of the device to degrade beyond the limits of usability and since the rate of material transport rises rapidly with temperature [4]. Acharyya et al. investigated the dependence of millimeter-wave performance of Continuous Wave (CW) DDR Si IMPATT device operating at 94 GHz [5] following a small-signal simulation approach based on Gummel-Blue approach [6-8]. In the present paper a rigorous transient thermal analysis of the pulsed Si SDR IMPATT has been carried out by using type-IIA diamond heat sink to find out the peak junction temperature by varying the pulsewidth (0 ns - 250 ns) for a fixed repetition rate (50 KHz) of the bias current pulse. The DC and high frequency properties and performance of the device are very much sensitive to the variation of junction temperature under pulsed operation.

Manuscript received on March, 2013.

Sri L.P. Mishra is an assistant professor at the Dept. of ECE, ITER, SOA University, Bhubaneswar, Orissa and currently doing his research at BESU, Shibpur.

Sri A. Acharyya did his M. Tech at Institute of Radio Physics & Electronics, Kolkata University and currently doing his Ph.D. work at Kolkata University, India.

Dr. M. Mitra is an Associate Professor at the Department of Electronics & Telecommunication engineering, BESU, Shibpur, Howrah, India.

After evaluating the junction temperature from the thermal analysis [9], the material parameters of Si corresponding to that temperature have been incorporated into the DC and high frequency simulation program developed by the authors to find out the pulsed power output and DC to RF conversion efficiency.

II. DC AND HIGH FREQUENCY SIMULATION TECHNIQUE

One-dimensional model of reverse biased p+nn+ structure as shown in Fig. 1 is taken for DC and high frequency simulation of pulsed SDR IMPATT device. The DC electric field and current density profiles in the depletion layer of the device are obtained from simultaneous numerical solution of fundamental device equations i.e., Poisson's equation, combined carrier continuity equation in the steady state, current density equations and mobile space charge equation subject to appropriate boundary conditions. A double-iterative, field maximum simulation method based on Gummel-Blue approach [8] described elsewhere [6] is used to solve these equations and obtain the electric field and current density profiles. In the above mentioned simulation method, the computation starts from the field maximum near the metallurgical junction. The boundary conditions for the electric field at the depletion layer edges are given by:

$$\xi(0) = 0 \qquad \text{and} \qquad \xi(W_n) = 0$$

(1)

Similarly the boundary conditions for normalized current density P(x) = (Jp(x) - Jn(x)) / J0 (where, J0 = Jp + Jn) at the depletion layer edges i.e., at x = 0 and x = Wn are given by:

$$P(0) = [(2/M_p) - 1]$$
 and $P(W_n) = [1 - (2/M_n)]$

here Mn and Mp are the electron and hole multiplication factors whose values are of the order of 106 under dark or un-illuminated condition of the device. Electric field profiles and current profiles are obtained from the DC simulation. The breakdown voltage (VB) is calculated by integrating the spatial field profile over the total depletion layer width (Wn), i.e.:

$$V_B = \int_{0}^{w_n} \xi(x) dx$$
(3)

And the avalanche zone voltage drop (V_A) is calculated by integrating the spatial field profile over the total avalanche layer width (x_A) , i.e.:

$$V_A = \int_{0}^{x_A} \xi(x) dx \tag{4}$$



Published By: Blue Eyes Intelligence Engineering & Sciences Publication Again the DC to RF conversion efficiency is calculated from the semi quantitative formula [10]:

 $\eta(\%) = \left(2m_p / \pi\right) \times \left(V_D / V_B\right)$

(5) where $V_D = (V_B - V_A) =$ voltage drop across the drift region and $m_p = 1/2$.



Fig.1. One dimensional model of SDR IMPATT device

The magnitude of peak field at the junction (ξ_p) , breakdown voltage (V_B) , the widths of avalanche and drift zones (x_A and x_D ; where $x_D = W_n - x_A$) and the voltage drops across these zones (V_A, V_D) are obtained from doubleiterative simulation program. These values are fed back as input parameters in the high frequency simulation from which the admittance properties of the device is obtained. The depletion layer edges of the device obtained from the output of DC simulation program are taken as the starting and end points of numerical computation in the high frequency program. Two second order differential equations are framed by resolving the device impedance $Z(x, \omega)$ into its real part $R(x,\omega)$ and imaginary part $X(x,\omega)$; where, $Z(x,\omega) =$ $R(x,\omega) + i X(x,\omega)$. A double-iterative simulation over the initial choice of the values of R and X described in details in [7] is used to solve simultaneously the two second order differential equations in R and X subject to appropriate boundary conditions. The negative specific resistance (R(x))and specific reactance (X(x)) profiles are obtained from the above solution. The device negative resistance (Z_R) and reactance (Z_X) are obtained from the numerical integration of the R(x)- and X(x) profiles respectively over the spacecharge layer width, W_n . Thus:

$$Z_R = \int_{0}^{W_n} R(x) dx \quad \text{and} \quad Z_X = \int_{0}^{W_n} X(x) dx$$
(6)

The impedance of the device is given by, $Z_D = Z_R + j Z_X$ and the device admittance is, $Y_D = 1/Z_D = G + j B$. The negative conductance (*G*) and positive susceptance (*B*) are computed from the following expressions,

$$|G(\omega)| = Z_R / \left(Z_R^2 + Z_X^2 \right) \text{ and } |B(\omega)| = -Z_X / \left(Z_R^2 + Z_X^2 \right)$$
(7)

It may be noted that both G and B are normalized to the area of the device. The admittance $(G(\omega) \text{ versus } B(\omega))$ plots of the device can be obtained for different bias current densities from the above analysis. The maximum power output P_{RF} from the device can be obtained from the following expression,

$$P_{RF} = (1/2)(V_{RF})^2 |G_p| A_j$$
(8)

where V_{RF} is the RF voltage ($V_{RF} = m_x \times V_B$; $m_x = 1/2$ for 50% modulation), $|G_p|$ is the magnitude of peak of the negative conductance at optimum frequency (f_p) and A_j is the device junction area.

III. RESULTS AND DISCUSSION

The active layer width (n-layer width (W_n) and background doping concentrations (n-layer doping

concentration (N_D) and n^+ -layer doping concentrations (N_{n+})) of Si SDR IMPATT device have been designed to operate at 35 GHz window frequency by using simple transit time formula by Sze and Ryder [11] and simulated using DC [6] and high frequency [7] simulation techniques as described in the previous section. The corresponding optimized design parameters are given in Table 1. The temperature and realistic field dependence of ionization rates (α_n, α_p) and drift velocities (v_n, v_p) and other material parameters of Si such as bandgap (E_g) , intrinsic carrier concentration (n_i) , effective density of states of conduction and valance bands (N_c, N_v) , diffusion coefficients (D_n, D_p) , mobilities (μ_n, μ_p) & diffusion lengths (L_n, L_p) of charge carriers and permittivity (ε_s) are taken from the recently published experimental reports [12-15].

Table 1: Design Parameters.

Design Frequency	Structure	<i>W_n</i> (μm)	$(\times 10^{22} \text{ m}^{-3})$	$(\times 10^{26} \text{ m}^{-3})$
35 GHz	p^+nn^+	1.43	2.70	1.0

Important DC parameters such as peak electric field (ξ_p) , breakdown voltage (V_B) , avalanche zone voltage drop (V_A) , DC to RF conversion efficiency (η) , avalanche region width (x_A) and ratio of avalanche zone width to total depletion layer width (x_A/W) for different peak pulsed bias current densities (J_0) are obtained from double-iterative fieldmaximum DC simulation [6] and given in Table 2. It can be observed from Table 2 that the peak electric field (ξ_p) decreases from 5.1543×10^7 V m⁻¹ to 5.1432×10^7 V m⁻¹ and the breakdown voltage (V_B) increases from 34.66 V to 37.08 V as the peak pulse bias current density changes from 5.0×10^7 A m⁻² to 9.0×10^7 A m⁻². The avalanche zone voltage drop (V_A) also increases from 26.23 V to 28.38 V due to same change in the peak pulse bias current density. The peak pulsed bias current densities (J_0) is varied from 5.0×10^7 A m⁻² to 9.0×10^7 A m⁻² to obtain it's optimum value for which the DC to RF conversion efficiency (η) of the device is maximum. The optimum peak pulsed bias current density is obtained as 7.0×10^7 A m⁻² for which DC to RF conversion efficiency (η) is maximum (8.46%). It can be noted from Table 2 that the sharp increase in the avalanche region width (x_A) is occurred as the bias current density is increased.

Table 2: DC and High Frequency Properties.

Parameters	Set I	Set II	Set III	Set IV	Set V
J_0	5.0	6.0	7.0	8.0	9.0
$(\times 10^7 \text{ A m}^{-2})$					
ξ_p	5.1543	5.1524	5.1505	5.1487	5.1432
$(\times 10^7 \text{ V m}^{-1})$					
$V_B(\mathbf{V})$	34.66	35.17	35.88	36.32	37.03
$V_A(\mathbf{V})$	26.23	26.44	26.34	27.31	28.38
$x_A (\mu m)$	0.6870	0.7168	0.7105	0.7523	0.7440
$x_A/W(\%)$	48.04	50.12	49.69	52.60	52.03
η (%)	7.74	7.90	8.46	7.89	7.44
f_p (GHz)	32.5	33.8	35.0	36.1	37.2
$G_p (\times 10^7 \mathrm{S m^{-2}})$	-2.1753	-2.6564	-2.9892	-3.3671	-3.5762
$B_p (\times 10^7 \text{ S m}^{-2})$	9.6712	9.8131	10.0162	10.2181	10.3167
$Q_p (= -B_p/G_p)$	4.45	3.69	3.35	3.03	2.88
$Z_R (\times 10^{-8} \Omega m^2)$	2.2137	2.5702	2.7359	2.9090	2.9996
$P_{RF}/A_j (\times 10^8 \text{ W m}^{-2})$	3.2665	4.1072	4.8103	5.5521	6.1297

Published By: Blue Eyes Intelligence Engineering & Sciences Publication



The electric field profiles of the device for different peak pulsed bias current densities are shown in Fig. 2. It can be observed from Fig. 2 that the electric field profiles are get distorted at higher peak pulsed bias current densities due to higher space charge effect [16-17]. The normalized current density profiles i.e. P(x)-profiles of the device for different peak pulsed bias current densities are shown in Fig. 3. Sharp increase of P(x)-profile indicates the narrower avalanche region width (x_A) and thus the higher DC to RF conversion efficiency (η) . It can be noted from Fig. 3 that the P(x)profiles for higher peak pulsed bias current densities smear out causing the widening of the avalanche region; thus results fall in DC to RF conversion efficiency (η) .



Fig. 2: Electric field profiles of pulsed Si SDR IMPATT device at 35 GHz.



Fig. 3: P(x)-profiles of pulsed Si SDR IMPATT device at 35 GHz.

Important high frequency properties such as optimum frequency (f_p) , peak negative conductance (G_p) , corresponding susceptance (B_p) , *Q*-factor $(Q_p = -B_p/G_p)$,

negative resistance and output RF power density (P_{RF} / A_j) for different peak pulsed bias current densities (J_0) are obtained from high frequency simulation [7] and given in Table 2. Admittance characteristics of the device for different peak pulsed bias current densities are shown in Fig. 4. It can be observed from Fig. 4 and Table 2 that the magnitude of negative conductance $(|G_p|)$ and corresponding susceptance $(|B_p|)$ increase as the peak pulsed bias current density increases. But the Q-factor (Q_p) which indicates the oscillation growth rate and stability of oscillation decreases from 4.45 to 2.88 as the peak pulsed bias current density increases from 5.0×10^7 A m⁻² to 9.0×10^7 A m⁻². At the optimum peak pulsed bias current density $(7.0 \times 10^7 \text{ A m}^{-2})$ the Q-factor is obtained as 3.35 which is not too much far away from the desired level (i.e. $Q_p \approx 1.0$) for stable oscillation.



IMPATT device at 35 GHz.

Negative resistivity profiles or R(x)-profiles of the device for different peak pulsed bias current densities are shown in Fig. 5. Negative resistivity profiles show a peak at the middle of the *n*-drift region and a minimum near the p^+ -*n* metallurgical junction. It can be noted from Fig. 5 that the negative resistivity peak associated with R(x)-profile is decreased as the peak pulsed bias current density is increased. Negative resistance (Z_R) of the device for different peak pulsed bias current densities are calculated for numerical integration of the R(x)-profiles throughout the total depletion region (W_n) . It can be observed from Table 2 that the negative resistance (Z_R) of the device increases as the peak pulsed bias current density is increases. Output RF power densities (P_{RF} / A_i) for different peak pulsed bias current densities are also calculated from the knowledge of $|G_p|$, J_0 and V_B for 50% voltage modulation. Peak pulsed power output can be obtained by multiplying the Output RF power density by device effective junction area $(A_i =$ $\pi(D_i/2)^2$; where circular cross-section of diameter, $D_i = 140$ µm is assumed for 35 GHz pulsed Si SDR IMPATT). Peak pulsed power output increases from 5.03 W to 9.44 W as the peak pulsed bias current density increases from 5.0×10^7 A m^{-2} to 9.0×10⁷ A m^{-2} .



Published By: Blue Eyes Intelligence Engineering & Sciences Publication

104



Fig. 5: Negative resistivity profiles of pulsed Si SDR IMPATT device at 35 GHz.

Type-IIA diamond heat sink having diameter (D_H) of 5.0 mm and thickness (L_H) of 2.0 mm is considered for the transient thermal analysis of 35 GHz pulsed DDR Si IMPATT device. Step function is used to represent the input bias current pulse. The program for transient thermal model developed by the authors is used to compute the junction temperature transients for different bias current pulsewidths with a fixed repetition rate ($f_c = 50$ KHz). Fig. 6 shows the junction temperature transients of the device having different junction diameters ($D_i = 110, 120, 130, 140 \mu m$) mounted on type-IIA diamond heat sink. It is observed from Fig. 6 that, the junction temperature of the device gradually increases from the ambient temperature ($T_a = 300$ K) during the on-time of the applied current pulse and reaches the maximum temperature at the end of the on time. It can be noted from Fig. 6 that larger the device junction diameter, greater the rate of rise of junction temperature with respect to time. This is because, as the junction diameter of the device increases, the device junction cross-sectional area increases, which intern allows greater current to pass through the device and thus causes greater rate of increase in junction temperature with time; since greater current increases the power dissipation in the device for fixed DC to RF conversion efficiency $(P_{diss} = (1-\eta) \times V_B \times I_0;$ where $I_0 =$ $J_0 \times A_i$). Usually the Ka-band pulsed Si DDR IMPATTs are operated with bias current pulse of 200 ns pulsewidth and 1.0% duty cycle. The thermal analysis presented in this paper shows that the maximum junction temperature rise $((T_{max})$ is 352.5 K for a peak pulsed bias current of 1.08 Ampere with 200 ns pulsewidth and 1.0% duty cycle. After repetitive run of the program for transient thermal model along with the DC and high frequency program, the maximum junction temperature ($T_{max} = 352.5$ K) at the end of the on time of the applied bias current pulse is obtained. Thus the DC and high frequency results presented in this paper are obtained by incorporating the material parameters of Si at that temperature.



Fig. 6: Variations of junction temperature with pulsewidth for different device junction diameters.

IV. CONCLUSION

In this paper the transient thermal analysis of 35 GHz pulsed Si SDR IMPATT device is presented. A doubleiterative field maximum computer method based on driftdiffusion model is used to obtain the DC and high frequency properties of the device. A transient thermal model has been developed by the authors' to study the temperature transients in pulsed Si SDR IMPATT at 35 GHz. Results show that the device is capable of delivering a peak pulsed power output of 7.40 W with 8.46% DC to RF conversion efficiency. The maximum junction temperature rise is 352.5 K for peak pulsed bias current of 1.08 Ampere with 200 ns pulsewidth and 1.0% duty cycle.

ACKNOWLEDGMENT

The authors would like to thank Professor (Dr.) J. P. Banerjee for many helpful discussions concerning the model of transient thermal analysis and DC and high frequency simulation of pulsed IMPATT source.

REFERENCES

- T. A. Midford and R. L. Bernick, "Millimeter Wave CW IMPATT diodes and Oscillators", IEEE Trans. Microwave Theory Tech., vol. 27, pp. 483-492, 1979.
- Y. Chang, J. M. Hellum, J. A. Paul and K. P. Weller, "Millimeter-Wave IMPATT Sources for Communication Applications", IEEE MTT-S International Microwave Symposium Digest, 1977, pp. 216-219.
- W. W. Gray, L. Kikushima, N. P. Morentc and R. J. Wagner, "Applying IMPATT Power Sources to Modern Microwave Systems", IEEE Journal of Solid-State Circuits, vol. 4, pp. 409-413, 1969.
- H. M. Olson, "A Mechanism for Catastropic failure of Avalanche Diodes", IEEE Trans. on Electron Devices, vol. ED-22, pp. 842-849, 1975.
- A. Acharyya, S. Banerjee and J. P. Banerjee, "Dependence of DC and Small-signal Properties of Double Drift Region Silicon IMPATT Device on Junction Temperature", Journal of Electron Devices, vol. 12, pp. 725-729, 2012.



Published By: Blue Eyes Intelligence Engineering & Sciences Publication

- S. K. Roy, M. Sridharan, R. Ghosh, and B. B. Pal, "Computer method for the dc field and carrier current profiles in the IMPATT device starting from the field extremum in the depletion layer", Proceedings of the 1st Conference on Numerical Analysis of Semiconductor Devices (NASECODE I), J. H. Miller, Ed., Dublin, Ireland, pp. 266-274, 1979.
- S. K. Roy, J.P. Banerjee and S. P. Pati, "A Computer analysis of the distribution of high frequency negative resistance in the depletion layer of IMPATT Diodes", Proc. 4th Conf. on Num. Anal. of Semiconductor Devices (NASECODE IV) (Dublin) (Dublin: Boole), pp. 494-500, 1985.
- H. K. Gummel and J. L. Blue, "A small-signal theory of avalanche noise in IMPATT diodes", IEEE Trans. on Electron Devices, vol. ED-14, no. 9, pp. 569-580, 1967.
- H. M. Olson, "Temperature Transients in IMPATT Diodes', IEEE Trans. on Electron Devices, vol. ED-23, no. 5, pp. 494-503, 1976.
- D. L. Scharfetter and H. K. Gummel, "Large-Signal Analysis of a Silicon Read Diode Oscillator", IEEE Trans. on Electron Devices, vol. ED-16, no. 1, pp. 64-77, January 1969.
- S. M. Sze, and R. M. Ryder, "Microwave Avalanche Diodes", Proc. of IEEE, Special Issue on Microwave Semiconductor Devices, vol. 59, issue 8, pp. 1140-1154, 1971.
- W. N. Grant, "Electron and hole ionization rates in epitaxial Silicon", Solid State Electron, vol. 16, no. 10, pp. 1189-1203, 1973.
- C. Canali, G. Ottaviani and A. A. Quaranta, "Drift velocity of electrons and holes and associated anisotropic effects in silicon", J. Phys. Chem. Solids, vol. 32, issue 8, pp. 1707, 1971.
- 14. Zeghbroeck, B.V.: Principles of Semiconductor Devices, Colorado Press, 2011.
- "Electronic Archive: New Semiconductor Materials, Characteristics and Properties," http://www.ioffe.ru/SVA/NSM/Semicond/Si/index.html.
- M. Sridharan, S. K. Roy, "Computer studies on the widening of the avalanche zone and decrease on efficiency in silicon X-band symmetrical DDR" Electron Lett., vol. 14, pp. 635-637, 1978.
- M. Sridharan, S. K. Roy, "Effect of mobile space charge on the small signal admittance of silicon DDR", Solid State Electron, vol. 23, pp. 1001-1003, 1980.



Published By:

& Sciences Publication

Blue Eyes Intelligence Engineering