# Design of High Speed Ladner-Fischer Based Carry Select Adder

**Pakkiraiah Chakali, Madhu Kumar Patnala**

***Abstract- In this paper, we propose a high speed Carry Select Adder by replacing Ripple Carry Adders with parallel prefix adders. Adders are the basic building blocks in digital integrated circuit based designs. Ripple Carry Adders (RCA) are usually preferred for addition of two multi-bit numbers as these RCAs offer fast design time among all types of adders. However RCAs are slowest adders as every full adder must wait till the carry is generated from previous full adder. On the other hand, Carry Look Ahead (CLA) adders are faster adders, but they required more area. The Carry Select Adder is a compromise on between the RCA and CLA in term of area and delay. CSLA is designed by using dual RCA: due to this arrangement the area and delay are still concerned factors. It is clear that there is a scope for reducing delay in such an arrangement. In this research, we have implemented CSLA with prefix adders. Prefix adders are tree structure based and are preferred to speed up the binary additions. This work estimates the performance of proposed design in terms of Logic and route delay. The experimental results show that the performance of CSLA with parallel prefix adder is faster and area efficient compared to conventional modified CSLA.***

***Index Terms- prefix adder, CSLA, delay, Carry Operator, area-efficient.***

## I. INTRODUCTION

In Digital Computer Design adder is an important component and it is used in multiple blocks of its architecture. In many Computers and in various classes of processor specialization, adders are not only used in Arithmetic Logic Units [6], but also used to calculate addresses and table indices. There exist multiple algorithms to carry on addition operation ranging from simple Ripple Carry Adders to complex CLA.

The basic operations involved in any Digital Signal Processing systems are Multiplication, Addition and Accumulation. Addition is an indispensible operation in any Digital, DSP or control system. Therefore fast and accurate operation of digital system depends on the performance of adders [6]. Hence improving the performance of adder is the main area of research in VLSI system design. Over the last decade many different adder architectures were studied and proposed to speed up the binary additions. The details of Ripple Carry Adder and Carry Select Adder are discussed in section II, and the implementation of proposed system is described in section III. The performance and simulation results were presented and discussed in section IV.

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## II. CARRY SELECT ADDER (CSLA)

In Electronics, carry-select adder is a particular way to implement an adder. It is a logic element that computes the sum of two n-bit numbers. The carry-select adder generally composes of two ripple carry adders [10] and a multiplexer.

### Ripple Carry Adder

The Ripple Carry Adder is used to compute addition of two N-bit numbers. It consists of N full adders to add N-bit numbers. From the second full adder, carry input of every full adder is the carry output of its previous full adder. This kind of adder is typically known as Ripple Carry Adder because carry ripples to next full adder. The layout [12] of Ripple Carry Adder is simple, which allows fast design time. The Ripple Carry Adder [9] is slowest among all the adders because every full adder must wait till the previous full adder generates the carry bit for its input. The 3-bit RCA is shown in Figure 1. Theoretically the Ripple Carry Adder has delay of $o(n)$ and area of $o(n)$.

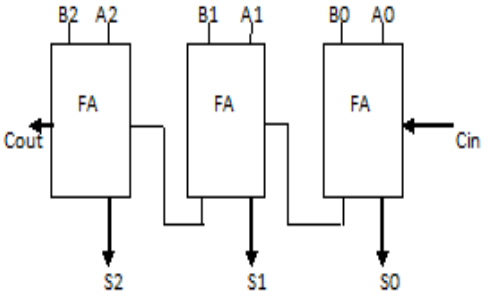


**Figure 1. 3-bit Ripple Carry Adder**

### Multiplexer

Multiplexer is a combinational circuit which has many inputs and single output. Depending on the select input combination the content on one of the selected input line is transferred on to the output line. It is also widely known as many to one circuit, data selector and universal parallel to serial converter. The 6:3 Multiplexer is shown in Figure 2.

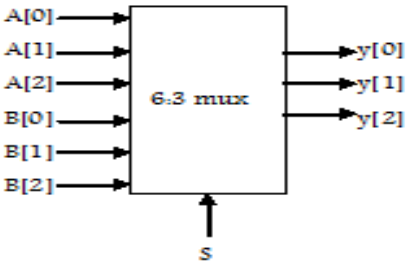


**Figure 2. 6:3 multiplexer**

**Carry Select Adder**

The Carry Select Adder [3] consists of dual Ripple Carry Adders and a multiplexer. The modified CSLA [1] is shown in Figure 3.In this diagram the addition of two 16-bit numbers is done with two RCAs [7] of $c_{in}$=0 and $c_{in}$=1. After the calculation for two cases of carry, the correct sum as well as correct carry is selected by using multiplexer once the correct carry is known.

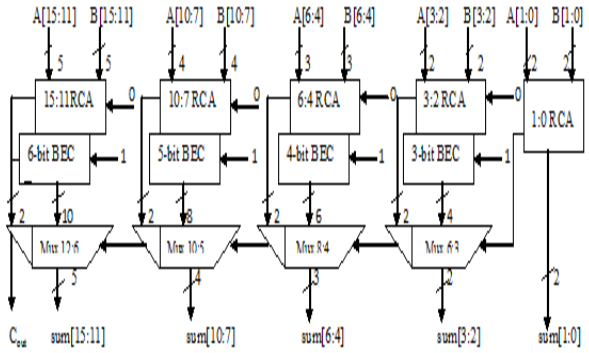


**Figure 3. Modified CSLA.**

There are two types of Carry Select Adders one is uniform and another one is variable carry select adder [4]. In uniform Carry Select Adder each block size is fixed in all stages, but in variable Carry Select Adder block size is variable. The delay at $c_{in}$ input stage can be reduced using variable type of CSLA [2]. Theoretically delay and area of Carry Select Adder are $o(\sqrt{n})$ and $o(2n)$ respectively.

## III. PROPOSED CSLA

**Parallel prefix adders**

The parallel prefix adders [11] are more flexible and are used to speed up the binary additions. Parallel prefix adders [14] are obtained from Carry Look Ahead (CLA) structure. We use tree structure form to increase the speed [13] of arithmetic operation. Parallel prefix adders are fastest adders and these are used for high performance arithmetic circuits in industries. The construction of parallel prefix adder [5] involves three stages

1. Pre- processing stage
2. Carry generation network
3. Post processing

**Pre-possessing stage**

In this stage we compute, generate and propagate signals to each pair of inputs A and B. These signals are given by the logic equations 1&2:

$$P_i=A_i \text{ xor } B_i \quad \text{..... (1)}$$
$$G_i=A_i \text{ and } B_i \quad \text{..... (2)}$$

**Carry generation network**

In this stage we compute carries corresponding to each bit. Execution of these operations is carried out in parallel [5]. After the computation of carries in parallel they are segmented into smaller pieces. It uses carry propagate and generate as intermediate signals which are given by the logic equations 3&4:

$$CP_{i:j}=P_{i:k+1} \text{ and } P_{k:j} \quad \text{.....(3)}$$
$$CG_{i:j}=G_{i:k+1} \text{ or } (P_{i:k+1} \text{ and } G_{k:j}) \quad \text{.....(4)}$$

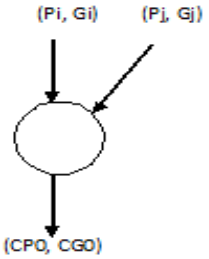


**Figure 4. Carry operator**

The operations involved in this figure are given as:

$$CP_0=P_i \text{ and } P_j \quad \text{..... (3(i))}$$
$$CG_0=(P_i \text{ and } G_j) \text{ or } G_i \quad \text{..... (3(ii))}$$

**Post processing**

This is the final step to compute the summation of input bits. It is common for all adders and the sum bits are computed by logic equation 5&6:

$$C_{i-1}=(P_i \text{ and } C_{in}) \text{ or } G_i \quad \text{..... (4)}$$
$$S_i=P_i \text{ xor } C_{i-1} \quad \text{..... (5)}$$

**Ladner-Fischer (LF) adder**

Ladner-Fischer adder is a parallel prefix form of Carry Look-ahead Adder. Ladner-Fischer adder [14] can be represented as a parallel prefix graph consisting of carry operator nodes. The time required to generate carry signals in this prefix adder is $o(\log n)$. It is the fastest adder with focus on design time and is the common choice for high performance adders in industry. The Ladner-Fischer adder concept was developed by R.Ladner and M. Fischer [14], which was published in 1980. The better performance of Ladner-Fischer adder is because of its minimum logic depth and bounded fan-out. On the other side it occupies large silicon area. The construction of 2, 3, 4, 5-bit Ladner-Fischer adder are shown below.

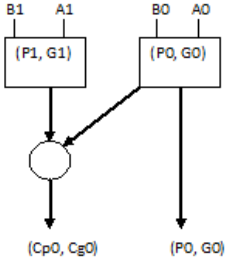


**Figure 5. 2-bit LF Adder**

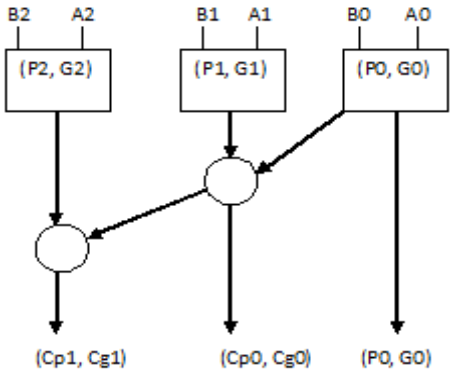


**Figure 6. 3-bit LF Adder**

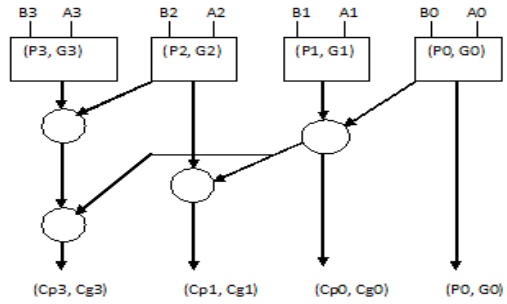


**Figure 7. 4-bit LF Adder**

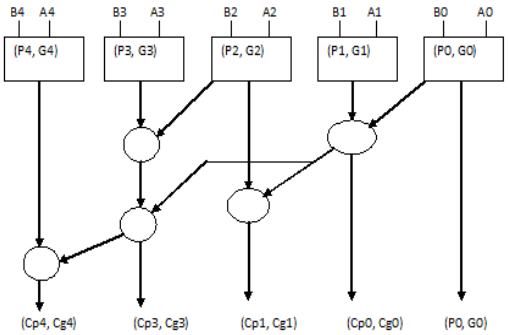


**Figure 8. 5-bit LF Adder**

Figure 9 shows the structure of modified CSLA. The modification is done by replacing 2, 3, 4, 5-bit RCAs with 2, 3, 4, 5-bit Ladner-Fischer adders.

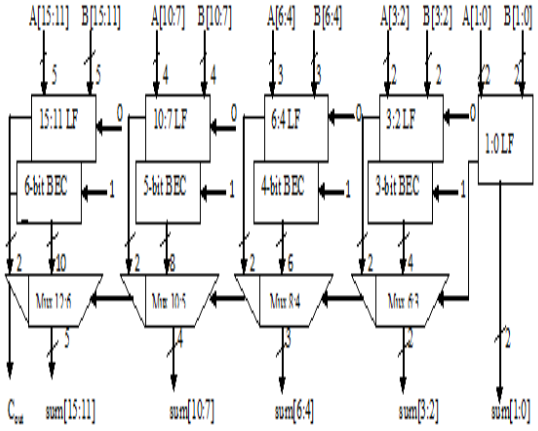


**Figure 9. Modified 16-b LF CSLA.**

## IV. SIMULATION RESULTS AND COMPARISONS

Various adders were designed using Verilog language in Xilinx ISE Navigator 10.1 and all the simulations are performed using Xilinx ISE simulator. The performance of proposed CSLA is analyzed and compared against the conventional CSLA designs. In this proposed CSLA architecture, the implementation code for 2, 3, 4, 5-bit Ladner-Fischer adders were developed and corresponding values of logic and route delay were tracked. These values are compared to 2, 3, 4, 5-bit Ripple Carry Adders logic and route delay. Table 1 shows the comparison of CSLA with Ripple Carry Adders and CSLA with Ladner-Fischer adders in terms of logic and route delay. The simulated output of 16-bit proposed CSLA is shown in Figure 10.

**Table 1. Logic and Route delay values of proposed CSLA and conventional CSLA.**

| Adder type | | Logic Delay (ns) | Route delay | Total delay |
|---|---|---|---|---|
| Ripple carry adder | 2-bit | 5.499 | 1.338 | 6.837 |
| | 3-bit | 6.111 | 1.787 | 7.898 |
| | 4-bit | 6.723 | 2.236 | 8.959 |
| | 5-bit | 7.335 | 2.685 | 10.020 |
| | Modified CSLA | 11.619 | 5.862 | 17.481 |
| Ladner-Fischer adder | 2-bit | 5.165 | 0.96 | 6.125 |
| | 3-bit | 5.499 | 1.434 | 6.933 |
| | 4-bit | 6.111 | 1.902 | 8.013 |
| | 5-bit | 7.335 | 2.477 | 9.812 |
| | Modified CSLA | 9.449 | 4.541 | 13.99 |

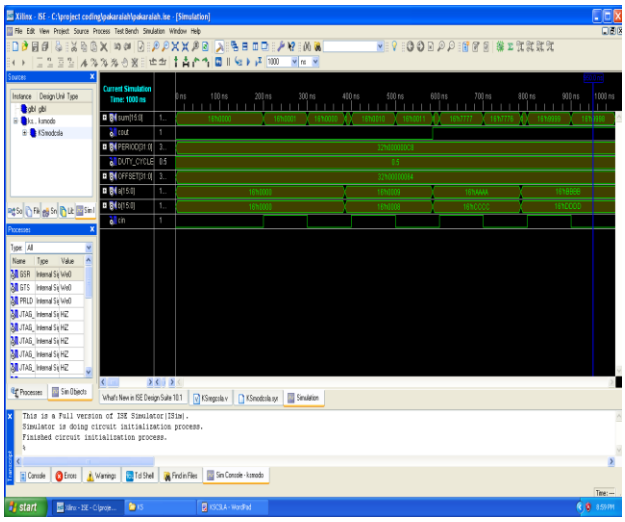

**Figure 10. Simulated Output of 16-b LF CSLA.**

The comparison between 2, 3, 4, 5-bit, proposed and conventional CSLA are shown in Figure 11 in terms of logic and route delay values.

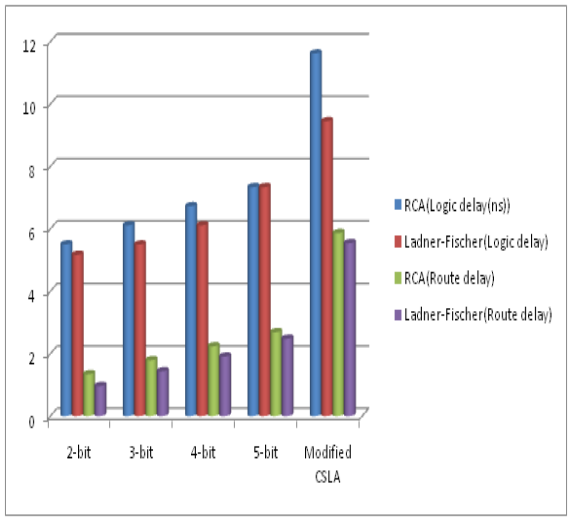


**Figure 11. Delay (logic and route) comparison between different adders.**

The comparison between proposed and conventional CSLA in terms of total delay is shown in Figure 12.

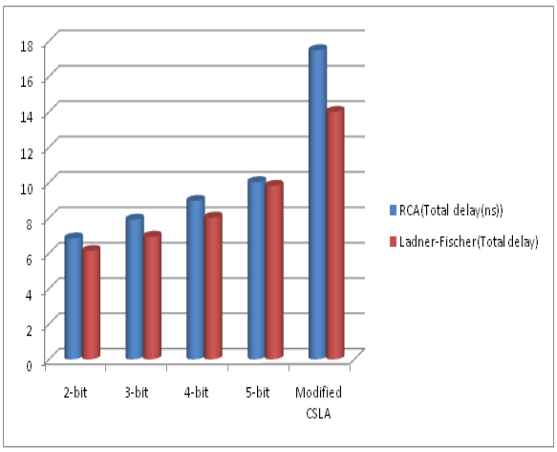


**Figure 12. Total delay values of different adders.**

## V. CONCLUSION

A new approach is proposed in this paper to reduce the delay of SQRT CSLA. The replacement of prefix adders in place of Ripple Carry Adders offers great advantage in the reduction of delay. The compared result shows that the proposed CSLA greatly reduces delay. The proposed CSLA architecture is therefore, faster because of less delay and area efficient for VLSI hardware implementations. It would be interesting to investigate the design of the proposed 128-b SQRT CSLA.

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