A Novel Rom-less Direct Digital Frequency Synthesizer based on Euler Infinite Series

U.Dinesh, Aravind Ram.S, M.Hariharan, K.Hariharan

***Abstract*—The traditional DDFS based on a look up table needs a large sized ROM and it is more complex. This paper deals with a novel ROM-less architecture based on the approximation of Euler's Infinite series. It has advantages of low complexity, low computational delay, and high spectral purity. The proposed DDFS has a high SFDR (spurious free dynamic range) when compared with [1] and the value is as good as 72.3dBc.**

***Index Terms*—Direct Digital Frequency Synthesis, Euler Infinite Series, low complexity, spectral.**

I. INTRODUCTION

Almost for all applications of communication system, there is a need to synthesize accurate waveforms of varying frequencies with low phase noise, low spur, and high frequency tuning resolution. In such applications, the mechanism to generate the waveform cost effectively is of significant concern.

The DDFS is a basic building block in all communication systems. The concept of DDFS was first framed by J.Tierney in 1971[2].Direct Digital Frequency Synthesis is a electronic means of generating samples and building arbitrary waveform out of those samples at different frequencies. A DDFS can provide fast switching [3] and high frequency resolution. Even DDFS is used in wireless transceivers [4] since the 1980's.

Traditional ROM based DDFS have several disadvantages like hardware complexity, high power consumption. Techniques like quarter wave symmetry, trigonometric approximations are used to reduce the size of ROM. However the quantization noise is introduced and limits the use of these techniques [5].The use of CORDIC algorithm introduces additional digital circuitry and path delays. In order to overcome all these problems, polynomial approximations for trigonometric functions were used. The accuracy of the output signal depends on the degree of the polynomial which in turn increases the hardware overhead for

better result [6].The proposed algorithm uses limited hardware with high speed based on the **approximation of Euler Infinite Series [7].**

Manuscript received on May, 2013.

U.Dinesh, Electronics & Communication Engg, Thiagarajar College of Engineering, Madurai, India.

Aravind Ram. S, Electronics & Communication Engg, Thiagarajar College of Engineering, Madurai, India.

M.Hariharan, Electronics & Communication Engg, Thiagarajar College of Engineering, Madurai, India.

K.Hariharan, Electronics & Communication Engg, Thiagarajar College of Engineering, Madurai, India.

II. CONVENTIONAL ARCHITECTURE

The conventional DDFS consists of a look up table where all the phase values of the sine wave are stored in an Erasable Programmable Read Only Memory (EPROM).

The phase accumulator generates the address for the LUT. The resolution of the DDFS depends with size of the memory employed. The phase accumulator keeps on adding its result with the frequency control word (FCW) until an arithmetic overflow occurs.

If TR is the tuning ratio, then the output frequency is given by, $f_{out} = \frac{TR * f_{clk}}{2^n}$, where $\frac{f_{clk}}{2^n}$ is the resolution compatible for the EPROM. The block diagram of the phase accumulator and the conventional DDFS block diagram are shown in Fig 1. and Fig 2. respectively.

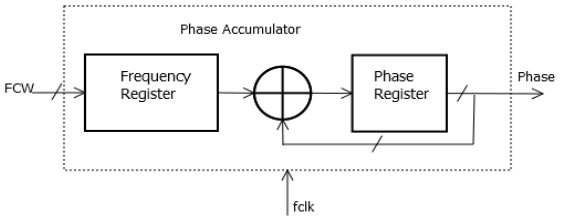

Fig 1. Phase Accumulator

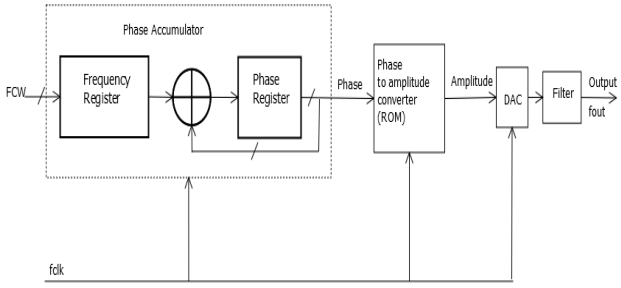

Fig 2. Block Diagram of a traditional DDFS

III. PROPOSED DDFS ALGORITHM

The proposed DDFS algorithm stands unique in two criteria without ameliorating the performance. First, the traditional ROM LUT is ignored by an approximation polynomial. Secondly, the hardware complexity is reduced when compared with [8].The resulting low power architecture meets the communication standards such as Bluetooth [9].

A. Euler Infinite Series Approximation

The Euler infinite series at a point x is given by,

$$\frac{\sin(x)}{x}=\left(1-\frac{x^2}{1.\Pi^2}\right).\left(1-\frac{x^2}{2^2.\Pi^2}\right).\left(1-\frac{x^2}{3^2.\Pi^2}\right).\left(1-\frac{x^2}{4^2.\Pi^2}\right).\left(1-\frac{x^2}{5^2.\Pi^2}\right)....\quad(1)$$

On truncating the equation up to 4 terms,

$$\frac{\sin(x)}{x}=\left(1-\frac{x^2}{1.\Pi^2}\right).\left(1-\frac{x^2}{2^2.\Pi^2}\right).\left(1-\frac{x^2}{3^2.\Pi^2}\right).\left(1-\frac{x^2}{4^2.\Pi^2}\right)\quad(2)$$

Fig 3.shows the sine wave based on (2).The deviation is approximated by changing the denominator values of each term so as to reduce the error.

The approximated equation is,

$$\frac{\sin(x)}{x}=\left(1-\frac{x^2}{1.\Pi^2}\right).\left(1-\frac{x^2}{(2.4).\Pi^2}\right).\left(1-\frac{x^2}{(6.7).\Pi^2}\right).\left(1-\frac{x^2}{(15.7).\Pi^2}\right)\quad(3)$$

Fig 4.shows the sine wave by approximated Euler Infinite Series. For hardware simplicity the equation is re arranged as,

$$\sin(x)=(\Pi.x).(1-0.4167x^2).(1-0.1492x^2).(1-0.0637x^2)\quad(4)$$

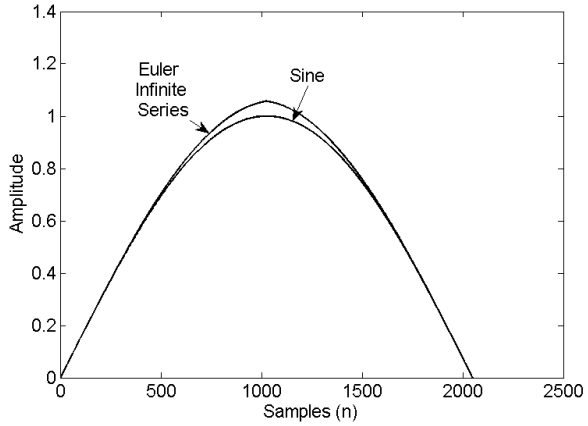

Fig 3.Sine wave based on (2) truncation of Euler Infinite Series

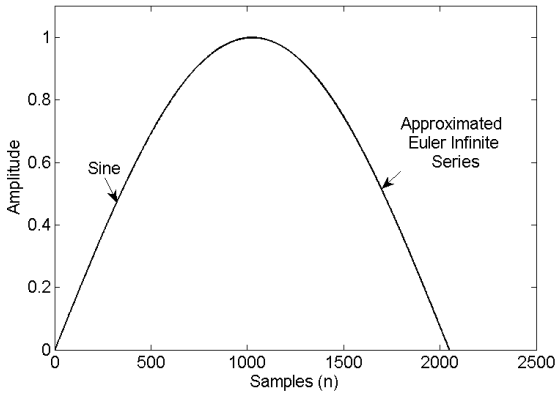

Fig 4.Sine wave based on (4) approximated Euler Infinite Series

In the above equation x varies between 0 and 1 producing a half sine wave in the interval (0,π).The other half is symmetrical in the interval (π,2π).

B. Proposed Architecture

Fig 5.represents the proposed architecture to implement the above algorithm. It consists of three blocks, namely, phase block, quadrant block and sine generator. It also has a ring counter, a 4X2 encoder, digital multiplexers and a DAC at the output stage. The frequency control word is given as an input to the phase accumulator which is present in the phase block.

The output from the comparator of phase block is fed to the quadrant block where the T-Flip Flop's output selects either the complemented or un-complemented output of the sine generator. The full cycle is generated by exploiting the symmetry of sine wave with respect to zero crossings over one full period [10].Thus the digital value is passed through the DAC to obtain the sine wave.

B1. Phase Block

The phase block consists of a phase accumulator, maximum range register(MRR) and a digital comparator as shown in Fig 6.The phase accumulator has an adder and a latch. The frequency control word is one of the inputs to the adder and the output of the latch is fed back to the other input of the adder. The FCW is added with the same value on each clock signal given by the encoder. The phase is quantized as,

$$x=n/2^N\quad(5)$$

where N is the size of the frequency control word and n is the value stored in the MRR. The phase accumulator gives a value in the range between 0 and 1 which when substituted in (4) gives the sine value ranging from 0 to π. The maximum range value to be stored is 1*2N. On each clock signal given by the encoder output to the latch of phase accumulator, the phase accumulator value (PAV) is compared with the MRR by the digital comparator. When they are equal, the comparator gives an active high signal (D) to reset the phase accumulator.

B2. Quadrant Block

The quadrant block consists of a T-flip flop and 2X1 MUX as shown in Fig 7.The T-input is always maintained in a logic 1.The clock terminal of the flip-flop is connected with the comparator output (D). Therefore whenever a positive clock edge appears the output is toggled. The output of the flip-flop goes through the select line of the 2X1 MUX. The output of the MUX goes to the DAC.

The phase block is designed in such a way that it generates values from 0 to 1 which is for 0 to π and for a full sinusoidal signal these values has to be regenerated again. The first quadrant values are obtained by the sine generator whose output is sent through the first input of the 2X1 MUX. The second input also gets the same output from the sine generator but with an additional 2's complement. The 2X1 MUX selects the complemented or uncomplemented value according to the T-Flip Flop's state.

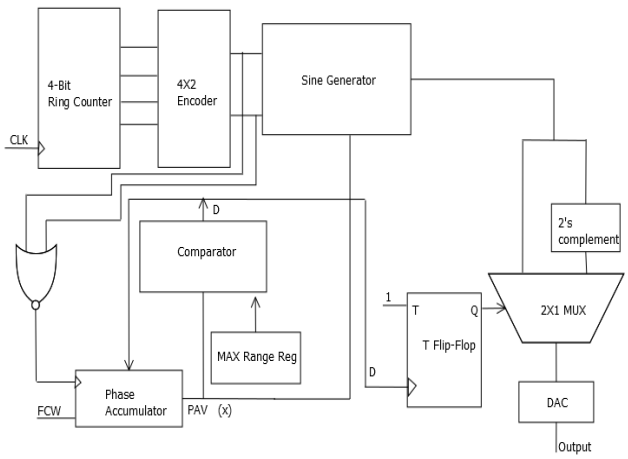

Fig 5.Proposed DDFS Architecture

Published By:
Blue Eyes Intelligence Engineering
& Sciences Publication

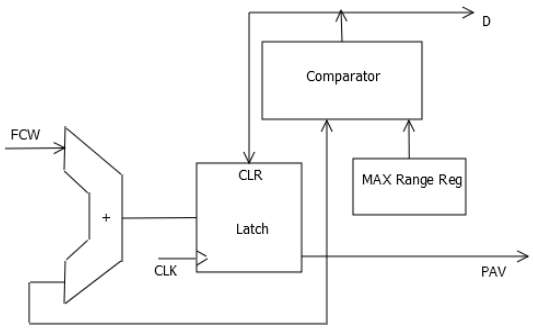

Fig 6. Phase Block

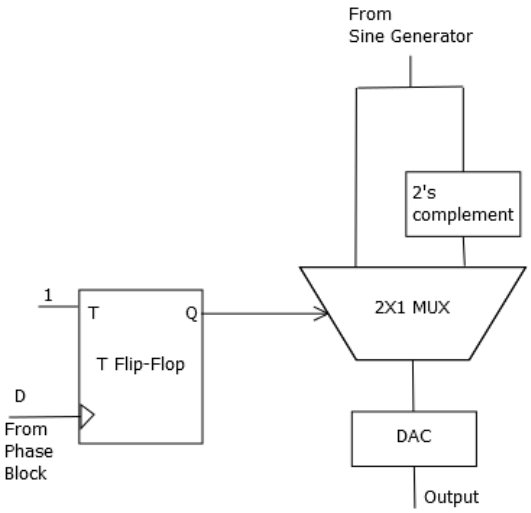

Fig 7. Quadrant Block

B3. Sine Generator

The initial part before the sine generator has two blocks namely, the 4-bit ring counter and a 4X2 encoder. The master clock signal is given to the 4-bit ring counter. The four output signals are given to the 4X2 encoder. Thus the four possible outputs of the ring counter 1000,0100,0010,0001 are encoded as 00, 01, 10, and 11 respectively.

The sine generator consists of a 4X1 MUX, a 1X4 DE-MUX, few registers, multipliers and an adder as shown in Fig 8.The encoder outputs are the select lines for both the MUX and the DE-MUX. The four inputs of the MUX are four registers namely a, b, c, d which holds the coefficients of the x^2 of all the terms in (4).The output of the MUX is multiplied with x^2 and added with 1 by an adder. The registers a, b, c, d are multiplied with x^2 sequentially according to the select lines with respect to the encoder output.

The de-mux's output has two registers R1 and R2 where R1 is connected with the first output and remaining outputs are connected with R2.Both the registers are multiplied and the result is stored in R3.The result is fed back to R1.Similarly, as said above for the MUX, the DE-MUX select lines comes from the encoder and the output of the first stage stored in R1 and thereafter the outputs are stored in R2.

The R3 is multiplied with (π*x) and given as the first input in the 2X1 MUX. The second input of the MUX is the same with the addition of the 2's complementer. The output of the 2X1MUX is connected to the DAC. Thus the full sine wave is generated.

IV. COHERENT SAMPLING

Frequency domain analysis is essential in characterizing a data converter which requires spectrally pure signal (IEEE1241).Coherent sampling is a method of sampling the periodic signal, where an integer number of cycles fit into a predefined sampling window. Non coherent sampling introduces spectral leakages during the spectrum estimation of the device under the test. Windowing and Coherent sampling prevents this problem.

For obtaining coherent sample, the FCW must satisfy the condition,

$$(360\%FCW) = 0 \qquad (6)$$

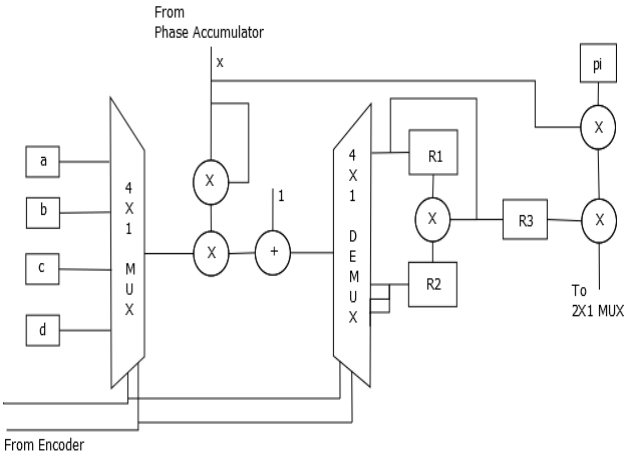

Fig 8. Sine Generator

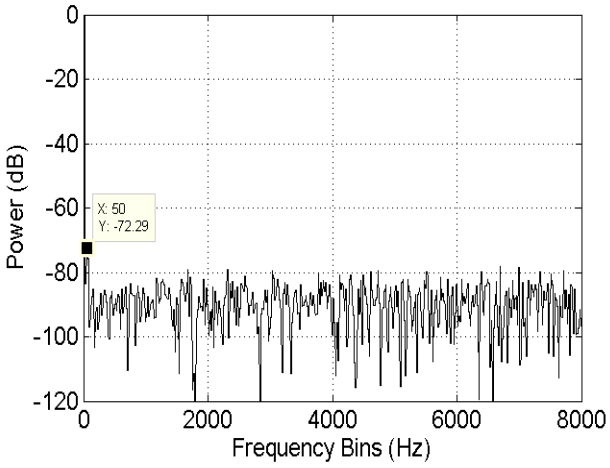

Fig 9.Spectrum of the Proposed DDFS

Table-1 Comparison of performance based on SFDR

Reference	Type	SFDR
Ours	Euler Infinite Series	72.3 dBc
Ref.[11]	Rom less	35dBc
Ref.[12]	Time Domain Interpolator	50dBc
Ref[13]	ROM-Look UP	64.5dBc

V. EXPERIMENTAL RESULTS

The MATLAB is used to simulate the above proposed algorithm. The number of bits of the DAC is 8.The signal to noise ratio of the DAC obtained was 49.3dB which coincides with the theoretical formula 6.02N+1.76dB, where N is the

number of bit of the DAC. The architecture is also coded in Verilog and implemented in the Altera FPGA DE1 kit and results were verified. The spectrum of the sine wave is shown in the Fig 9.The maximum spurious free dynamic range (SFDR) measured from the spectrum was 72.3dBc.Our proposed paper has high spectral purity which can be seen from the Table-1.

VI. CONCLUSION

Low complexity DDFS architecture has been proposed in this paper. The proposed method avoids the use of large sized memory and involves less hardware in generating a sine wave. Still, a high speed system can be achieved by reducing the hardware overhead while maintaining the spectral purity to 72.3dBc.Therefore it can be used as a basic building block of a communication system.

REFERENCES

[1] M. Kesoulis, D. Soudris, C. Koukourlis and A.Thanailakis, 'Systematic methodology for designing low power direct digital frequency synthesizers', lET Circuits Devices Syst., 4, p.293 (2007).

[2] J.Tierney, C.M.Radre and B.Gold,'A Digital Frequency Synthesizer', IEEE Transactions on Audio and Electroacoustics, March 1971.

[3] Avanindra Madisetti, Alan Y Kwentus, Alan N Wilson, 'A 100-MHz, 16-b, Direct Digital Frequency Synthesizer with a 100-dBc Spurious-Free Dynamic Range', IEEE Journal of solid-state circuits, vol 34, 8 August 1999, pp 1034-1043.

[4] D.Soudris, M.Kesoulis, C.Koukourlis, A.Thanailakis and S.Blionas, 'Alternative Direct Digital Frequency Synthesizer Architectures with Reduced Memory Size', Proceedings of The 2003 IEEE International Symposium on Circuits and Systems, vol 2,pp 73-76.

[5] J.Vankka, 'Methods of mapping from phase to sine amplitude in direct digital frequency synthesis', IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control, vol 44,no.2,pp.526-534,(1997)March.

[6] Kenneth A.Essenwanger, Victor S.Reinhardt, 'Sine Output DDSs A Survey Of The State Of The Art', IEEE International Frequency Control Symposium(1998)

[7] Paul Trow's Math Page, 'A Famous Infinite Series', March 25,2013,http://ptrow.com/articles/Infinite_Series_Sept_07.htm

[8] Run Xing, Xiao-tong Zhang, Han Li, Qin Wang and Zhan-cai Li, "An Area Optimized Direct Digital Frequency Synthesizer Based on Improved Hybrid CORDIC Algorithm", IEEE Proceedings of International Workshop on Signal Design and its Applications in communications,pp.243-246 (2007).

[9] Tze-Yun Sung,Lyu-Ting Ko and His-Chin Hsin, "Low Power and High SFDR Direct Digital Frequency Synthesizer Based on Hybrid CORDIC Algortihm", IEEE International Symposium on Circuits and Systems,pp.249-252 (2009).

[10] Shu-Chung Yi, Kun-Tse Lee, Jin-Jia Chen, Chien-Hung Lin, NCUE, Changhua, Taiwan 500,ROC,"A low power efficient direct digital frequency synthesizer based on new two-level lookup table", IEEE CCECE/CCGEI, Ottawa (2006) May.

[11] Yu Xuefeng, Dai Foster, Shi Yin, Zhu Ronghua,"2 GHz 8-bit CMOS ROM-less direct digital frequency synthesizer", ISCAS 2005 IEEE International Symposium on Circuits and Systems, Vol 5,pp.4397-4400.

[12] Heiskanen Antti, Mantyniemi Antti, Rahkonen Timo E,"A 30 MHz DDS Clock Generator with 8-bit,130ps delay generator and -50dBc spurious level", Proceedings of the 27th European Solid State Circuits Conference,2001.

[13] "Qualcomm 2368 Dual Direct Synthesizer", Synthesizer Products Data Book, 80-24127-1 A, 8/97.

[14] K.Hariharan, E.Benitta Hubert, K.V.O.Divyalakshmi,K.Shamalla and V.Abhai Kumar, "Coherent Sinusoid Generation using Novel DDFS Architecture", Internation Journal of Smart Home,Vol.6,No.1,January 2012.

U.Dinesh is pursuing Bachelor's degree in Electronics & Communication Engineering at Thiagarajar College of Engineering, Madurai, Tamil Nadu, India. His areas of interest include Embedded Systems, VLSI,DSP and microcontrollers.

Aravind Ram.S is pursuing Bachelor's degree in Electronics & Communication Engineering at Thiagarajar College of Engineering, Madurai, Tamil Nadu, India. His areas of interest include Embedded Systems, VLSI, microprocessors and microcontrollers.

M.Hariharan is pursuing Bachelor's degree in Electronics & Communication Engineering at Thiagarajar College of Engineering, Madurai, Tamil Nadu, India. His areas of interest include Embedded Systems, VLSI, Signal Testing, Microprocessors and microcontrollers.

Dr.K.Hariharan is an Assistant Professor in Electronics and Communication Engineering at Thiagarajar College of Engineering, Madurai, TamilNadu, India. He received the Bachelor's degree in Electronics and Communication Engineering from the Madras University, India in 1998 and the M.E., degree in Thiagarajar College of Engineering. He obtained his PhD degree from Thiagarajar College of Engineering, Madurai, TamilNadu, India. His research interests include digital computer architectures, VLSI system design, mixed signal IC testing and embedded system design. He has registered two Indian patents in these relevant areas.