2- Bit Comparator Using Different Logic Style of Full Adder

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Abstract- In this paper a new design of comparator is described with the help of Full adder which are the basic building block of ALU and ALU is a basic functioning unit of the microprocessors and DSP. In the world of technology it has become essential to develop various new design methodologies to reduce the power and area consumption. In this paper comparator are developed using various design of full adder. This will reduce the power of the comparator design. The proposed comparator has been designed using DSCH 3.1 and Microwind 3.1 at 120 nm technologies. The developed comparator with show an improvement of 25.14% in power.

Keywords: Full adder, nmos, pmos, cmos, speed, low power, less transistor count, efficiency.

I. INTRODUCTION

The Comparator is a very basic and useful arithmetic component of digital systems. There are several approaches to designing CMOS comparators, each with different operating speed, power consumption, and circuit complexity. One can implement the comparator by flattening the logic function directly [1-6]. Full adder is one of the basic building blocks of many of the digital VLSI circuits. Several refinements have been made regarding its structure since its invention. The main aim of those modifications is to reduce the number of transistors to be used to perform the required logic, reduce the power consumption and increase the speed of operation. One of the major advantages in reducing the number of transistors is to put more devices on a single silicon chip there by reducing the total area. One of the ways to reduce power is to explore new types of circuits in order to find better circuit techniques for energy savings. In this paper, we propose several design techniques for high performance and power-efficient CMOS comparators.

Here we use Microwind to draw the layout of the CMOS circuit. In digital system, comparison of two numbers is an arithmetic operation that determines if one number is greater than, equal to, or less than the other number [7-12].So comparator is used for this purpose. Magnitude comparator is a combinational circuit that compares two numbers, A and B, and determines their relative magnitude. The outcome ofcomparisonThe outcome of comparison is specified by three binary variables that indicate whether B>A, A=B.

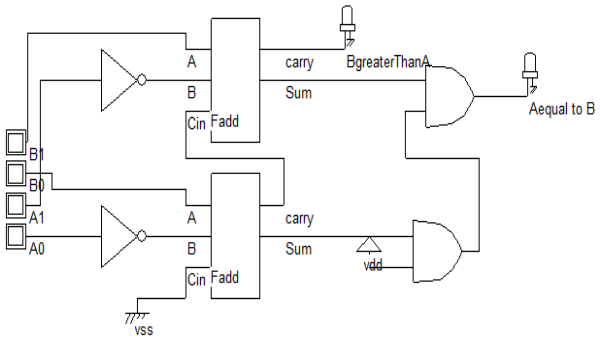

Fig.1. full adder based 2-bit comparator

Full adder based comparator is a 2-bit comparator consist of 2 full adders, 2 inverters at one of the input
And 2 and gate at the output side. There are two outputs.One shows A=B and another shows B>A .Truth table of full adder based comparator is as shown below

Table.1. truth table of full adder based 2-bit comparator

A1	A0	B1	B0	B>A	A=B
0	0	0	0	0	1
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	1	0
0	1	0	0	0	0
0	1	0	1	0	1
0	1	1	0	1	0
0	1	1	1	1	0
A1	**A0**	**B1**	**B0**	**B>A**	**A=B**
1	0	0	0	0	0
1	0	0	1	0	0
1	0	1	0	0	1
1	0	1	1	1	0
1	1	0	0	0	0
1	1	0	1	0	0
1	1	1	0	0	0
1	1	1	1	0	1

II. RELATED RESEARCH WORKS

A basic full adder has three inputs and two outputs which are sum and carry. The logic circuit of this full adder can be implemented with the help of XOR gate, AND gates and OR gates.

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The logic for sum requires XOR gate while the logic for carry requires AND, OR gates. The basic logic diagram for full adder using its Boolean equations with basic gates can be represented as shown below.

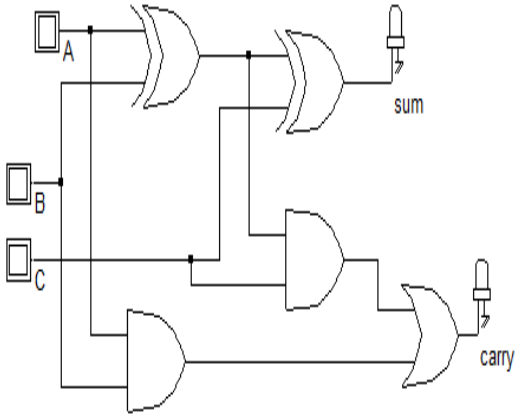

Fig.2.Logic diagram of basic full adder

The XOR gate is the basic building block of the full adder circuit. The performance of the full adder can be improved by enhancing the performance of the XOR gate. Several refinements have been made in its structure in terms of transistors to increase the performance of full adder. The early designs of XOR gates were based on eight transistors or six transistors that are conventionally used in most designs. The main intention of reducing this transistor count is to reduce the size of XOR gate so that large number of devices can be configured on a single silicon chip. There by reducing the area and delay. There by educing the area and delay. reducing the area and delay.

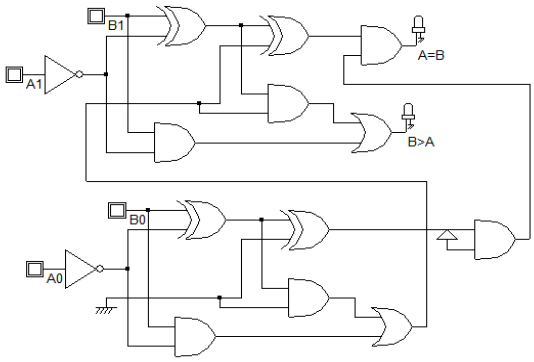

Fig.3.Logic diagram of basic full adder comparator

The layout design of the basic full adder based comparator is shown in fig.4... layout is the general concept that describes the geometrical representation of the circuits by the means of layers.Different logical layers is used by designers to generate the layout.

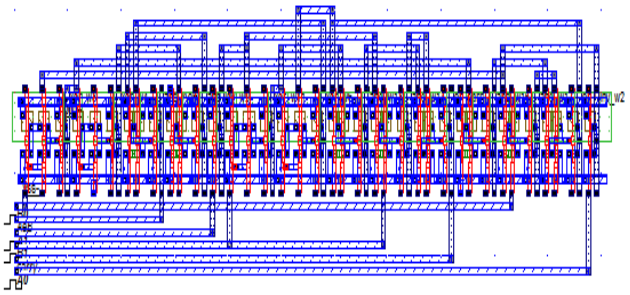

Fig.4.layout design of basic full adder based comparator

The logic diagram of hybrid comparator is as shown below .this logic style consist of two xor gate and one multiplexer.

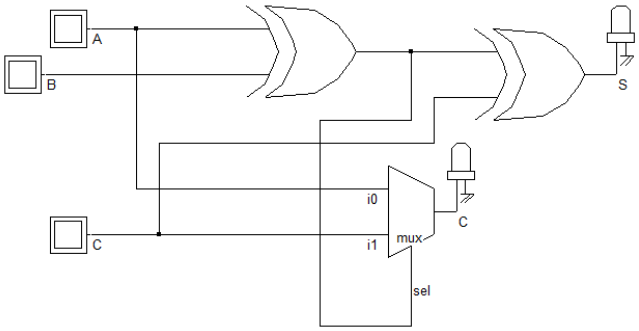

Fig.5.logic diagram of hybrid comparator

The comparator using hybrid full adder is shown in fig.6.the comparator consumes more power and area as compared to the basic full adder based comparator. It consists of four xor gate, two multiplexer, two not gate and two AND gate. Comparator has four input (A1, A0, B1, B0) and two output (A=B, B>A).

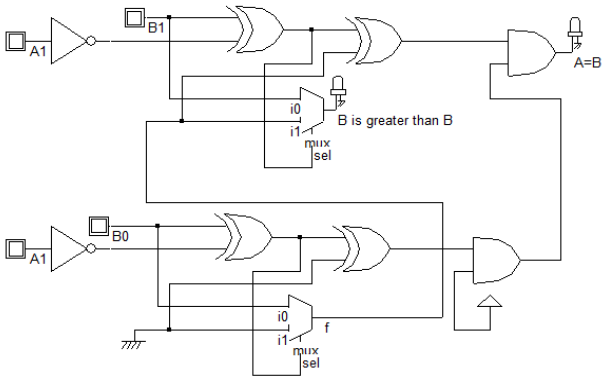

Fig.6.logic diagram of hybrid full adder based comparator

The layout design of hybrid full adder based Comparator is shown in fig.7.

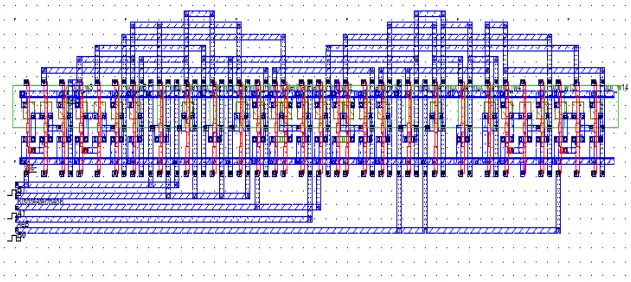

Fig.7.layout design of hybrid full adder based comparator

III. PROPOSED WORK

Proposed work of comparator is based on another logic style of full adder.thislogic style of comparator provides less power consumption than other logic styles described in this paper. The implementation of new logic full adder based comparator is shown in fig.9.It consists of two full adders, two not gates at one of the input and two AND gates at the output of the comparator. It has four input (A1, B1, A0, B0) and two output (A=B, B>A).

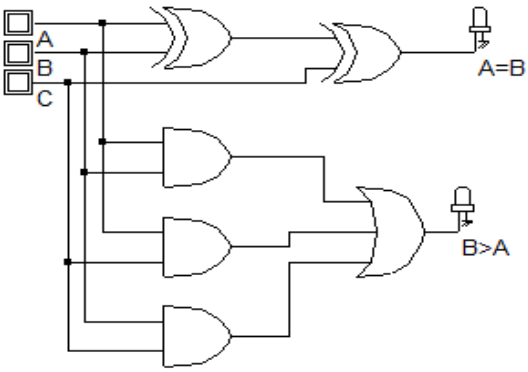

Fig.8.logic diagram of full adder using logic

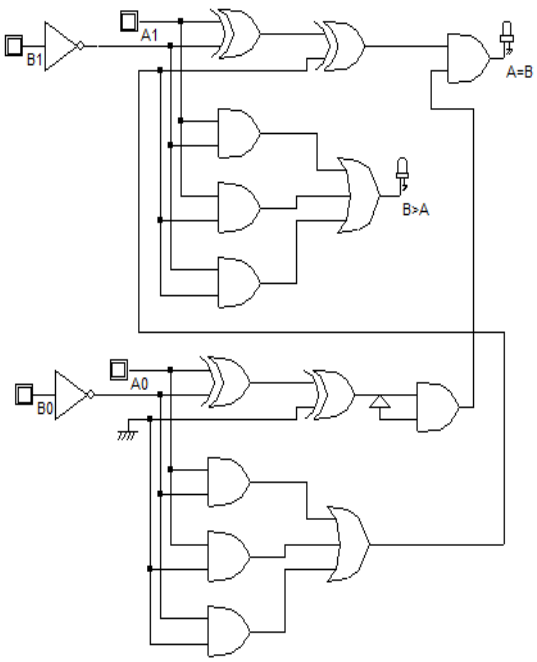

Fig.9.logic diagram of proposed full adder based comparator

The layout design of comparator using another logic of full adder is shown in fig.10.layout is the general concept that describes the geometrical representation of the circuits by the means of layers and polygons. Different logical layers are used by designers to generate the layout. Different logical layers are used by the designers to generate the layout.

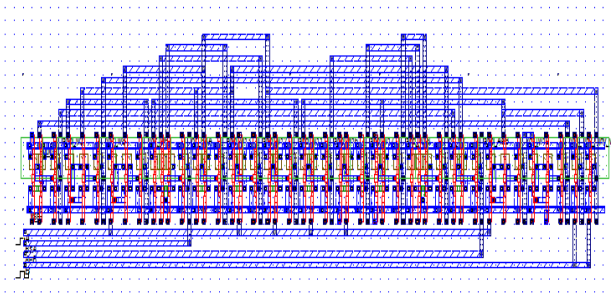

Fig.10.layout design of proposed full adder based comparator

IV. ANALYSIS AND COMPARISON

Analysis and comparison of different logic styles of comparator using various logic styles of full adder is shown in table.2. Simulations are obtained in Microwind Tool. First step in obtaining the simulations is to compile the Verilog file in Microwind 3.1. Verilog file is created from the circuit diagram, which is designed in the schematic. The Verilog file is now compiled in Microwind 3.1. After the compilation of Verilog file, the layout for the circuit diagram drawn in schematic will be generated in Microwind. After that simulations are performed on the layout generated using Verilog files. The results are simulated at room temperature.

Table.2.Simulation results of various full adder based comparator

	Basic comparator	Hybrid comparator	Proposed comparator
Routed wires	25	36	30
Width	33.7	64.4	77.9
Height	9.8	9.4	10.3
Area	331.8	603.2	803.7
Power	27.725	42.480	26.286

V. CONCLUSION

This paper describes different logic styles of full adder for designing a comparator for low Power Consumption. Basic full adder based comparator Logic Style provides low power and area design as compared to other Logic Style. Hybrid comparator logic style provides high power consumption & area. The proposed comparator consumes less power as compared to other logic styles. But the area consumption is greater than basic full adder based comparator. By using the proposed architecture the power is reduced up to 0.439 mw and area is increased up to 602.6 μm² than the other logic styles. Future scope for this paper is area reduction.

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