A Novel High ICMR and High Frequency Response of an Inverting Summing OpAmp

Dhanalakshmi Manikyam, Ganesh Kumar Ganjakunta

Abstract — In this paper, we propose a novel high ICMR (input common mode range) and high frequency response of an inverting summing pomp (operational amplifier). While selecting an operational amplifier for circuit design the most critical parameters must be consider. Some of the parameters are supply voltage, gain-bandwidth product, input noise voltage, slew rate, PSRR (power supply rejection ratio) and CMRR (common mode rejection ratio). The most important parameter is input common mode range, if we violate this parameter leads an undistorted waveform at the output stage. This leads an impact on the frequency response. Perhaps too much capacitance on the output stage causing clipping or oscillations on the output waveform. This paper work estimates the increasing the ICM range value by cascading the output stage combined with unusual implementation of differential amplifier to get better frequency response than conventional inverting summing operational amplifier.

Index Terms−amplifier, CMRR, Gain, ICMR, OpAmp.

I. INTRODUCTION

High element densities in CMOS circuits entail lower power consumption of the circuit. Further, smaller component dimensions entail the use of lower supply voltages requires the lower breakdown voltages. It is anticipated that supply voltages will go down from 4.5-5v to 0.9-1v. These technologies affect the fundamental limits in the design of analog circuits[2].

Why low voltage circuits are needed :

1) The device channel length is very small scaled down to submicron and the gate oxide thickness becomes nanometre thick, the supply voltages has to be reduced this ranges from 5V to 3V and even to 2V

2) A silicon chip dissipates a limited amount of power per unit area. So, dissipation amount of power should be reduced in order to avoid overheating of the device.

3) In order to make the device portable, battery powered equipment needs low power to ensure an acceptable operation and the supply voltage is minimum.

Conventional inverting summing operational amplifier have poor large signal behavior since their tail currents are constant, results limited slew-rate[4]. The input stage of OpAmp is to amplify differential signals and reject common mode range voltage. The typical implementation of the differential pair using p- channel pair and n-channel pair is shown in Figure 1. [1].
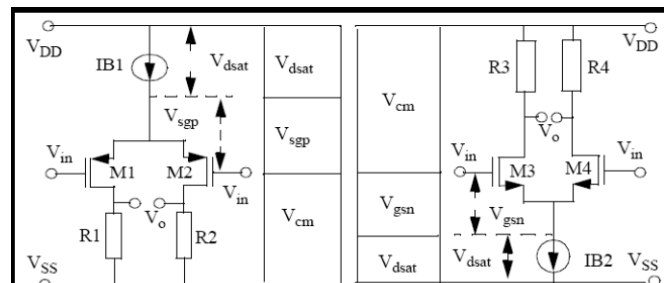
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Figure 1. The common-mode input range of a p-channel and an n-channel differential pair

For an n-channel pair, the common mode input voltage range is given by:

$VSS + Vgsn + Vdsat \leq Vcommon \leq VDD$

Where *Vcommon* is the common mode input voltage,

Vsgp is the source-gate voltage of an input transistor,

Vdsat is the voltage across a current source,

VDD is the positive supply voltage,

and *VSS* is the negative supply voltage.

For a p-channel input pair, the common mode input voltage is given by:

$VSS \leq Vcommon \leq VDD– Vdsat – Vsgp.$

Where *Vgsn* is the gate source voltage of an n channel input transistor.

II. CONVENTIONAL INVERTING SUMMING AMPLIFIER

The conventional inverting summing OpAmp uses different types of operational amplifier like TLC2272, OPA333, OPA735 etc uses different supply voltage rails which are not use in low voltage and low power applications.
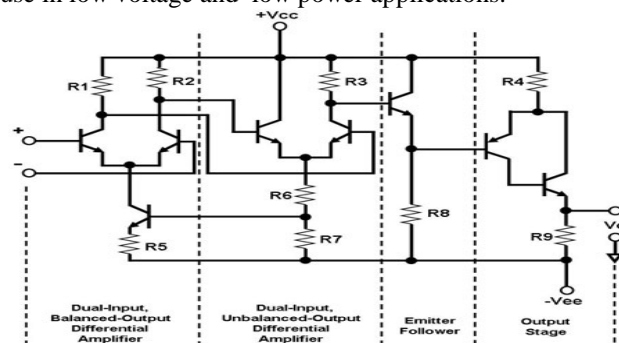

Figure 2. conventional operational amplifier using BJT'S

The above Figure 2 shows the circuit arrangement of conventional operational amplifier using BJT's having the stages of Dual-input, Balanced-output differential amplifier, Dual-input, Unbalanced-output differential amplifier, Emitter follower and output stage. The

large resistor values require a high biasing circuit. In low power applications the supply voltage should be minimum. The proposed inverting summing OpAmp uses the folded cascode operational amplifier works under the supply voltage of 2V in vdd and vss.

III. FOLDED CASCODE OPERATIONAL AMPLIFIER

The folded cascade operational amplifier does not require perfect balance of current in differential amplifier because the more dc current can flow in the current mirror circuit in the operational amplifier. The two drains of M1 and M2 are connected to drains of M4 and M5, so the dc current through current mirror never Zero. If this current is Zero it is require larger time to turn On the current mirror circuit[1]. This OpAmp itself provides the gain of two stage amplifier.

The Figure 3 shows the circuit arrangement of folded cascade operational amplifier having three biasing voltages stabilizes the dc current through the current mirror circuit and will not be Zero.
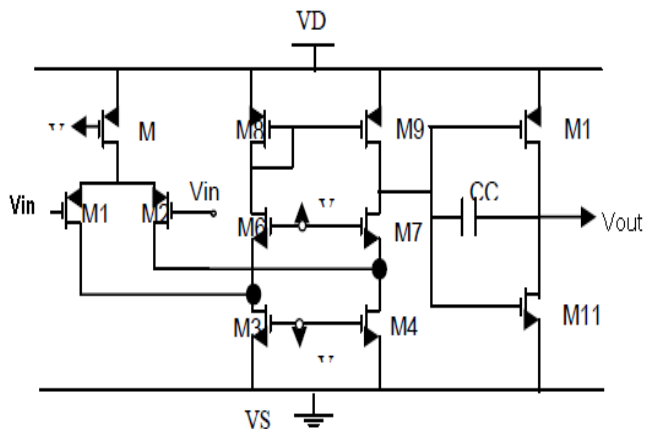

Figure 3. Folded cascode operational amplifier

The bias circuit uses the MOSFET's with the independent current source of 1uA. By combining the Figure 3 and Figure 4 , the complete circuit of inverting summing amplifier was designed and is shown in simulation results.
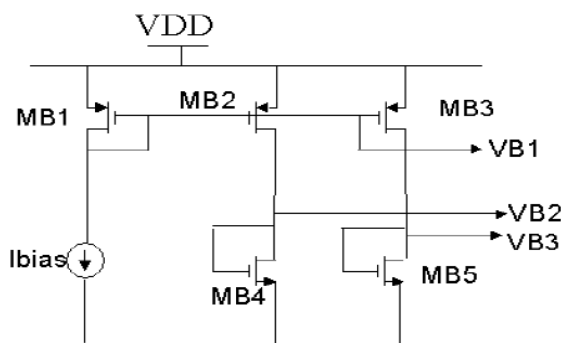

Figure 4. Bias circuit

IV. PROPOSED INVERTING SUMMING OPAMP

The proposed inverting summing amplifier was shown in Figure 5. Here the external circuit was designed to get the summation at the output stage with inversion mode. The two input signals are given through the 1Kohm resistor and the feedback resistor uses 2Kohm resistor. There by the total summation will perform by adding the input voltages with the

gain of operational amplifier.
The bias current is 1uA
The load capacitor is 10pf
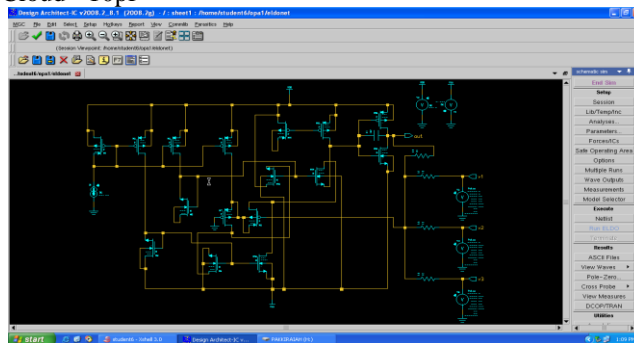Positive Power supply is 2v
Negative Power supply is -2v
Cloud= 10pf

Figure 5. Complete schematic of an inverting summing OpAmp

V. SIMULATION AND RESULTS

The inverting summing amplifier was designed using HSPICE tool and the schematic uses IC station in Mentor Graphics.
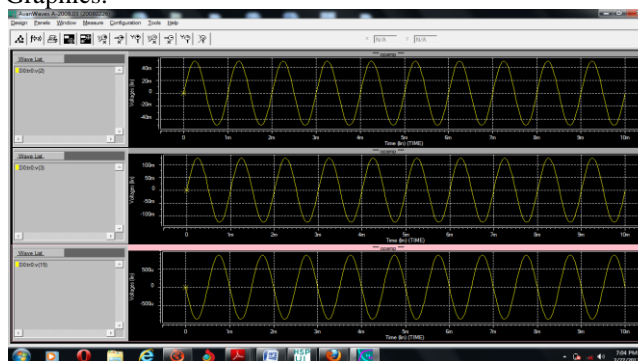

Figure 6. Output Response of Proposed Inverting Summing OpAmp

In convectional inverting summing operational amplifiers due to the limited ICMR the output may clipped or nonlinearity. The simulated result of Figure 6 gives the linear waveform with in the ICMR of the operational amplifier. The gain of the circuit will be increased over the range of frequencies.
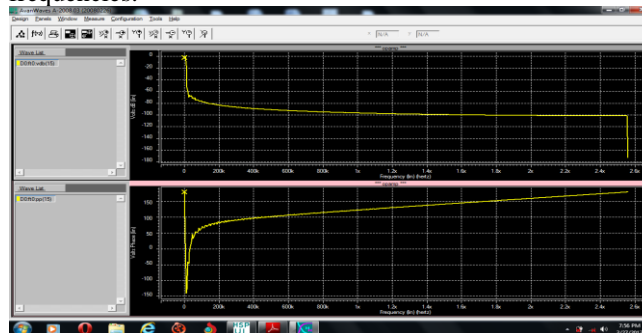

Figure 7. Frequency response of proposed inverting summing OpAmp

The Figure 7 shows the frequency response of the proposed system gives a 100db gain over the range of frequencies. Whereas the conventional inverting summing operational amplifier gives 102db gain, but this gain is at one particular

frequency after the gain falls rapidly. So the proposed circuit the gain is linear from kHz to Mhz.

VI. CONCLUSION

 The proposed inverting summing operational amplifier using folded cascode operational amplifer gives high ICMR range their by we can obtain high input common mode range and better frequency response over the range of frequencies than conventional inverting summing pomp's using different operational amplifier IC versions.

This inverting summing OpAmp has a great application in audio signal mixing and wide use in analog and digital signal mixing. The simulation results can also get from PSPICE for better result approximation we used HSPICE for frequency response analyzer.

VII. ACKNOWLEDGMENT

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