Low Voltage, High Bandwidth & Input Impedance CMOS Differential Amplifier at NANO Scale

Adil Zaidi, Divakar Veer Vikram Singh, Firoz, Dileep Kumar, Veerendra Pratap

Abstract—Since analog circuits have proved primarily essential in many of today’s high performance systems. This paper demonstrate designing and simulation of low power CMOS technology based differential amplifier at nano scale of different channel length (45nm, 32nm, 22nm) via applying various supply voltages i.e. 1.1V, 0.95V, 0.9V respectively. Here the high input impedance, low power dissipation circuit is mainly characterized in terms of common mode rejection ratio (CMRR), voltage gain and gain band width product. The input impedance calculated are in the range of 190 GΩ (giga ohm), cut off frequency (-3db) approximately greater than 50 MHz (mega hertz) and average power dissipation in the order of less than 130 µw (micro watt). The simulation result shows that all transistors are operated in saturation region, with this unique behavior of MOSFET transistor operating in this region not only allows a designer to work at a low voltage but also at a high frequency. Finally, the analog design consists of low operating voltages via very deep sub micron (nano scale) technology. The simulation is carried out using PTM Low Power 45nm, 32nm, & 22nm Metal Gate / High-K / Strained-Si technology with H-spice. A Matlab tool is also used to plot the graph of various parameters at different channel length in two dimensions (2-D).

Index Terms—Very deep sub-micron (VDSM), Nanoelectronics, Scaling.

I. INTRODUCTION

The great progress toward building electronic circuits integrated on the nanometer scale has opened the possibility for shrinking drastically the size and power consumption of large-scale, general-purpose electronic memories and processors. These recent advances in nano fabrication and nano electronics could have conspicuous, pervasive impacts for general purpose computing in several years time. However, these advances also make it possible to shrink the form factor and power requirements for a wide class of much simpler circuits.

Such circuits often are dedicated to specialized applications in the control and monitoring of other systems [1]. CMOS technology has been widely used for various RF applications, such as cellular phone, WLAN, and Bluetooth, due to its super integration scale and powerful on-chip digital signal processing capability [2]. The demand of low voltage, low power and high performance are great challenges for the engineering of sub 50nm gate length. CMOS device of the increasing interest and necessities of nomadic electronic systems [3].

Designing high performance analog integrated circuits is becoming increasingly exigent with the relentless trend toward reduced supply voltages and transistor channel length. A large part of the success of the MOS transistor is due to the fact that it can be scaled to increasingly smaller dimensions, which results in higher performance. The feature size of individual transistor is shrinking from deep sum-micrometer (DSM) to even nanometer region. As the scale of integration improves, more transistors, faster and smaller than their predecessors, are being packed into a chip. This leads to the steady growth of the operating frequency and processing capacity per chip [4,5,6,7]. Impact of scaling is characterized in terms of several indicators:

- Minimum feature size
- Number of gates on one chip
- Power dissipation
- Maximum operational frequency
- Production cost

The differential amplifier is one of the most versatile circuits used in analog circuit design. These are widely used in the electronics industry and are generally preferred over their single-ended counterparts because of their better common-mode noise rejection, reduced harmonic distortion, and increased output voltage swing. Differential amplifiers are used to amplify analog as well as digital signals, and can be used in various implementations to provide an output from the amplifier in response to differential inputs [2]. Current mirrors are used extensively in CMOS analog circuits both as biasing elements (NMOS) and as active loads (PMOS) to obtain high AC voltage gain enhancement mode transistors remain in saturation when the gate is tied to the drain

\[ V_{DS} > V_{GS} - V_{th} \]  \hspace{1cm} (1)

Based on Eq.1 constant current sources are obtained through current mirrors designed by passing a reference current through a diode-connected (gate tied to drain) transistor.
The objective of the differential amplifier is to amplify the difference between two different potentials regardless of common mode value. For ideal differential amplifier, the common mode gain is zero which makes the CMRR infinite. The input offset voltage is also zero for the ideal case. The common mode gain is zero which makes the CMRR infinite.

The differential amplifiers are used to amplify analog as well as digital signals, and can be used in various implementable applications so as to provide an output from the amplifier in desired response to the differential inputs. It is also very compatible with integrated circuit technology and serves as the input stage to most of operational amplifier. These circuits can be readily adapted to behave as an operational amplifier, a comparator, an instrumentation amplifier, etc. The differential amplifier is often a building block or sub-circuit used within high-quality integrated circuit amplifiers, linear and nonlinear signal processing circuits, and even certain logic gates and digital interfacing circuits in various VLSI applications.

Differential amplifier gain-

\[ A_d = \frac{V_{out}}{V_{id}} = g_m (R_D // r_o) \]

Where:

- \( A_d \): differential gain, \( V_{out} \): output voltage, \( V_{id} \): differential input, \( g_m \): transconductance, \( R_D \): drain resistance, \( r_o \): output resistance

**II. MODELING & DESIGNING OF CMOS DIFFERENTIAL AMPLIFIER AT NANO SCALE**

This manuscript investigates a high impedance, low power and high bandwidth differential amplifier dc, transient and ac analysis designed at 45nm, 32nm, 22nm respectively where DC analysis explain the transfer characteristics (output voltage versus input voltage), transient analysis describes time domain approach and AC analysis includes frequency domain study.

The paper is classified as follows: section II includes the modeling of differential amplifier at nano scale. Section III describes simulated characteristics i.e. DC, Transient & AC analysis curves at different channel length (45nm, 32nm, 22nm) in nanometer range correspondingly. Section IV includes results and discussion, section V contains acknowledgement followed by references in section VI.

**Fig.1.1 Active load (P-MOS current mirror)**

**Fig.1.2 Bias element (N-MOS current mirror)**

**Fig2.1 CMOS DIFFERENTIAL AMPLIFIER WITH ACTIVE LOAD**

The voltage developed across the diode-connected transistor is applied to the gate and source of the second transistor, which provides a constant output current. Since both the transistors have the same gate to source voltage, hence both transistors will be in the saturation region. The current ratio \( I_{OUT}/I_{REF} \) is determined by the aspect ratios of the transistors. For identical sized transistors, the ratio is unity, which means that the output current mirrors the input current. Because the physical channel length that is achieved can vary substantially due to process variations, the accurate ratios usually result when devices of the same channel length are used, and the ratio of currents is set by the channel width [11].

Active load differential amplifier has better performance only if all transistors are identical. The use of identical transistors leads to no mismatch, hence offset voltage becomes zero, but practically it is not possible. Practical differential amplifiers have non-zero common mode gain, therefore, the CMRR becomes finite and they have non-zero offset voltage. The circuit arrangement for CMOS differential amplifier with active load and single ended output is shown in Figure. 1. To achieve better performance in voltage gain, bandwidth and gain bandwidth product, all transistors should be in saturation region.[5,12,13] CMOS design is becoming increasingly blurred, especially with the challenges presented by very deep sub-micron (VDSM) fabrication technologies, very low operating voltages, and operating frequencies extending well into GHz range while analog figure of merit, such as transistor gain and output swing are degraded [5,6,12,14].
Common mode gain:-
\[ A_{cm1} = A_{cm2} = \frac{v_{cm1}}{v_{cm2}} = \frac{\frac{1}{g_m} + \frac{R_D}{2R_{ss}}}{A_{gm}} \]
Where:
\[ A_{cm1}, A_{cm2} \text{ common mode gain} \]
\[ R_{ss}, \text{source resistance} \]

CMRR (Common mode rejection ratio):-
\[ CMRR = \frac{A_{d1}}{A_{cm1}} = \frac{A_{d2}}{A_{cm2}} = g_m R_{ss} \]

III. SIMULATION CHARACTERISTICS

H-spice tool is used for simulation of CMOS differential amplifier. Apart from this matlab tool is also used for plotting graph in ac analysis. Simulation section is divided into three parts: - DC, transient, and AC analysis at 45nm, 32nm, 22nm respectively.

1) DC ANALYSIS:-

1.1 Input parameters

<table>
<thead>
<tr>
<th>Technology</th>
<th>At 45nm</th>
<th>At 32nm</th>
<th>At 22nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdd</td>
<td>0.1v</td>
<td>0.1v</td>
<td>0.1v</td>
</tr>
<tr>
<td>RL</td>
<td>100K</td>
<td>100K</td>
<td>100K</td>
</tr>
<tr>
<td>CL</td>
<td>100f</td>
<td>100f</td>
<td>100f</td>
</tr>
<tr>
<td>Vdd</td>
<td>1.1V</td>
<td>0.95V</td>
<td>0.9V</td>
</tr>
<tr>
<td>Vss</td>
<td>-1.1V</td>
<td>-0.95V</td>
<td>-0.9V</td>
</tr>
<tr>
<td>Iref</td>
<td>10u</td>
<td>10u</td>
<td>10u</td>
</tr>
</tbody>
</table>

1.2 DC transfer curves

The differential mode curve is linear for input voltage between -400mV and +400mV. So the present circuit is suitable for low voltage applications. Differential amplifier is in the balance condition that’s why output of differential amplifier is zero for zero differential input shown in the figure 3.1, 3.2 and 3.3 at 45nm, 32nm and 22nm respectively.
1.3 Output parameter

1.4. Internal parameters

The various internal parameters mentioned in TABLE 1.1 shows that with the decrease in channel length from 45nm to 22nm value of Vth, increase and the value of Cgs and Cgd decreased.

Currents: Id.
Voltages: Vgs, Vds, Vth, Vdsat.
Transconductance: gm.
Capacitances: Cgd, Cgs.
Current gain: Beta.
various subscripts indicates:
g for gate terminal
d for drain terminal
s for source terminal
th for threshold
sat for saturation

<table>
<thead>
<tr>
<th>Technology</th>
<th>At 45nm</th>
<th>At 32nm</th>
<th>At 22nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vin</td>
<td>0.1v</td>
<td>0.1v</td>
<td>0.1v</td>
</tr>
<tr>
<td>RL</td>
<td>100K</td>
<td>100K</td>
<td>100K</td>
</tr>
<tr>
<td>CL</td>
<td>100f</td>
<td>100f</td>
<td>100f</td>
</tr>
<tr>
<td>Vdd</td>
<td>1.1V</td>
<td>0.95V</td>
<td>0.9V</td>
</tr>
<tr>
<td>Vss</td>
<td>-1.1V</td>
<td>-0.95V</td>
<td>-0.9V</td>
</tr>
<tr>
<td>Iref</td>
<td>10u</td>
<td>10u</td>
<td>10u</td>
</tr>
</tbody>
</table>

TABLE 1.1
Where:-

- Red indicate output voltage
- Yellow indicate input voltage

Figure 3.4-3.6 shows the transient analysis for a sinusoidal input with peak-to-peak amplitude of 0.2V applied to the CMOS differential amplifier at a frequency of 1kHz. An output waveform is obtained at output port v(5): 0.8v, 0.57v and 0.35v at 45nm, 32nm and 22nm respectively.

3. Output parameter

The various output parameters mentioned in TABLE 1.2 are:

- Currents: \(I_d\)
- Voltages: \(V_{gs}, V_{ds}, V_{th}, V_{dsat}\)
- Transconductance: \(g_m\)
- Capacitances: \(C_{gd}, C_{gs}\)

3. AC ANALYSIS

3.1 Input parameter

<table>
<thead>
<tr>
<th>Technology</th>
<th>At 45nm</th>
<th>At 32nm</th>
<th>At 22nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{in})</td>
<td>0.1v</td>
<td>0.1v</td>
<td>0.1v</td>
</tr>
<tr>
<td>(R_L)</td>
<td>100K</td>
<td>100K</td>
<td>100K</td>
</tr>
<tr>
<td>(C_L)</td>
<td>100f</td>
<td>100f</td>
<td>100f</td>
</tr>
<tr>
<td>(V_{dd})</td>
<td>1.1V</td>
<td>0.95V</td>
<td>0.9V</td>
</tr>
<tr>
<td>(V_{ss})</td>
<td>-1.1V</td>
<td>-0.95V</td>
<td>-0.9V</td>
</tr>
<tr>
<td>(I_{ref})</td>
<td>10u</td>
<td>10u</td>
<td>10u</td>
</tr>
</tbody>
</table>

3.2 Differential gain, Phase & CMMR curve

For the frequency response plot, an AC signal of 0.1V is swept with 6 points per decade from a frequency of 10Hz to 1GHz. Fig.3.7-3.15 illustrates the frequency response which shows a AC gain in dB, phase in degree and CMMR versus frequency in Hz (in log scale).
Fig. 3.7 Differential gain at 45nm

Fig. 3.8 Differential phase at 45nm

Fig. 3.9 CMRR at 45nm

Fig. 3.10 Differential gain at 32nm

Fig. 3.11 Phase at 32 nm

Fig. 3.12 CMRR at 32 nm

Fig. 3.13 Differential gain at 22nm
3.3 Internal parameter
The various internal parameters mentioned in TABLE 1.3 are: 
- Currents: $I_d$, Voltages: $V_{gs}$, $V_{ds}$, $V_{th}$, $V_{dsat}$.
- Transconductance: $g_m$.
- Capacitances: $C_{gd}$, $C_{gs}$.
- Current gain: Beta.
- Various subscripts indicate: 
  g for gate terminal, 
  d for drain terminal 
  s for source terminal, 
  th for threshold 
  sat for saturation

3.4 Output parameter

<table>
<thead>
<tr>
<th>Technology</th>
<th>At 45nm</th>
<th>At 32nm</th>
<th>At 22nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (in db)</td>
<td>12.30</td>
<td>9.39</td>
<td>5.20</td>
</tr>
<tr>
<td>-3db frequency (Mhz)</td>
<td>59.43</td>
<td>59.29</td>
<td>55.08</td>
</tr>
<tr>
<td>Phase margin</td>
<td>103.71</td>
<td>109.68</td>
<td>123.23</td>
</tr>
<tr>
<td>CMRR</td>
<td>27.77</td>
<td>23.53</td>
<td>11.78</td>
</tr>
<tr>
<td>Unity gain BW (Mhz)</td>
<td>238.23</td>
<td>164.43</td>
<td>83.94</td>
</tr>
<tr>
<td>GBW (Mhz)</td>
<td>730.98</td>
<td>556.73</td>
<td>286.42</td>
</tr>
</tbody>
</table>

IV. RESULTS & DISCUSSIONS

The figure 4.1 depicts the variation of average power dissipation (in uW), gain (in db), and bandwidth (in MHz) with respect to the channel length at 22nm, 32nm, and at 45nm respectively of the CMOS based differential amplifier. The graph clearly shows that as the channel length decrease in the sequence, 45nm, 32nm, & 22nm the average power dissipation decrease and bandwidth is maintained near about 55MHz while the gain of the differential amplifier is decreased as channel length is decreased in the sequence 45nm, 32nm and 22nm respectively.
Low Voltage, High Bandwidth & Input Impedance CMOS Differential Amplifier at NANO Scale

Figure 4.1

V. ACKNOWLEDGEMENT

The authors would like to thank to the anonymous reviewers for their comments and suggestions, which have helped to improve this paper. We would also like to thank Electronics and Communication department, CET-IILM – AHL Gr. Noida, Gautam Buddh Nagar, Uttar Pradesh.

REFERENCES

[1] “Shamik Das, Member, IEEE, Alexander J. Gates, Hassan A. Abdu, Student Member, IEEE, Garrett S. Rose, Member, IEEE, Carl A. Picconatto, and James C. Ellenbogen, Member, IEEE “Designs for Ultra-Trap, Special-Purpose Nanoelectronics Circuits”
[2] Zhiwei Xu1, Qin Jane Gu2, Ining Ku3 and Mau-Chung Frank Chang3 HRL Laboratories, Malibu, California, USA, A Compact, Fully Differential D-band CMOS Amplifier in 65nm CMOS.
[3] Electronics device architecture for the nano CMOS era from ultimate CMOS scaling to beyond CMOS device by simon deleoniubus, 2009 - Pan Stanford publishing PTE. Ltd
[13] “Priyanka Kakoti” Design of a high frequency low voltage CMOS operational amplifier
[14] “Juan Pablo Martinez Brito , Sergio Bampi” A DC offset and CMRR analysis in a CMOS 0.35 mm operational transconductance amplifier using Pilgrims area/accuracy tradeoff
[16] “Rajinder Tiwari, R K Singh” AN OPTIMIZED HIGH SPEED DUAL MODE CMOS DIFFERENTIAL AMPLIFIER FOR ANALOG VLSI APPLICATIONS.
[18] Vladimir I. Podanov, Student Member, IEEE, and Michael M. Green, Member, IEEE A Differential Active Load and its Applications in CMOS Analog Circuit Designs.

Dileep Kumar is pursuing B.TECH in Electronics & Communication from CET-IILM-AHL Greater Noida Uttar Pradesh. He had done his summer training from B.H.E.I. IP Jagdishpur, Sultanpur U.P.

Divakar veer Vikram singh is pursuing B.TECH in Electronics & Communication from CET-IILM-AHL Greater Noida Uttar Pradesh. He had done his summer training from B.H.E.I. IP Jagdishpur, Sultanpur U.P.

Veerandra pratap is pursuing B.TECH in Electronics & Communication from CET-IILM-AHL Greater Noida Uttar Pradesh. He had done his summer training from CETPA Noida U.P.

Adil Zaidi has received his Bachelors Degree B.Tech in Electronics & Communication from CET-IILM-AHL, Greater Noida, and Master’s Degree M.Tech in VLSI Design from Maharishi Dayanand University, Haryana. His research interest includes Analog & Digital VLSI Design, Low Power Circuits, CNTFET, Nanoelectronics etc. Presently he is serving as Assistant Professor in the Department of Electronics and communication Engineering, CET-IILM-AHL, GreaterNoida Uttar Pradesh, India.

Firoz is pursuing B.TECH in Electronics & Communication from CET-IILM-AHL Greater Noida Uttar Pradesh. He had done his summer training from B.H.E.I. IP Jagdishpur, Sultanpur U.P.