Implementation of Area Efficient OFDM Transceiver on FPGA

Preeti.G.Biradar, Uma reddy.N.V

Abstract— orthogonal frequency division multiplexing (OFDM) is a modulation technology which is widely adopted in many new and emerging wired and wireless communication systems. OFDM offers superior advantages of high spectral efficiency, robustness against a inter carrier and inter symbol interference. In this paper we are designing a transceiver of an OFDM and it is implemented on FPGA. In order to reduce the circuit complexity and space, pipelined 128 point FFT /IFFT architecture is used and also aims to optimize in terms of area and speed at low frequency.

Index Terms— FFT/IFFT, OFDM, Pipeline, spectral efficiency

I. INTRODUCTION

Multicarrier modulation is a technique used for the data transmission which divides the high bit rate data streams into several parallel low bit data streams, and these low bit data streams are used to modulate many carriers. There are many useful properties of the multicarrier transmission such as spectral efficiency, delay spread tolerance. Orthogonal frequency division multiplexing [OFDM] is one of the multicarrier modulation technologies which are widely used in emerging wired and wireless communication system [1]. Recent trend says that orthogonal frequency division multiplexing gained lot of popularity among the broadband community. OFDM is implementing in many emerging communication protocols due to several advantages over the traditional multiplexing technique frequency division multiplexing [FDM]. OFDM transforms a frequency selective wideband channel into a group of non selective narrowband channels, by preserving orthogonality in the frequency domain, OFDM makes robust against the large delay spreads. The Fast Fourier Transform [FFT] and Inverse Fast Fourier Transform [IFFT] are the two important key points in the OFDM system. FFT is a fast way to calculate the Discrete Fourier Transform [DFT], which transforms data from time domain to frequency domain where as IFFT transforms data from frequency domain to time domain. The hardware implementation of FFT/IFFT approaches is a challenging issue where the digital signal processors (DSPs) and field programmable gate array (FPGA) chips are two considering designing environments for implementing different schemes of FFT approaches. Recently, the FPGA technology is used as due to fast progress in very large scale integration (VLSI) technology. The FPGA devices provide complete programmable system on chip environments by incorporating the programmability of programmable logic devices and the architecture of gate arrays.

They consist of thousands of logic gates and some configurable logic blocks which make them appropriate solution for prototyping the application specific integrated circuits(ASIC) with dedicated architectures for specified digital signal processing applications[2].

This paper presents the design and implementation of OFDM transceiver on FPGA. The proposed design is simulated using Xilinx and then it is implemented on FPGA. This system utilizes the optimal number of resources in terms of slices, LUTs and multipliers to provide high performance cost effective solutions for wireless communications. In order to reduce the circuit complexity and space a pipelined FFT /IFFT architecture is used and also aims for high through put, high data rate at low frequency. The baseband processing however is mostly carried out by simulations only. In recent years few attempted implementation on FPGA or ASICs. In this paper the code is developed using verilog and simulated using Xilinx and then it is implemented on FPGA.

II. RELATED WORK

According to the literature survey various design and implementations have been done for OFDM transceiver [3]. In paper [4] discussed about the 32 point FFT architecture using radix-2 algorithm, which uses direct mathematical design. In paper [2] discussed about four FFT approaches such as Cooley Tukey, Good Thomas, Radix-2 FFT and showed among them radix-2 method uses least number of slices. In paper [5] pipelined 64 point FFT/IFFT processor for OFDM applications has been described which has a working frequency up to 80MHz. In paper [6] a radix-2 serialized 512 point FFT algorithm is used to enhance the speed and this design simulated up to 227.355 MHz. Most of the hardware implementation has been done either on vertex based FPGA or on ASICs [3]. ASIC based designs suffer from more time to market factor, high cost and provide less flexibility. FPGA uses parallel processing to realize functions in an unlimited only limited by resources. In this work an OFDM Transceiver system is designed on a low cost FPGA Sparten3 or Virtex2 Pro to improve both speed and area at a time, by utilizing less number of resources in terms of slices, LUTs and multipliers of target FPGA to provide high performance cost effective solution for wireless communication applications [6].

III. PROPOSED DESIGN

Orthogonal frequency division multiplexing is the enhanced technology of the frequency division multiplexing in which the total available bandwidth is divided into N non-overlapping frequency sub-channels which are orthogonal to each other.

Manuscript Received July, 2013.

Ms. Preeti.G.Biradar, Electronics and Communication department, AMC engineering college, Bangalore, India.

Prof. Uma reddy.N.V, Electronics and Communication department, AMC engineering college, Bangalore, India.

Each sub-channel is modulated with a separate symbol stream. OFDM communication system performs several steps as shown in fig.1.

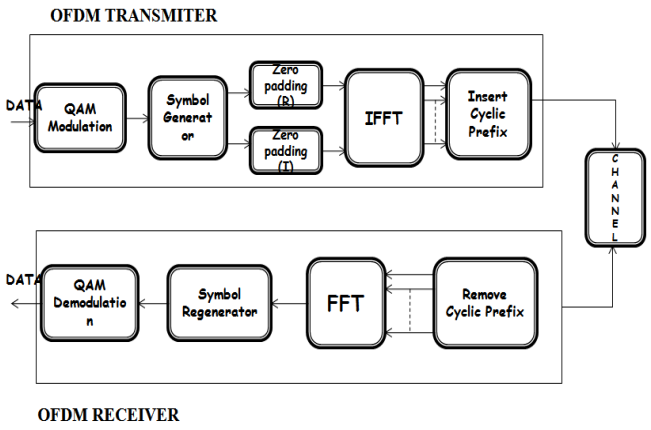

Fig: 1. Proposed Design

The fig 1 shows the proposed design. This system consists of OFDM transmitter and OFDM receiver. At the transmitter a serial data is sent as an input to the QAM modulation, where the data is converted to parallel by using serial in parallel out [SIPO]. Then the parallel data is sent to constellation mapping in order to recognize type of interference and distortion in the signal. By mapping, the symbol can be sent with two carriers on the same frequency. The modulated output from 16 bit QAM modulation is sent to symbol generator to generate symbols of 64bit. Then the 32 bit zeros are added at both LSB and MSB bits for both real and imaginary as shown in fig 1 in order to create a brick wall and to enable the signal to decay. Then these 128bits real and imaginary bits are sent to the Inverse Fast Fourier transform which transforms the data from frequency domain to time domain it is explained in detail in part IV. One of the main limitations of the wireless communication system is Inter Symbol Interference [ISI] which is caused due to multipath reflection in the channel. In order to prevent Inter Symbol Interference and to preserve orthogonal property between the sub carriers a cyclic prefix is inserted at the post prefix and prefix.

At the receiver end the output from the transmitter is given to the receiver through channel, where the cyclic prefix is removed and then sent to the Fast Fourier transform which converts back the data from time domain to frequency domain and then the symbols are regenerated by using symbol regenerator then de-mapping is done finally the OFDM signal is generated.

IV. FFT/IFFT

Fast Fourier transform is a discrete Fourier transform [DFT] algorithm which is an efficient way of implementation, which transforms a signal much faster than a DFT. FFT divides DFT successively in the smaller calculations to increase computation efficiency. The FFT reduces the number of computation needed for N points from N^2 to $N\log_2 N$. By using equation1 the DFT of the given discrete signal x (n) can be directly computed. FFT calculation can be done using decimation in time (DIT) algorithm or decimation in frequency (DIF) algorithm. In DIT, the twiddle factor is first multiplied and then it is summed, whereas in DIF first input is summed and then twiddle factor is multiplied. In DIT algorithm inputs are in bit reversed order and outputs are natural order and in DIF inputs are natural order and outputs are reversed order.

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{nk}, k = 0,1, \ldots . N-1 \quad (1)$$

Where,

$W_N^{nk} = e^{-j2kn/N}$

The DIT algorithm provides better signal to noise ration compared to DIF [7]. In our system we are using radix-2 DIT algorithm

A. Types of FFT/IFFT architectures

Generally the FFT/IFFT processors can be divided into three main categories-

1. Pipeline FFT/IFFTs. In order to achieve high performance concurrent or parallel processing of the various stages has been employed.
2. Column FFT/IFFTs. Each and every stage in the FFT/IFFT is computed with a set of processing elements and the output is given as feedback to the same processing elements for the computing the next stage.
3. Fully parallel FFT/IFFTs. The signal-flow graph operations are mapped to a hardware structure in an isomorphic manner. The hardware implementations are intensive with respect to current technology and not suitable for large FFT/IFFTs

B. Pipelined FFT Architectures

The low power high speed FFT processor will be essential in many advanced signal processing. In this paper pipelined FFT/IFFT architecture is used. The advantage of this architecture is its ability of decreasing the number of complex twiddle factor multiplications. By reducing the number of multiplications implies a reduced number of computations required to complete an overall FFT algorithm. Pipelined architecture is the best choice for high throughput applications. Due to its regular structure and relatively simple control, it is the best choice to implement high speed long size FFT/IFFT. To improve the performance of the sequential processor, parallism can be introduced by using separate arithmetic unit for each stage of the FFT/IFFT. This increases the throughput by a factor of $\log_2 N$ when the different units are pipelined [8].

C. Radix-2 DIT FFT algorithm

The objective of the radix-2 DIT FFT algorithm is to reduce the DFT computation to a series of radix 2 butterfly operations and twiddle factor multipliers. The basic computation performed in each stage is called butterfly. The fig.2 shows the single butterfly computation for DIT radix-2 FFT. Each butterfly is computed with the help of equation2. The Radix-2 FFT requires bit reversed data ordering i.e. the LSB bits becomes MSB and MSB bits becomes LSB bits as shown in fig.3, in order to increase the efficiency.

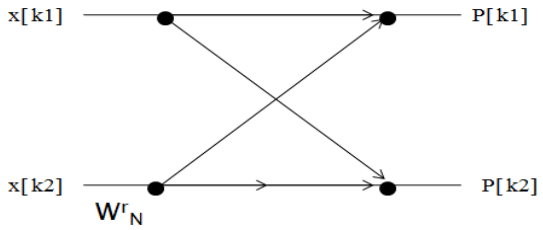

Fig.2. Butterfly computation for DIT radix-2 FFT

$$P(X1) = x(k1) + W_N^r\ x(k2)$$
$$P(X2) = x(k1) - W_N^r\ x(k2) \qquad (2)$$

Where,

$$x(k1) = x_{re}(k1) + j\,x_{im}(k1)$$
$$x(k2) = x_{re}(k2) + jx_{im}(k2)$$
$$W_N^r = e^{-j2\pi r/N} = \cos\left(\frac{2\pi r}{N}\right) - jsin\left(\frac{2\pi r}{N}\right)$$

The fig.3 shows the signal flow graph of an eight point DIT algorithm showing the different stages, groups and butterflies. The N point DIT FFT has $\log_2$ (N) stages, numbered p= 1, 2…….$\log_2$ (N). Each stage comprises N/2 butterflies. The P^{th} stage has N/2 twiddle factors numbered k=0, 1, 2… (N/2) - 1. For N=8 the complex multiplication required in direct computation is 64 where as using FFT is 12, hence about 5.3 factor speed is improved compared to direct computation.

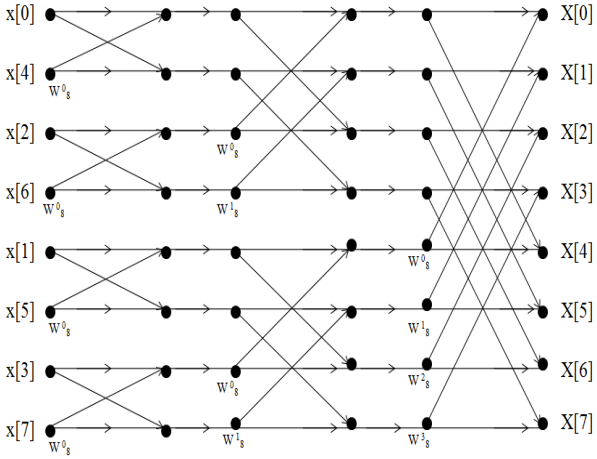

Fig.3. signal flow graph of 8 point DIT radix-2 FFT

V. SIMULATION AND IMPLEMENTATION RESULTS

The proposed design has been simulated using Xilinx and Modelsim, the wave form obtained after simulating is as shown in fig .4. The RTL schematic of the proposed system is as shown in fig. 5, then it simulated result is implemented on FPGA vertex 2 pro. The design summary of the system is as shown in table 1. The design summary shows that the proposed design utilizes 4423 (32%) number of slices, 2202 (8%) number of slice flip flops, 7849 (28%) number of 4 input LUTs, 7 (1%) number of bounded IOBs, 12 (8%) number of multipliers and 4 (25%)Global clocks out of available sources in the FPGA device. The comparison of the proposed design with previous work in terms of multipliers and bounded IOBs is as shown in table 2. The table 2 shows that the proposed design optimized in the area factor in terms of multipliers. The timing summary of the proposed design shows the speed factor of the device is -2, minimum period is 27.92ns.

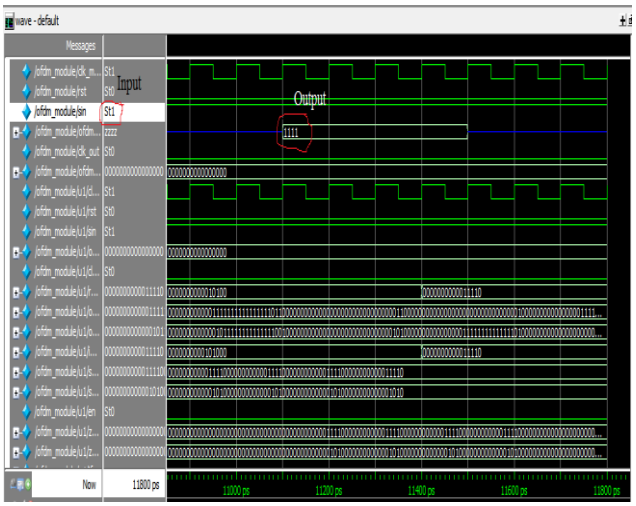

Fig.4. Simulated waveform of OFDM transceiver

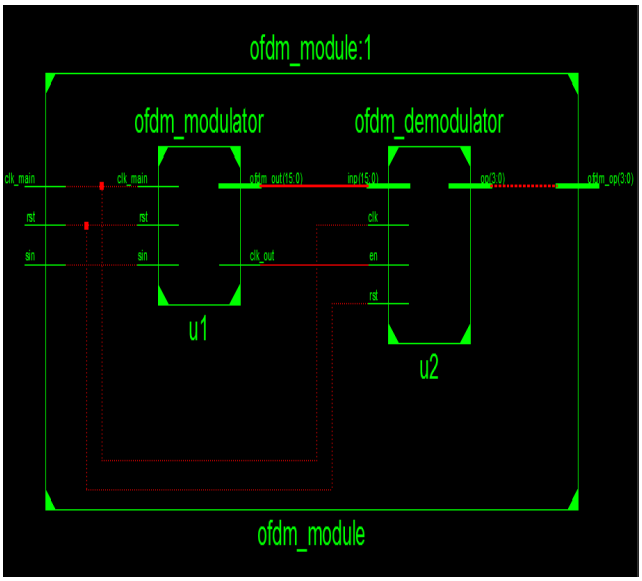

Fig.5. RTL schematic of proposed system

Table.1. Design Summary

Logic Utilization	Used	Available	Utilization
Number of Slices	4423	13696	32%
Number of Slice Flip Flops	2202	27392	8%
Number of 4 I/P LUTs	7849	27392	28%
Number of Bounded IOBs	7	556	1%
Number of MUL	12	136	8%
Number of GCLKs	4	16	25%

Table.2. Comparison

Logic utilization	Proposed Design	Previous Design
Number of Bounded IOBs	7	52
Number of MUL(Area Factor)	12	32

VI. CONCLUSION

A transceiver of an OFDM system is analyzed and implemented on FPGA using a low cost Vertex 2 pro target device. A concept of pipelined FFT/IFFT architecture is used in order to reduce circuit complexity and space. In this work area and speed are optimized also compared with previous work and showed that the proposed design optimized in the area factor in terms of multipliers. The minimum input arrival time required before clock is 2.485ns and the maximum output time required after clock is 4.715ns. Thus area and speed optimized at the low frequency.

ACKNOWLEDGMENT

The authors would like to thank for the support of Department Electronics and Communication Engineering AMCEC, Bangalore, Karnataka, India.

REFERENCES

1. Mounir Arioua et.al, " VHDL Implementation of an optimized 8-point FFT/IFFT processor on pipeline architecture for OFDM systems. IEEE , 978-1-61284-732-0/11,2010
2. Arman Chahardahcherik et.al. "Implementing FFT Algorithms on FPGA" IJCSNS International Journal of Computer Science and Network Security, VOL No.11, November 2011
3. Manjunath Lakkannavar et.al, "Design and Implementation of OFDM using VHDL and FPGA" IJEAT ISSN: 2249-8958, volume-1,Issue-6, August 2012.
4. Asmita Haveliya, " Design and Simulation of 32 point fft using radix-2 algorithm for FPGA Implementation", 2012, second International conference on AC and CT.
5. A. Anbarasan et.al, "Design and Implementation of low power FFT/IFFT processor for wireless communication" International conference on PI and ME". March , 2012
6. Shaminder Kaur et.al. "FPGA Implementation of OFDM Transceiver using FFT Algorithm" International Journal of Engineering Science and Technology (IJEST) ISSN : 0975-5462 Vol. 4 No.04 April 2012.
7. Tran-Thong et.al, Fixed Point Fast Fourier Transform Error Analysis", IEEE Transactions on AS and SP, 24(6): 563573, December 1976.
8. K. Umapathy et.al. "Low Power 128-Point Pipeline FFT Processor using Mixed Radix 4/2 for MIMO OFDM Systems" International Journal of Soft Computing and Engineering (IJSCE) ISSN: 2231-2307, Volume-2, Issue-5, November 2012

AUTHORS PROFILE

Ms. Preeti.G.Biradar, born on 9th Feb 1990 in Bijapur, Karnataka, India. She received Bachelor's degree in Electronics and Communication Engineering in the year 2011 from SIET, Bijapur under VTU University. Currently she is pursuing MTech in Digital Electronics and Communication from AMCEC, Bangalore under VTU University. Her research interests are wireless Communication, Networking, Embedded systems, Signal processing.

Prof. Uma reddy N.V, received her BE (Electronics) degree from Kuvempu University in 1995 and M.Tech (Electronics) degree from Viveswaraya technological University Belgaum, India in 2004, Presently pursuing PhD in VTU, Bangalore, India. she has more than fifteen years of experience in teaching her area of interest include CMOS VLSI, HDL, CCN, AMS, presently she is Working as HOD, Professor in the Department of ECE in AMC EC, Bangalore.