Implementation of OFDM Transmitter and Receiver using FPGA

Nasreen Mev, Brig. R.M. Khaire

Abstract: ***Orthogonal Frequency Division Multiplexing (OFDM) is the most promising modulation technique. It has been adopted by most wireless and wired communication standards. The idea is to utilize a number of carriers, spread regularly over a frequency band, in such a way so that the available bandwidth is utilized to maximal efficiency. The objective of this paper is to carry out an efficient implementation of the OFDM system (i.e. transmitter and receiver) using "Field Programmable Gate Array (FPGA)" and find the result by simulating all the blocks used in proposed project by using QuartusII & Modelsim simulation tool.***

Keywords- OFDM, FPGA.

I. INTRODUCTION

The OFDM is the modulation scheme having multi carrier transmission techniques here the available spectrum is divided into many carriers each one being modulated at a low rate data stream. The spacing between the carriers is closer and the carriers are orthogonal to one another preventing interferences between the closely spaced carriers hence OFDM can be thought of as a combination of modulation and multiplexing techniques, each carrier in a OFDM signal has very narrow bandwidth so the resulting symbol rate is low which means that the signal has high tolerance to multi path delay spread reducing the possibility of inter symbol interference (ISI)which is the requirement for today's communication systems.

OFDM is similar to FDM but much more spectrally efficient by spacing the sub-channels much closer together (until they are actually overlapping). This is done by finding frequencies that are orthogonal, which means that they are perpendicular in a mathematical sense, allowing the spectrum of each sub-channel to overlap another without interfering with it. In Figure 1.1 the effect of this is seen, as the required bandwidth is greatly reduced by removing guard bands (which are present in FDM) and allowing signals to overlap.

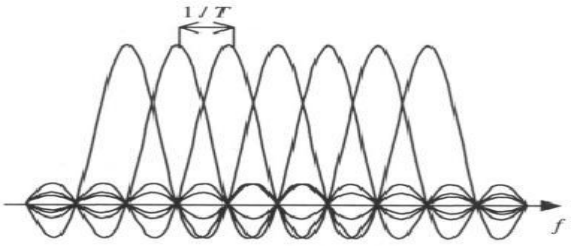

Figure 1.1 Spectrum overlap in OFDM

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A. Orthogonality

The key to OFDM is maintaining orthogonality of the carriers. If the integral of the product of two signals is zero over a time period, then these two signals are said to be orthogonal to each other. Two sinusoids with frequencies that are integer multiples of a common frequency can satisfy this criterion. Therefore, orthogonality is defined by:

$$\int_0^T \cos(2\pi n f_o t)\cos(2\pi m f_o t)\, dt = 0 \qquad (n \neq m)$$

where n and m are two unequal integers; f_o is the fundamental frequency; T is the period over which the integration is taken. For OFDM, T is one symbol period and f_o set to $\frac{1}{T}$ for optimal effectiveness.

B. Field Programmable Gate Array

By modern standards, a logic circuit with 20000 gates is common. In order to implement large circuits, it is convenient to use a type of chip that has a large logic capacity. A field programmable gate arrays (FPGA) is a programmable logic device that support implementation of relatively large logic circuits [6]. FPGA is different from other logic technologies like CPLD and SPLD because FPGA does not contain AND or OR planes.

Instead, FPGA consists of logic blocks for implementing required functions.

An FPGA contains 3 main types of resources: logic blocks, I/O blocks for connecting to the pins of the package and interconnection wires and switches. The logic blocks are arranged in a two-dimensional array, and the interconnection wires are organized as horizontal and vertical routing channels between rows and columns of logic blocks [7].

The routing channels contain wires and programmable switches that allow the logic blocks to be interconnected in many ways. FPGA can be used to implement logic circuits of more than a few hundred thousand equivalent gates in size [7]. Equivalent gates is a way to quantify a circuit's size by assuming that the circuit is to be built using only simple logic gate and then estimating how many of these gates are needed. Figure 1.2 a clear picture of the FPGA design flow.

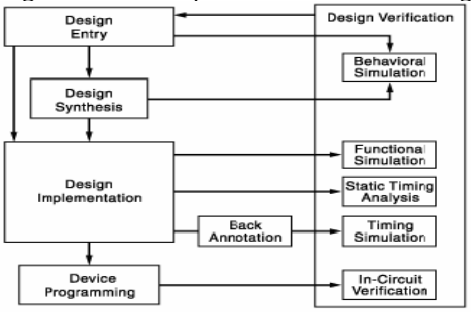

Figure 1.2FPGA design flow

II. OFDM TRANSMITTER & RECEIVER

Block Diagram

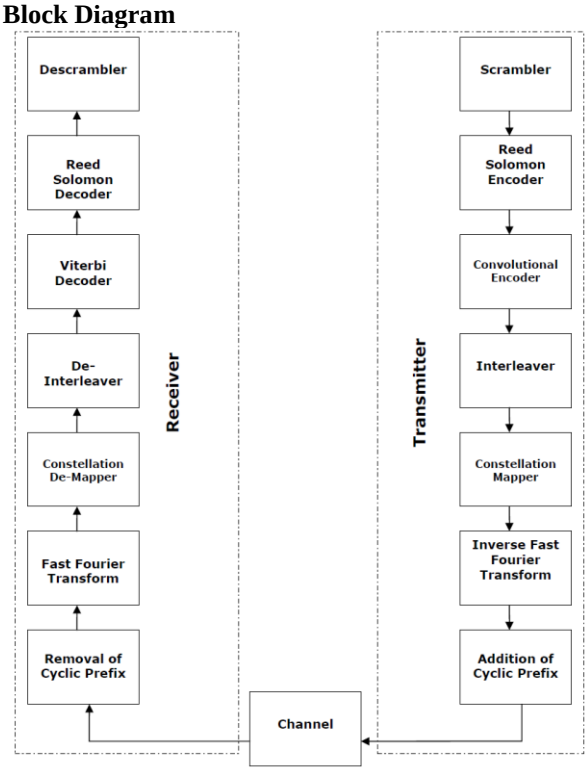

Fig1.3 Complete OFDM System

A. Scramble/Descramble

Data bits are given to the transmitter as inputs. These bits pass through a scrambler that randomizes the bit sequence. This is done in order to make the input sequence more disperse so that the dependence of input signal's power spectrum on the actual transmitted data can be eliminated.

At the receiver end descrambling is the last step. Descrambler simply recovers original data bits from the scrambled bits.

B. Reed-Solomon Encoder/Decoder

The scrambled bits are then fed to the Reed Solomon Encoder which is a part of Forward Error Correction (FEC). Reed Solomon coding is an error-correction coding technique. Input data is over-sampled and parity symbols are calculated which are then appended with original data [3]. In this way redundant bits are added to the actual message which provides immunity against severe channel conditions. A Reed Solomon code is represented in the form RS (n, k), where

$$n = 2^m - 1 \qquad (1)$$

$$k = 2^m - 1 - 2t \qquad (2)$$

Here m is the number of bits per symbol, k is the number of input data symbols (to be encoded), n is the total number of symbols (data + parity) in the RS codeword and t is the maximum number of data symbols that can be corrected. At the receiver Reed Solomon coded symbols are decoded by removing parity symbols.

C. Convolutional Encoder/Decoder

Reed Solomon error-coded bits are further coded by Convolutional encoder. This coder adds redundant bits as well. In this type of coding technique each m bit symbol is transformed into an n bit symbol; m/n is known as the code rate. This transformation of m bit symbol into n bit symbol depends upon the last k data symbols, therefore k is known as the constraint length of the Convolutional code.

Viterbi algorithm is used to decode convolutionaly encoded bits at the receiver side.

Viterbi decoding algorithm is most suitable for Convolutional codes with $k \leq 10$.

D. Interleaver/De-Interleaver

Interleaving is done to protect the data from burst errors during transmission. Conceptually, the in-coming bit stream is re-arranged so that adjacent bits are no more adjacent to each other. The data is broken into blocks and the bits within a block are rearranged. Talking in terms of OFDM, the bits within an OFDM symbol are rearranged in such a fashion so that adjacent bits are placed on non-adjacent sub-carriers.

As far as De-Interleaving is concerned, it again rearranges the bits into original form during reception.

E. Constellation Mapper/De-Mapper

The Constellation Mapper basically maps the incoming (interleaved) bits onto different sub-carriers. Different modulation techniques can be employed (such as QPSK, BPSK, QAM etc.) for different sub-carriers. The De-Mapper simply extracts bits from the modulated symbols at the receiver.

F. Inverse Fast Fourier Transform/ Fast Fourier Transform

This is the most important block in the OFDM communication system. It is IFFT that basically gives OFDM its orthogonality. The IFFT transform a spectrum (amplitude and phase of each component) into a time domain signal. It converts a number of complex data points into the same number of points in time domain. Similarly, FFT at the receiver side performs the reverse task i.e. conversion from time domain back to frequency domain.

G. Addition/Removal of Cyclic Prefix

In order to preserve the sub-carrier orthogonality and the independence of subsequent OFDM symbols, a cyclic guard interval is introduced. The guard period is specified in terms of the fraction of the number of samples that make up an OFDM symbol. The cyclic prefix contains a copy of the end of the forthcoming symbol. Addition of cyclic prefix results in circular convolution between the transmitted signal and the channel impulse response. Frequency domain equivalent of circular convolution is simply the multiplication of transmitted signal's frequency response and channel frequency response, therefore received signal is only a scaled version of transmitted signal (in frequency domain), hence distortions due to severe channel conditions are eliminated**.** Removal of cyclic prefix is then done at the receiver end and the cyclic prefix–free signal is passed through the various blocks of the receiver.

III.SPECIFICATION OF TRANSMITTER & RECEIVER

Figure 1.3 shows a top-level block diagram of the OFDM transmitter and receiver. Single-Clock operation speaks itself for the synchronous operation of the system.

The Reset input must be asserted for at least one clock cycle for the system to reset. Output of the transmitter is fed to the host PC via the serial port and also to the OFDM receiver. Specifications are listed below:

- OFDM with 64 sub-carriers (all data sub-carriers)
- All the sub-carriers are modulated using QPSK
- IFFT: 64-point. Implemented using FFT radix 22 algorithm
- Channel coding: Reed Solomon code + Convolution code
- Reed Solomon Encoder: RS (15, 9)
- Convolution Encoder: m=1, n=2, k=7. Code rate = ½
- Block Interleaver and 1/8 Cyclic Prefix

IV. RESULTS

A. Srambler

To verify proper functioning of the Scrambler was initially fed with a seed value of 1110101 and the following input bit stream was given to the Scrambler:

in: 0110101000

The output was: out: 1101110001

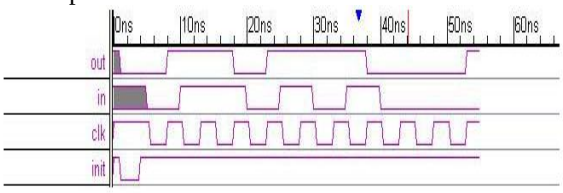

Figure 1.4 Scrambler simulation results

After a dry run of the scrambler using high-level modelling in Verilog it was verified that the output was correct.

B. Read Solomon Encoder

In order to check the proper functioning of Reed Solomon Encoder a test bench waswritten in Verilog. The input given to the encoder through the test bench was a string of alternating 36 (9 symbols) bits starting with 0. Such that:

in: 555555555H

It is well known in the art that if all the input symbols to a Reed Solomon encoder areidentical, then the parity symbols will all be identical as well and will be equal to the input symbols. Therefore, the output turned out to be

out: 555555555555555H

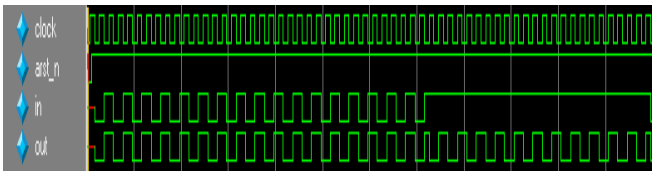

Figure 1.5 Reed Solomon Encoder simulation results

C. Convolutional Encoder

After simulation of the above shown Verilog code the following waveform wasgenerated. It can be seen that first of all a low pulse was given to the arst_n (reset) inputin order to initialize the shift register with all zeroes. Next the following bit stream wasgiven at the input,

in: 1011101

The output turned out to be,

out: 11010001011100

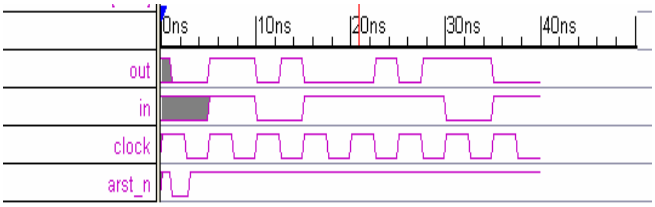

Figure 1.6 Simulation Waveform of the Convolutional Encoder

For a 7 bit input a 14 bit output is generated. Once again this circuit was taken through a dry run using high level modeling in Verilog and the results were verified.

D. Interleaver

The waveform for the interleaver goes upto 128 clock cycles. Therefore, it is not shown here. For an input block of data containing alternate 1s and 0s the output was

out:

000000001111111100000000111111110000000…….

so on

This clearly shows how bit positions have been changed.

E. Constellation Mapper

Following wave form shows that when an input of 10 was given to the Constellation Mapper the output was,

out: 00b504ff4afch

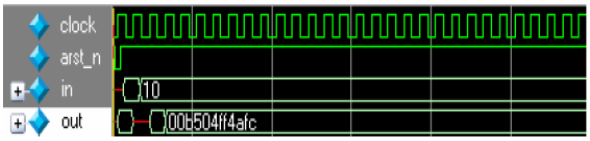

Figure 1.7 Constellation Mapper simulation results

F. IFFT

The IFFT was tested by giving the following 64 complex data points,

h00b504000000,h030000000000, h00b504000000,…, h00b504000000

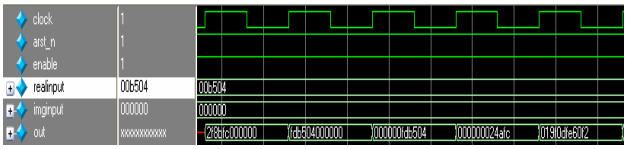

Figure 1.8 IFFT simulation results

The outputs were,

h2f8bc000000, h5db504000000, h0000005db504 and so on.

G. Cyclic Prefix Adder

The inputs given to the cyclic prefix adder were

47'h000000100101,47'h000010100001,
47'h001110100101,47'h110010100101,
47'h000010100101,47'h010101000101, 47'h011110100101,
47'h000011100101. . .
47'h000011100101

The outputs turned out to be

47'h000011100101,47'h000011100101, 47'h000011100101,
47'h000011100101,
47'h000011100101,47'h000011100101, 47'h000011100101,
47'h000011100101,
47'h000000100101,47'h000010100001, 47'h001110100101,
47'h110010100101,
47'h000010100101,47'h010101000101,
47'h011110100101,47'h000011100101…….. .
.47'h000011100101

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Note that the first eight outputs are actually the last eight inputs and the rest of the output points are same as the inputs

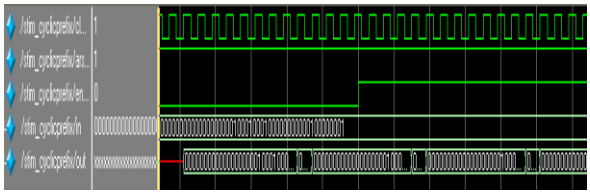

Figure 1.9 Cyclic Prefix Adder simulation result

H. Constellation Demapper

The constellation demapper basically maps the incoming QPSK constellation points to actual data.

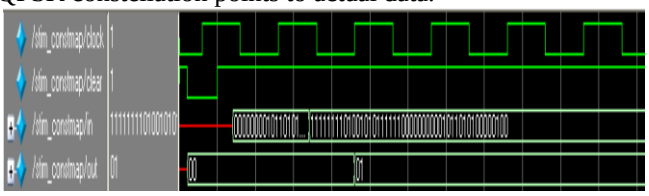

Figure 1.10 Constellation De-Mapper simulation results

I. De-Interleaver

Just like the interleaver the simulation waveform of de-interleaver extends to 128 cycles so can't be shown here.

J. Descrambler

The inverse of scrambling is done by the De-Scrambler. For the input,

b111111111000000000

the output was,

b110111111111000010

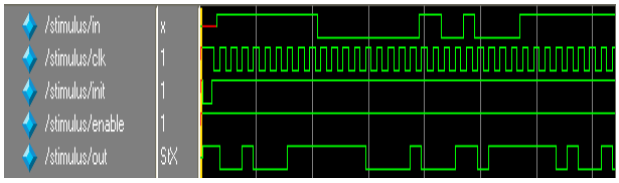

Figure 1.11 De-Scrambler simulation results

V. CONCLUSION

Orthogonal Frequency Division Multiplexing (OFDM) transmitter and receiver have been design using Quartus II tool and Simulation have been carried out using Altera Modelsim simulation tool. By using channel coding & decoding methods and error detection & correction methods synthesis and analysis has been done and how exactly OFDM system works, is verified. Verilog is used as Hardware Description Language (HDL) to program all the components of the OFDM Transmitter and Receiver and verification of functionality of all components has done by giving different input and output is verifieid. It is also found out that how many number of logic elements and memory bits are required to design each component.

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