# Design and Implementation of Dual-mode Programmable Decimation Filter for WCDM and GSM Systems

**Majid S. Naghmash, Faeza A. Abid**

***Abstract— In this paper, the dual mode receiver for wide and narrow band wireless system is investigated. In the current wireless system like GSM and WCDMA, the receiver base station should extract the individual radio channels from digitized wideband signal at extremely high sampling rate. However, the base station receiver must be capable at the same time isolate multiple channels from different bandwidths equivalent to channel bandwidths of different communication principles. The key requirements of current wireless systems is the reconfigurability and low complexity. The reconfigure digital filter design based on decimation is proposed to support current systems and accelerate the transition to new wireless generation using SIMULINK block set environment in MATLAB program. To extract the pass band widths for different standards, an cascaded digital filter need to be used in this case. The experiments and simulation results shows an important improvement in the complexity reduction and power consumption over the conventional approach.***

***Keywords SIMULIN, K MATLAB***

## I. INTRODUCTION

Now days, the basic approach of wireless and mobile systems receivers is to replace most of the analogue signal processing with digital signal processing to provide the advantage of flexibility through reconfiguration and enable different air-interface implementation over single generic hardware platform[1-3]. In wideband and narrowband receivers, several specifications of power consumption and high speed should be realize to achieve the user demands [4-5]. The most important requirements of modern wireless mobile systems is the reconfigurability in the receiver as well as the computationally concentrated part in the channel because it operate at maximum sampling rate in the digital front-end [6-7]. The receiver should extract numerous narrowband channels from a wideband signal.

Therefore, low complexity and high speed reconfigure channel are required in this case. To provide all this environments, a bank of digital filters known as channel filter have to employed. Many researchers are investigate in this field which propose efficient implementation of multi-stage digital filter bank [8-9].

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An independent channel filter approach is proposed by [10] which complexity is directly proportional with number of received channels. Consequently, this approach is efficient if the number of channels is small. Capable implementation of channelized filter by using discrete Fourier transform filter bank is projected in [11-12]. Based on combination of polyphase filter design modules, a hybrid filter bank has been targeted by [13] with less computation corresponding to conventional design associated by some limitations. Efficient sample rate converter with two stages filter bank and multi-mode channelizer has been proposed by [14]. The front-end digital filter bank has fixed number of channel and overlapped in pass band with each other resulting in simple isolation of channels.

In this paper, a novel reconfigurable half band and low pass FIR filters design based on decimation is investigated to provide the objectives of modern wireless and mobile principle according to user demand. MATLAB, System Generator and FDATool environments from Mathworks and Xilinx [15-20] is employed to design the proposed filter. The dual- mode channel receiver shown in Figure 1 is investigated properly.

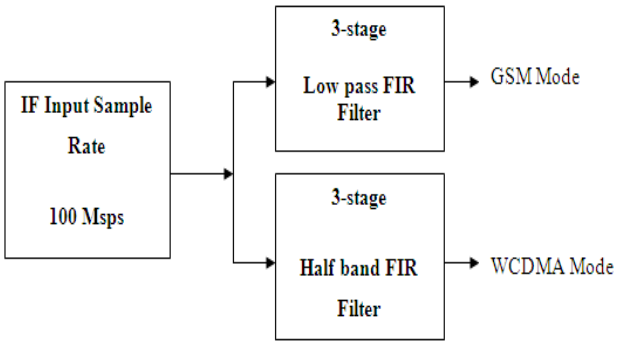


**Figure 1: Dual-mode channelizer Filter**

The reconfigurability of channelizer have to talented the same filter hardware for new communication standard with less reconfiguration overhead instead of employing separate filter for each standard. In the conventional filter, the reconfigurability is achieved by switching between two filters which is not an proficient advance. The reconfigurability in the filter have to achieved by reconfiguring the same prototype filter to process the signal of new communication standard with less possible overhead. Though, the Multiply-Accumulate (MAC) decomposition need to investigated.


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## II. SYSTEMS REQUIREMENTS

The Decimation part must be designed to satisfy the WCDMA and GSM specification and mask frequency which defines the reception requirements for the base station radio. Table 1 shows the summary of requirements for the receiver path. The modules of decimation filter have to design in complete WCDMA and GSM requirements which are obtained from 3rd Generation Partnership Project specification. The input to the decimation filter is a real signal sampled at 69,333 Msps and 61.44 MSPS with quantized factor of 14 bits. The complex baseband outputs are produced at a sampling rate of 2*F chip = 7.68 MSPS where Frequency chip is 3.84 MSPS. Consequently, the factor of 61.44/7.68 = 8, which can be realized in a few ways, is needed.

**Table 1. Specifications for the receiver Path**

| Parameters | WCDMA | GSM |
|---|---|---|
| Decimator Input Sample Rate | 61.44 MHz | 69.333248 MHz |
| Decimator Output Sample Rate | 7.8 MHz | 270 kHz |
| Input Signal Quantization | 14-bit | 16-bit |
| Output Signal Quantization | 14-bit | 16-bit |

Usually speaking, it is better to perform the decimation in a cascade of smaller rate stages than in one single stage with a large rate change. There are reasons from viewpoints of both system design and hardware implementation. In system design, a smaller rate alteration results in wider transition band, which leads to much fewer taps in the filter design. From a hardware implementation perspective, multiple stages usage makes later decimation stages operate at a lower sample rate. Therefore, the composite decimator uses less hardware than a single stage, and the computational efficiency is increased significantly. Furthermore, the successive filtering stages have successively wider transition bands. Based on the considerations above, we have designed three halfband and low pass FIR filters with down sampled by 2 filter to implement the decimation process. The block diagram of GSM and WCDMA decimation filters is shown in Figure 2.

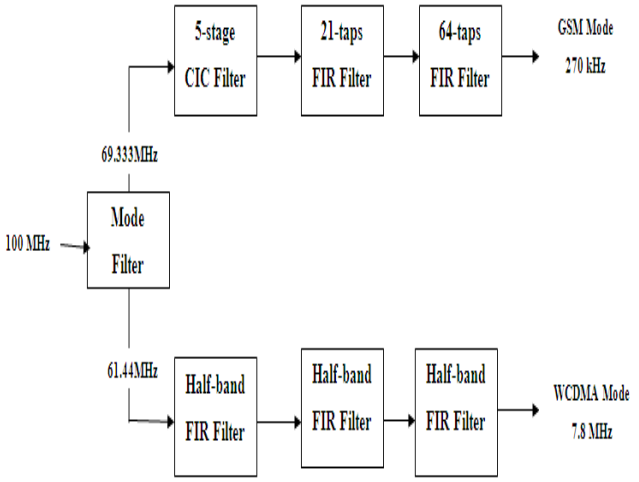


**Figure 1. GSM and WCDMA decimation filter Block Diagram**

### A. WCDMA Decimation Filters

After the frequency translation, a cascade of three half-band decimation filters is used to decrease the sampling rate From 61.44 Msps to 7.68 Msps. Half-band filters are a type of FIR filters whose passband and stopband ripples are the same, and the passband-edge and stopband-edge frequencies are equidistant from the halfband frequency pi/2. It is usually the structure of choice for filter implementation with a rate of two because every odd indexed coefficient in the time domain is zero except the center tap and even indexed coefficients are symmetric. This characteristic decreases computational workloads significantly. In our design, the three half band decimation filters are designed using Equiripple methods with a factor of 2 both on the basis of system tradeoff consideration. The detailed parameters of the three half-band filters are summarized in Table 2

**Table 2. Specifications Summary of Half-band Filters**

| Filter Stage | First | Second | Third |
|---|---|---|---|
| Passband Fpass (MHz) | 2.34 | 2.34 | 2.34 |
| Sample Rate F (MHz) | 61.44 | 30.72 | 7.68 |
| Filter Order | 10 | 18 | 94 |
| Peak – to – Peak Ripple (dB) | 0.0001 | 0.0001 | 0.0001 |
| Stopband Attenuation (dB) | 100 | 100 | 100 |
| Coefficient Quantization | 16 bits | 16 bits | 16 bits |
| Design Method | Equiripple | Equiripple | Equiripple |

The first stage Halfband Equiripple filter shows a stable impulse response and stable group delay within 11-taps filter length and bandwidth as illustrated in Figure 2 and Figure 3 respectively. The phase response is linear within the bandwidth of interest and the group delay is constant within the bandwidth as shown in Figure 4. Linear phase refers to the condition where the phase response of the filter is linear (straight line) function of the frequencies [10]. This results in the delay though the filter being the same at all frequencies. Therefore, the filter does not cause phase distortion or delay distortion. The second and third stage of the proposed decimation filter state that the filters response is stable and the phase and group delay is constant along with bandwidth. The stability of three filters gives a great indication for proposed filter performance and efficiency in the band of interest.

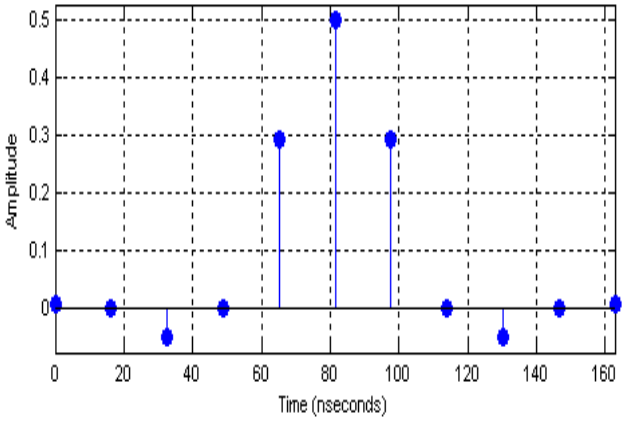


**Figure 2: Impulse response of first stage halfband filter**

The magnitude response of last stage halfband Equiripple filters shows that the filter provides the WCDMA specification requirements as shown in Figure 5. If one have a look to the filter response in the band of interest 2.34MHz that

represent the WCDMA IF specifications, the filter give flat response with no distortion in this band. Therefore, the filter provides the WCDMA requirements as these paper objectives. Finally, the filter provides constant phase and group delay along with band of interest as illustrated in Figure 6 and Figure 7 respectively.

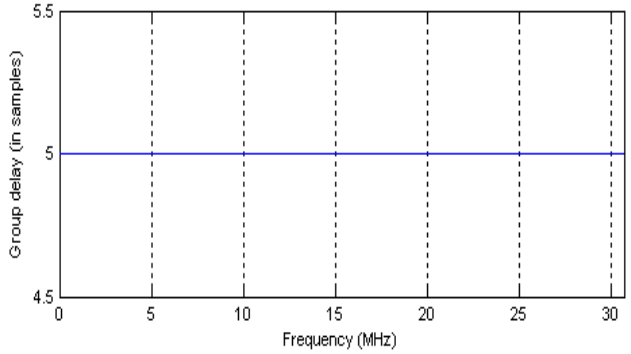


**Figure 3: Group delay of Filrst stage halfband filter**

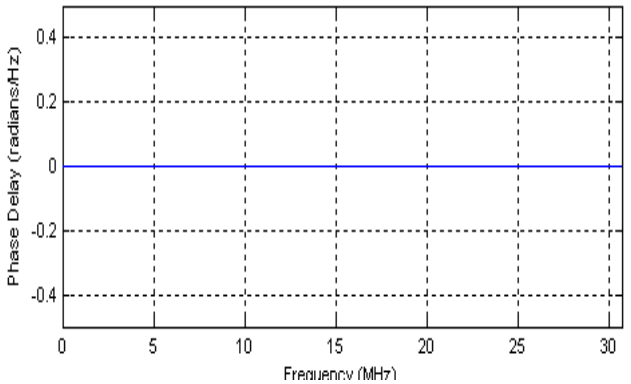


**Figure 4: Phase delay of first stage halfband filter**

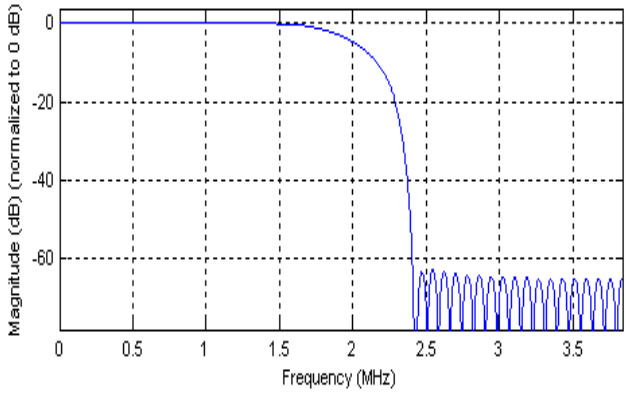


**Figure 5: Magnitude response of last stage in filter chain**

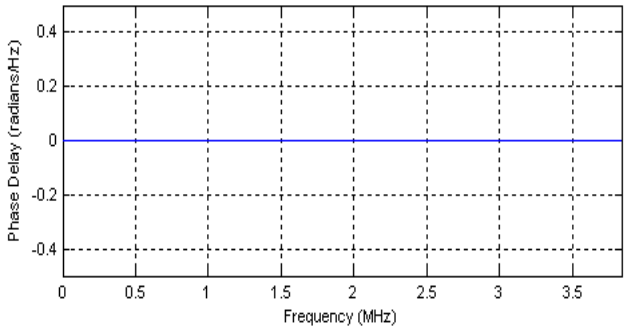


**Figure 6: Phase delay of last stage Equiripple filter**

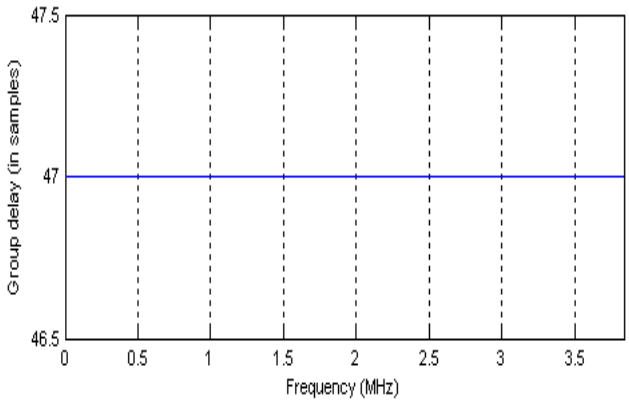


**Figure 7: Group delay of last stage Equiripple filter**

### *B. GSM Decimation Filter*

The projected decimation filter model is designed and simulated in the SIMULINK block to verify the filter performance in the SDR transceivers. The decimation filter structures in the SIMULINK block set are shown in Figure 8. The GSM signal is generated by chirp block and filtered down from 69.333248 MHz to 270.833 KHz through the three stages of the decimation filter to recover the GSM signal**.** The FFT power spectrum shows an exact GSM waveform as clear in Figure 9.

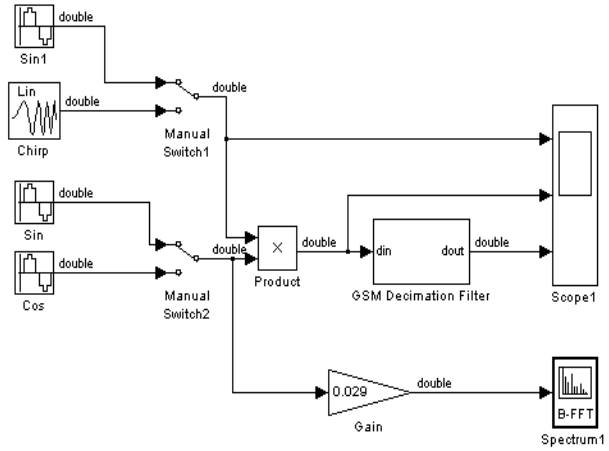


**Figure 8: GSM Decimation Filter design**

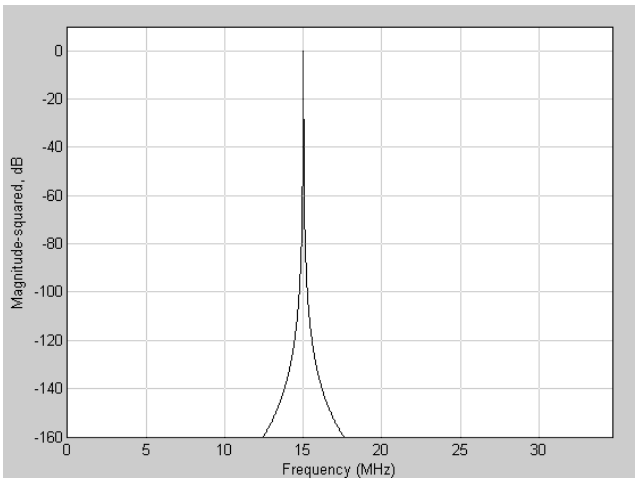


**Figure 9: GSM Power spectrum**


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The three stages of the decimation filter in floating point design contain CIC, CFIR, and PFIR, which are combined in the System Generator, as shown in Figure 10. The proposed filter response is illustrated in Fig.11.

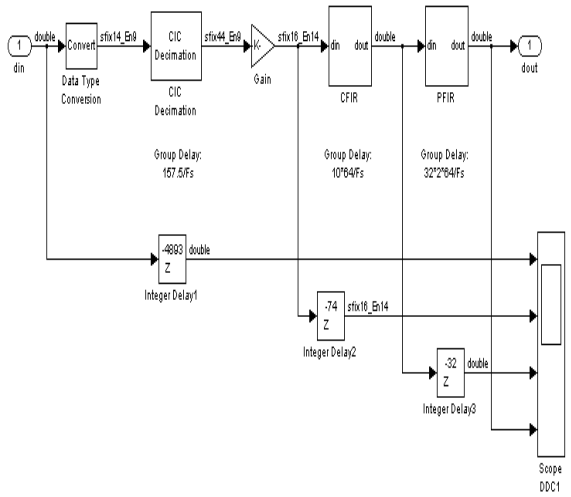


**Figure 10: GSM Decimation filter chain**

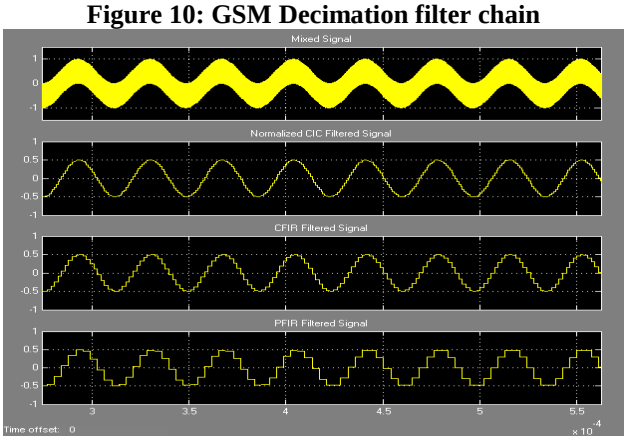


**Figure 11: GSM Decimation Filter response**

## III. DECIMATION MODULES SIMULATION

Having designed the three Equiripple decimation filters in MATLAB FDATool [11], [12], [13] then the cascaded of three decimation filter is running in a WCDMA transceiver model as shown in Figure 12.

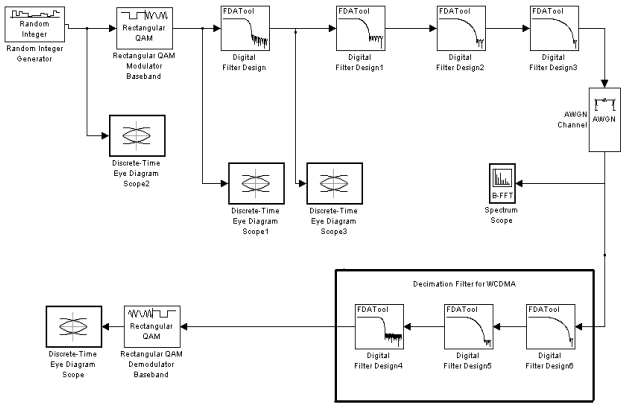


**Figure 12: WCDMA transceiver design with three halfband decimation filter modules**

The random integer generator generates the data with sample time of $3.84 \times 10^{-6}$ frame based output which represent the WCDMA original signals. The rectangular QAM modulates the input signal with in-phase and quadrature channels as shown in Figure 13. The modulated signal is up sampled to IF level by mean of DUC interpolator The original spectrum of the baseband signal is processed under the 20dB AWGN channels as shown in Figure 14. The power of the baseband magnitude signal is 3 dB as illustrated in Figure 15.

In the receiver path, the output signal from AWGN channel is pass through the proposed decimation filter to down sample and filtering in same time. The decimation filter consist of three halfband Equiripple filters is used to down convert the incoming signal from IF band to baseband in order to demodulated and recovered the origin signal. Due to efficient design of the decimation filter, the received signal is free from the channel noise and inters symbol interference (ISI). However, no distortion is found in the output of proposed decimator. .

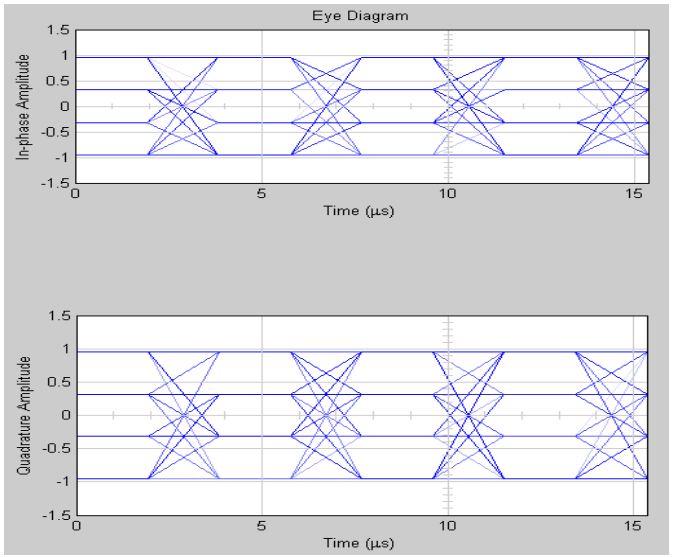


**Figure 14. Eye diagram of In-phase and qudrature channels**

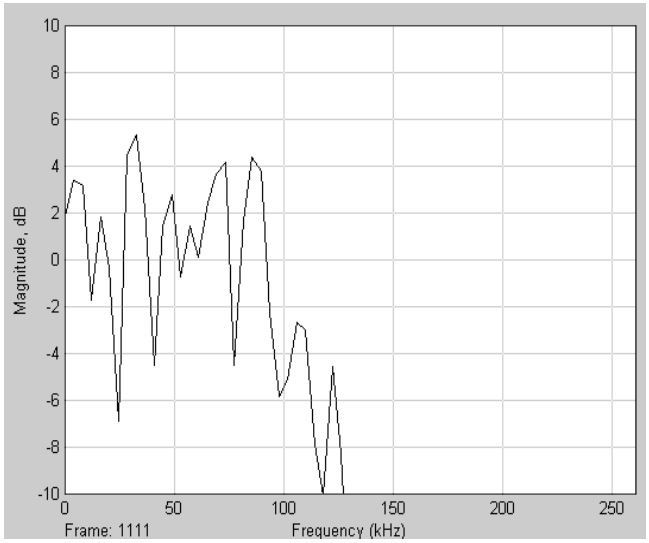


**Figure 15: WCDMA Original Baseband Signal**

## IV. HARDWARE IMPLEMENTATION

The Multiply-Accumulate (MAC) decomposition based FIR utilizing has been used to introduce the computational efficient implementation of proposed filter as shown in Figure 16.

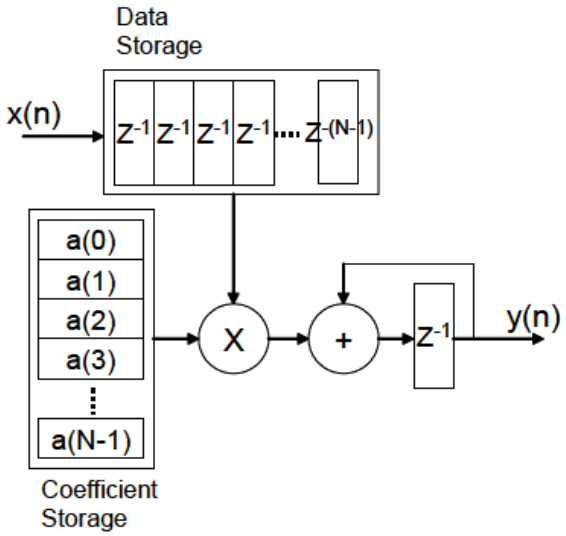


**Figure 16: Multiply-Accumulate (MAC) decomposition Design**

In the above design, the signal is decimated before filtering which reduce the filter coefficients number necessary to implements the preferred filter which resulting in speed improvement and power consumption. The whole decimator design is synthesized to create the Verilog netlist using the output options under System Generator token GUI interface and the results of the performance of map, place and route task done, by using the project navigator tool to implement the design in real time. The ISE project file is produced in the netlist directory specified in the System Generator token GUI along with the design and its association with timing constraints.The HDL code has been developed and synthesis on Xilinx Vertix-4 using Integrated software environments (ISE). The maximum frequency of the proposed filter is 100MHz. The project status of ISE software generates the decimation utilizing summary as shown in Table 3. The table lists the total number of slices and look-up tables (LUTs) used in this design. In each slice they are two LUTs and two FFs, during the PAR, the ISE software put all necessary LUTs close to each other for minimum propagation of data, for that some LUT inside slice not used and in some slice only FFs is used without LUT so, the number of LUTs cannot be calculated manually, therefore the LUTs could be less or more than Slices depend on software optimization. The device utilization summary generated by ISE software represents the available logic elements in FPGA and logic elements used by the in hand project been designed. The percentage of used logic elements to the available logic elements is calculated as follow:

$$\text{Utilization \%} = \frac{\text{used logic elements}}{\text{available logic elements}} X\ 100$$ , for examples:

Utilized number of Slice Flip Flop = (850/30720) x 100 = 3%

Utilized number 4-input LUTs = (430/30720) x 100 = 1%

Utilized number of occupied Slices = (600/15360) x 100 = 4%

Utilized number of bonded IOBs = (30/448) x 100 = 6%

**Table 3: decimation project device utilization summary**

| Device Utilization Summary | | | | |
|---|---|---|---|---|
| **Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** |
| Number of Slice Flip Flops | 850 | 30,720 | 3% | |
| Number of 4 input LUTs | 430 | 30,720 | 1% | |
| **Logic Distribution** | | | | |
| Number of occupied Slices | 600 | 15,360 | 4% | |
| Number of Slices containing only related logic | 600 | 661 | 100% | |
| Number of Slices containing unrelated logic | 0 | 661 | 0% | |
| **Total Number of 4 input LUTs** | 755 | 30,720 | 2% | |
| Number used as logic | 430 | | | |
| Number used as a route-thru | 8 | | | |
| Number used as Shift registers | 218 | | | |
| Number of bonded IOBs | 30 | 448 | 6% | |
| Number of BUFG/BUFGCTRLs | 2 | 32 | 3% | |
| Number used as BUFGs | 2 | | | |
| Number used as BUFGCTRLs | 0 | | | |
| Number of FIFO16/RAMB16s | 2 | 192 | 1% | |
| Number used as FIFO16s | 0 | | | |
| Number used as RAMB16s | 2 | | | |
| Number of DSP48s | 2 | 192 | 1% | |
| **Total equivalent gate count for design** | 158,984 | | | |
| Additional JTAG gate count for IOBs | 1,488 | | | |

## V. CONCLUSIONS

An optimized hardware efficient techniques has been used to implement the decimation filter for GSM and WCDMA systems based SDR technology is presented in this paper. The multi-stage Equiriple FIR digital filter algorithms and multistage half band FIR filter decomposition is proposed for less filter length and better computational complexity to enhanced the filter rate. The Multiply-Accumulate (MAC) decomposition based FIR architecture is used in hardware implementation to optimize the speed and area together which resulting in power consumption reduction. The FPGA vertix-4 and DSP48E blocks from Xilinx are used which contains multiplierless MAC filter. The proposed decimation filter could be used at maximum frequency of 100MHz with minimum power and FPGA area efficient. Therefore, the implementation of decimation filter on specific target FPGA results in cost effective solution for SDR technology which is promising to support the current and future generation of wireless and mobile systems.

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