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Reducing the Voltage Sag and Swell Problem in Distribution System using Dynamic Voltage Restorer with PI Controller

Raunak Jangid, Kapil Parkh, Pradeep Anjana

Abstract— ***One of the major problems observed in distribution system in recent days is Power Quality. Today most of the people are using the sophisticated electrical equipment based on semiconductor device, these equipment pollute the power quality. The sag and swell problem not only occur by the disturbed power quality but also due to high system tapping at the point of common coupling in the system. The non linear load is also creating the same problem at the load end. The Dynamic Voltage Restorer is recognized as the best solution for mitigation of voltage sag and swell associated problems in the highly taped distribution system.***

This work presents the simulation modeling and analysis of advanced DVR system for solving these problems. The PI control scheme is used for generating the gate pulse for IGBT bridge converter. The reference DC voltages are taken from the battery. The three phase fault is creating in the system and for analyzing the result. The role of DVR is to compensate the load current and voltage is investigated during the fault condition. Over all the DVR is improving the voltage quality as well as the reactive power demand during the uncharacteristic condition

Index Terms— ***Voltage sag, swell, DVR, PI controller, LC filter***

I. INTRODUCTION

It had been observed that in modern industrial devices most of devices are based on electronic devices such as programmable logic controllers and electronic drives. The power electronic devices are very sensitive to disturbances and become less tolerant to power quality problems such as voltage sags, swells and harmonics in the entire problems associated with voltage dips is considered as one of the most severe disturbances to the industrial equipment.

The problem of poor power quality like voltage sag for sensitive loads can be better dealt or solved by power electronics based Dynamic Voltage Restorer. With the application of DVR, the power system can be operated without voltage sag and the power supply by flexibly changing the distribution configuration after the occurrence of a fault.

Basic functions of customer power applications are fast switching and current or voltage injection for correcting anomalies in supply voltage or load current.

The DVR is a series conditioner based on a pulse width modulated (PWM) voltage source inverter (VSI), which could generate or absorb real or reactive power independently. The condition of Voltage sags caused by unsymmetrical line to line, single line to ground (SLG), double line to ground fault and symmetrical three phase faults is, influenced in case of sensitive loads. The DVR injects the individual voltages to restore and maintained sensitive loads to its nominal value. The combination of the custom power devices DVR with PI controller for the power quality improvement in the distribution system. Here linear load are considered, only when different fault conditions are measured with these loads to analyze the operation of DVR to improve the power quality in distribution system.

A new control strategy has been developed for achieving maximum benefits by eliminating or mitigating voltage sag / swell and power quality problem when abnormal condition occur in the distribution system, for this purpose the dynamic voltage restorer is proposed to improve the power quality and to reduce the sag and swell problem in the system. The DC link capacitor clamped converter is connected with series through transformer. We have proposed that if DC source is integrated with grid, with developing adequate control of grid-interfacing inverter, all objectives can be accomplished either individually or simultaneously. We have implemented the features of DVR for maximum utilization of distribution voltage, which are not fully utilized due to intermittent nature of distribution voltage because our system was highly tapped.

II. POWER QUALITY PROBLEMS AND SOLUTIONS

Power quality means the fitness of electrical power and its stabilized disposition to power consumer device. PQ problem is defined as any problem manifested in voltage, current or a frequency deviation that leads to the failure or disoperation of consumer equipment. Power quality is not a single unit measurement it is a collection of several type which includes Capacitor switching, lightning surge (Transient), Interruptions, Sags/Swells (Disturbance), Harmonics, Flicker, Voltage regulation, Reliability, Power factor (Steady-state).
There are several types of power quality problems that a customer may encounter and may classified according or depending on how the voltage waveform is being distorted. There are transients, short duration of variations (sags, swells, and interruption), long duration variations (sustained interruptions, under voltages, over voltages), voltage imbalance, waveform distortion (dc offset, harmonics, inter harmonics, notching, and noise), voltage fluctuations and power frequency variations.

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Raunak Jangid, Electrical, Shrinathji Institute of Technology & Engineering, Nathdwara, Rajasthan. India.

Kapil Parikh, Electrical, Shrinathji Institute of Technology & Engineering, Nathdwara, Rajasthan. India.

Pradeep Anjana, Electrical, Malaviya National Institute of Technology Jaipur, Rajasthan. India.

A. Voltage Sags

Voltage sag is defined as the reduction of RMS voltage between 0.1 p.u. and 0.9 p.u. and lasting between 0.5 cycles to 1 minute. Voltage sag are mostly caused by system fault and last for duration ranging from 3 cycles to 30 cycles depending on the fault clearing time.

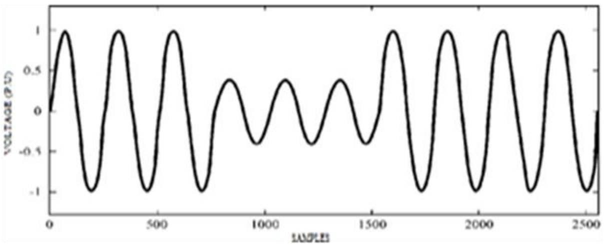

Fig. 1 Voltage Sag

B. Voltage Swells

A voltage swells is defined as a rise in RMS voltage which is between 1.1 p.u and 1.8p.u for period stuck between 0.5 cycles to 1 minute. A voltage swell is characterized by its magnitude (RMS) and duration.

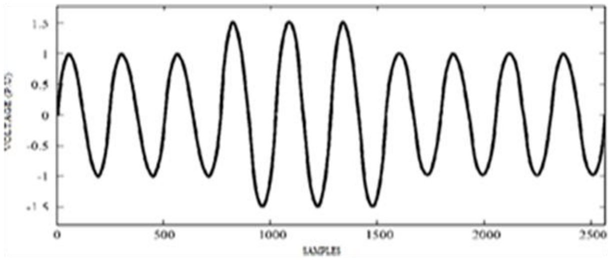

Fig. 2 Voltage Swell

C. Solutions of Power Quality Problems

In general, there are two come within reach of followed to alleviate the tribulations associated with power quality. First approach is called load training, which guarantees that the equipment is less perceptive to power turbulence permitting the operation still below significant voltage deformation and the second approach is to mount line conditioning schemes that suppress or neutralizes the power schemes turbulences. The procession conditioning system or convenience side solutions will participate a major role in improving the inherent supply quality; some of the effective and economic measures can be identified which are as follows: Lightening and Surge Arresters, Thyristor Based Static Switches, Energy Storage Systems, Harmonic Filters etc.

III. DYNAMIC VOLTAGE RESTORER

Among the several type of power quality problems (sags, swells, harmonics) voltage sags are the most severe type of disturbances. In order to overcome problems associated with power quality, the concept of custom power devices is introduced in recent times. One of those devices most recognizable and good in performance is the Dynamic Voltage Restorer, which is the most efficient and effective modern custom power device used in power distribution networks.

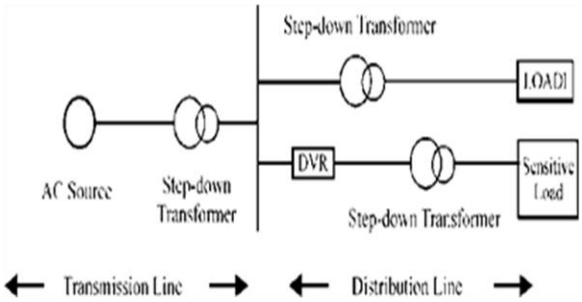

Fig. 3 location of DVR

A. Basic Principle of DVR Operation

A DVR is a solid state power electronics switching device consisting of whichever GTO or IGBT, a capacitor depository as an power storage device and inoculation transformer. It is linked in series between a distribution and a load that shown in figure 4

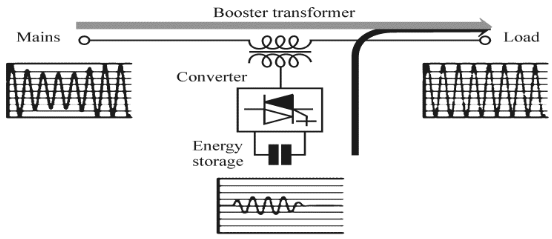

Fig. 4 Principle of DVR with a response time of less than one millisecond

The DVR is capable to generate or absorb reactive power but the active power injection of the device must be provided by an external energy source or energy storage system. The response time of DVR is very short and is limited by the power electronics devices and the voltage sag detection time.

B. Basic Configuration of DVR

The general arrangement of the DVR is composition of Injection/ Booster transformer, Harmonic filter, Storage Devices, Voltage Source Converter (VSC), DC charging circuit, Control and Protection system.

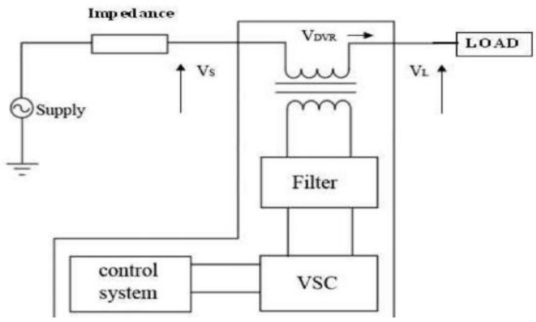

Fig. 5 Schematic diagram of DVR

C. Voltage Injection Methods of DVR

There are four dissimilar methods of DVR voltage injection.

1. Pre-Sag/dip Compensation Method (PDC)

In this technique or procedure the injected vigorous power cannot be managed and it is determined by external condition such as the type of faults.

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Where V_L* is the pre sag voltage.
V_{DVR} = Vpre fault – Vsag

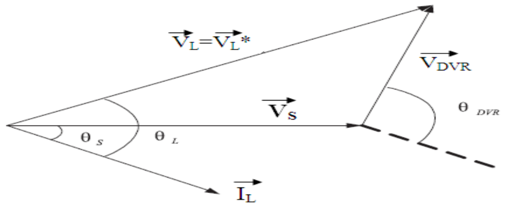

Fig. 6 Single-phase vector diagram of the PDC method

2. In - Phase Compensation Method (IPC)

This method is that the minimum amplitude of DVR injected voltage for certain voltage sag in comparison with other strategies. The practical submission of this scheme is in non-sensitive loads to phase angle jump. Where V_L* is the pre sag voltage and I_L* Pre-sag load current, $\theta_1 = \theta_S$.

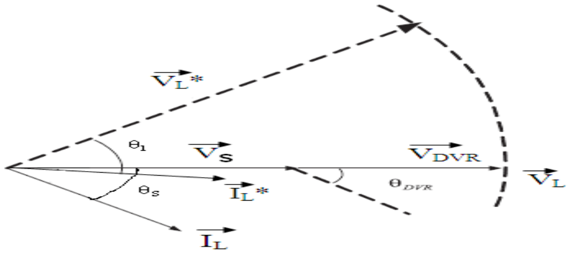

Fig. 7 Single-phase vector diagram of the IPC method

3. In-Phase Advanced Compensation Method (IPAC)

In this method the real power spent by the DVR is decreased by minimizing the power angle between the sag voltage and load current. In this method the vigorous power is generally injected into the system during disturbances.

4. Voltage Tolerance Method with Minimum Energy Injection

This compensation method will maintain the load voltage within the tolerance area with small change of voltage magnitude as shown in Fig -8

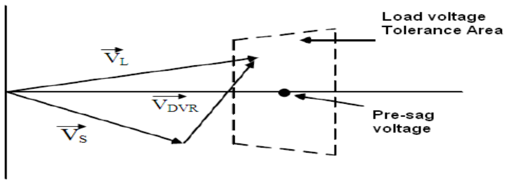

Fig. 8 Voltage tolerance method with minimum energy injection

IV. MATHEMATICAL MODELING OF DYNAMIC VOLTAGE RESTORER SYSTEM

A. Series Voltage Injection by DVR System

The compensation of voltage sag/swell can be limited by a number of factors, which includes limited DVR power rating, loading situations, power class tribulations and types of sag/swell. The electrical circuit model to indicate voltage injection by a DVR system is shown in Fig-9

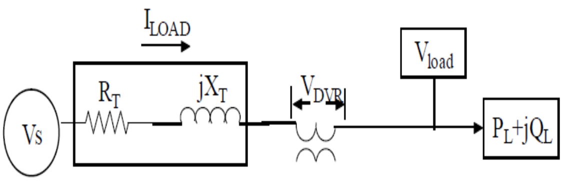

Fig. 9 Electrical Circuit Model for DVR Voltage Injection

The equation for the injected voltage of DVR can be written as

$$V_{DVR} + V_{sf} = V_{Load} + Z_T I_{Load} \quad (1)$$

$$V_{DVR} = V_{Load} + Z_T I_{Load} - V_{sf} \quad (2)$$

Where

$$Z_T = R_T + j X_T \quad (3)$$

Where, VDVR is voltage supply by the DVR, V_{Load} is the desired load voltage magnitude, Z_T is the load impedance, I_{Load} is the load current, V_{sf} is the system voltage during fault condition.

Calculation for the load side current could be done as

$$V_{load} I_{Load} = P_L + j Q_L \quad (4)$$

$$I_{Load} = \left[\frac{(P_L + j * Q_L)}{V_{Load}} \right]$$

Where load voltage consider as a reference, P_L is load active power, and Q_L is load reactive power.

Then DVR voltage can be written as

$$V_{DVR}\angle\alpha = V_L\angle 0^\circ + Z_r I_{Load}\angle(\beta-\theta) - V_{sf}\angle\delta \quad (5)$$

Where α, β and δ are the angles of V_{DVR}, Z_T, and V_{sf} respectively.

$$\theta = \tan^{-1}\left(\frac{Q_L}{P_L}\right) \quad (6)$$

Where θ is load power factor angle.

The obvious electrical power inoculation from DVR is given with

$S = V_{DVR} * I_L$

B. Three-Phase Inverter with Output LC Filter

This Paper work proposes a new and simple MPC scheme for a three-phase inverter with output LC filter.

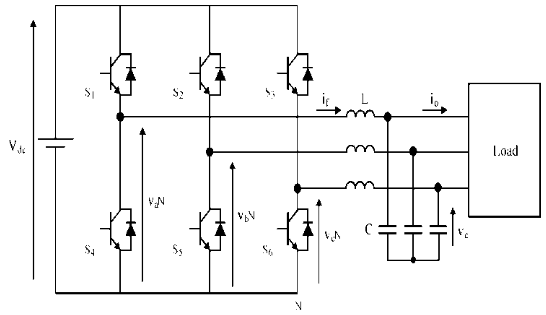

Fig. 10 Three-Phase Inverter with Output LC Filter

The controller uses a model of the structure to envisage, on every sampling intermission, the behavior of the output voltage for each possible switching state, and then, a cost function is used as a criterion for selecting the switching state that will be applied during the next sampling interval.

1. Converter Model

The three-phase inverter with output LC filter considered in this work is shown in fig. 10 The converter and filter models are presented here, and the load is assumed unknown. The switching states of the converter are determined by the Sa, S_b, and Sc gating signals as follows:

$$S_a = \begin{cases} 1, & \text{if } S_1 \text{on and } S_4 \text{ off} \\ 0, & \text{if } S_1 \text{off and } S_4 \text{ on} \end{cases} \quad (7)$$

$$S_b = \begin{cases} 1, & \text{if } S_2 \text{on and } S_5 \text{ off} \\ 0, & \text{if } S_2 \text{off and } S_5 \text{ on} \end{cases} \quad (8)$$

$$S_c = \begin{cases} 1, & \text{if } S_3 \text{on and } S_6 \text{ off} \\ 0, & \text{if } S_3 \text{off and } S_6 \text{ on} \end{cases} \quad (9)$$

These could be articulated vectorial structure by

$$S = \frac{2}{3}(S_a + aS_b + a^2 S_c) \quad (10)$$

Where $a = e^{j(2\pi/3)}$

Subsequent equation will characterize the output-voltage gap vectors generated by the inverter

$$v_i = \frac{2}{3}(v_{aN} + av_{bN} + a^2 v_{cN}) \quad (11)$$

Where v_aN, v_bN, and v_cN are the phase voltages of the inverter, with respect to the negative terminal of the dc-link N (see fig. 10). Then, the load voltage vector v_i can be related to the switching state vector S by

$$v_i = V_{dc} S \quad (12)$$

Where, V_{dc} is the dc-link voltage.

Considering all the possible combinations of the S_a, S_b, and S_c gating signals, eight switching situations and, thus, eight voltage vectors are attained. Note that $v_0 = v_7$, resulting in only seven different voltage vectors, as shown in fig. 11

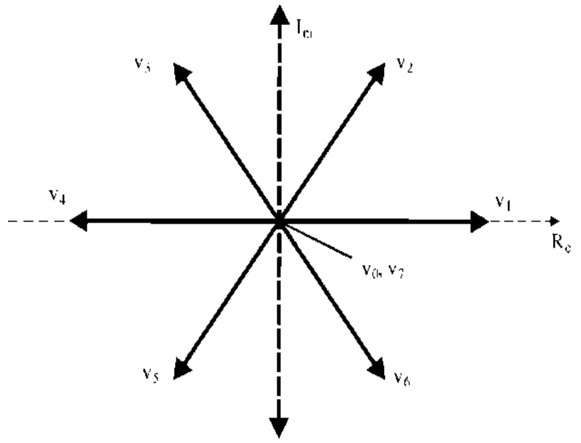

Fig. 11 Possible Voltage Vectors Generated by the Inverter.

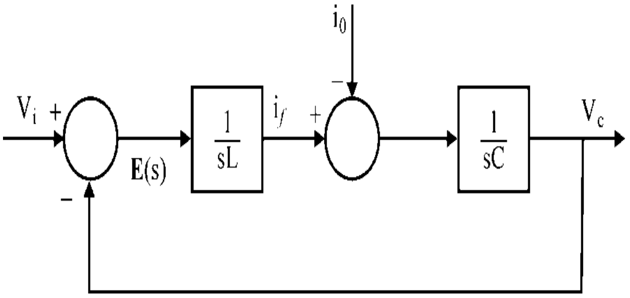

Fig. 12 LC filter model.

Using modulation techniques like pulse width intonation, the inverter can be reproduced as a continuous system. Nevertheless, in this paper, the inverter is considered as a nonlinear discrete system with only seven different voltage vectors as possible outputs.

Using vectorial notation, the filter current if , the output voltage vc, and the output current i_o can be expressed as space vectors and are defined as

$$i_f = \frac{2}{3}(i_{fa} + ai_{fb} + a^2 i_{fc}) \quad (13)$$

$$v_c = \frac{2}{3}(v_{ca} + av_{cb} + a^2 v_{cc}) \quad (14)$$

$$i_o = \frac{2}{3}(i_{oa} + ai_{ob} + a^2 i_{oc}). \quad (15)$$

The LC filter is modeled as shown in the block diagram in fig. 12. This model can be described by two equations, one that describes the inductance dynamics and the other describing the capacitor dynamics.

The filter inductance equation for vectorial form is

$$L\frac{di_f}{dt} = v_i - v_c \quad (16)$$

Where, L is the filter inductance.

The dynamic behavior of the output voltage can be expressed by the following:

$$C\frac{dv_c}{dt} = i_f - i_o \quad (17)$$

Where, C is the filter capacitance.

The above stated equations could be rephrase as a state-space structure as

$$\frac{dx}{dt} = Ax + Bv_i + B_d i_o \quad (18)$$

where

$$x = \begin{bmatrix} i_f \\ v_c \end{bmatrix} \quad (19)$$

$$A = \begin{bmatrix} 0 & -1/L \\ 1/C & 0 \end{bmatrix} \quad (20)$$

$$B = \begin{bmatrix} 1/L \\ 0 \end{bmatrix} \quad (21)$$

$$B_d = \begin{bmatrix} 0 \\ -1/C \end{bmatrix}. \quad (22)$$

Variables i_f and v_c are measured, while v_i can be calculated using (12), and i_o is considered as an unknown disturbance. The value of V_{dc} is assumed fixed and known. The output of the system is the output voltage v_c and written as a state equation

$$v_c = [0 \quad 1]x. \tag{23}$$

2. Discrete-Time Model of the Filter

A discrete-time model of the filter is obtained from (16) for a sampling time Ts and is expressed as

$$x(k+1) = A_q x(k) + B_q v_i(k) + B_{dq} i_o(k) \tag{24}$$

where

$$A_q = e^{AT_s} \tag{25}$$

$$B_q = \int_0^{T_s} e^{A\tau} B d\tau \tag{26}$$

$$B_{dq} = \int_0^{T_s} e^{A\tau} B d\tau \tag{27}$$

The above stated equations are used as the analytical model in the proposed predictive controller.

In order to predict the output voltage using (24), the output current i_o is needed, but generally, this electrical power is not deliberated, and the load is unknown. A simple estimation of the load current can be calculated from filter-current and output-voltage measurements using the following equation obtained from (17):

$$i_o(k-1) = i_f(k-1) - \frac{C}{T_s}(v_c(k) - v_c(k-1)). \tag{28}$$

Nevertheless, this inference is very responsive to noise in the measurements, because it is based on the derivative of the output voltage, so it will be preferred to use an observer such as the one presented in the next section.

3. Load-Current Observer

The load current depends on the load connected at the output of the filter which is unknown. However, some considerations can be taken in order to build an appropriate observer. These Considerations consist of assuming a certain dynamic behavior of the load current. A simple consideration is to assume that the load current is shifting awfully slowly but surely, in comparison to the sampling rate of recurrence.

Let's assume that the load current can be approximated as a constant, so its behavior is described by the following differential equation:

$$\frac{di_o}{dt} = 0 \tag{29}$$

Then, including this load-current model in the filter model, the system is described by the following state-space equations:

$$\frac{d}{dt}\underbrace{\begin{bmatrix} i_f \\ v_c \\ i_o \end{bmatrix}}_{x} = \underbrace{\begin{bmatrix} 0 & -\frac{1}{L} & 0 \\ \frac{1}{C} & 0 & -\frac{1}{C} \\ 0 & 0 & 0 \end{bmatrix}}_{A} \begin{bmatrix} i_f \\ v_c \\ i_o \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix}}_{B} v_i. \tag{30}$$

The output of this system is the two measured variables that are the filter current and the output voltage, and is defined by the following equation:

$$y = \underbrace{\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix}}_{C} \begin{bmatrix} i_f \\ v_c \\ i_o \end{bmatrix}. \tag{31}$$

A full-order observer for the system can be used to estimate the state vector x. A spectator is an open-loop model of the scheme which includes a correcting term based on the designed acquiesces. That is

$$\frac{d\hat{x}}{dt} = A\hat{x} + Bv_i + J(y - \hat{y}) \tag{32}$$

Where $\hat{y} = C\hat{x}$ and J is the so-called observer gain [31].

The particular equation can be rephrased as

$$\frac{d\hat{x}}{dt} = A_{obs}\hat{x} + [B \quad J]\begin{bmatrix} v_i \\ i_f \\ v_c \end{bmatrix} \tag{33}$$

Where $A_{obs} = A - JC$. The output of the observer is the estimated load current

$$\hat{i}_o = [0\ 0\ 1]\hat{x}. \tag{34}$$

Note that the observer can be understood just as a filter which gives an estimate of the (unknown) load current $\hat{i}_o$, based on measurements of the filter current i_f , the output voltage v_c, and the inverter voltage v_i. Matrix gain J will define the observer dynamics. A simpler alternative is to choose the observer gain such that the poles of the observer give dynamics several times faster than the open-loop system dynamics.

V. IMPLEMENTATION OF DYNAMIC VOLTAGE RESTORER SYSTEM USING IN MATLAB/ SIMULATION

A. Proposed Without DVR System Model

In this presented SIMULINK model in the systematic configuration we have a system in which two parallel feeders are shown. In both the feeders, further loads are also connected in parallel.

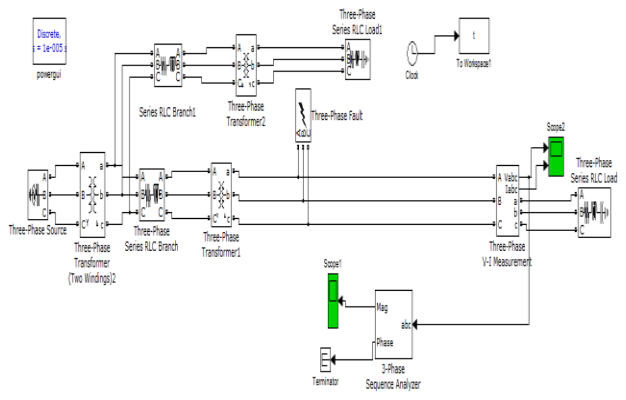

Fig. 13 Proposed Without DVR System Model in MATLAB/SIMULINK

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B. Proposed With DVR System Model

In this SIMULINK model there is a system in which two parallel feeders are presented and in both the feeders, further loads are also connected in parallel. PI controller is used for the control purpose. Here DVR system is connected to the distribution system using a booster transformer. In order to study the effects of the entire DVR System the proposed system is modeled using MATLAB/SIMULINK environment by using different toolboxes

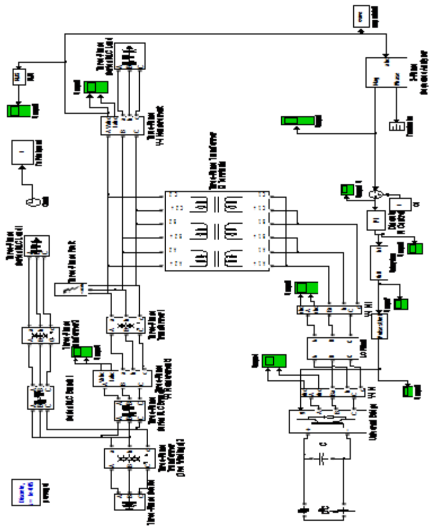

Fig. 14 Proposed with DVR System Model in MATLAB/SIMULINK

C. PI Controller

The aim of the control scheme is to maintain a constant voltage magnitude at the sensitive load point, under the system disturbance. The control system only measures the RMS voltage at load point; for example, no reactive power measurement is required in the DVR controller scheme implemented in MATLAB/SIMULINK.

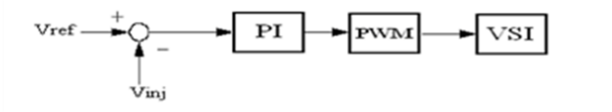

Fig. 15 PI controller

The modulating angle δ or delta is applied to the PWM generators in phase A, whereas the angles for phase B and C are shifted by 240° or -120° and 120° respectively

$V_A = \text{Sin}\ (\omega t + \delta)$ (35)

$V_B = \text{Sin}\ (\omega t + \delta - 2\pi/3)$ (36)

$V_C = \text{Sin}\ (\omega t + \delta + 2\pi/3)$ (37)

This is the output of the subsystem as shown in the Fig -16

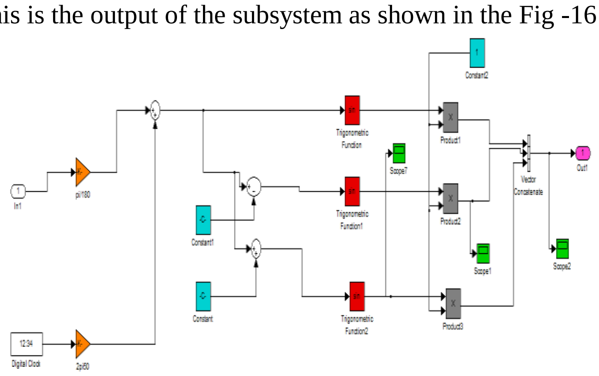

Fig. 16 Phase-Modulation of the control angle δ

Fig. 17 shows that there is an error signal applies to proportional gain (Kp) and integral gain (Ki). Proportional gain (Kp) is applied to zero order hold, the Zero-Order hold block samples and holds its input for the specified samples period.

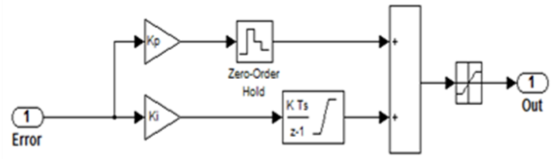

Fig. 17 Discrete PID Controller

D. Sequence Analyzer

The Three-Phase Sequence Analyzer block outputs the magnitude and segment of the positive, negative, in addition to zero-progression mechanism of a set of three balanced or unstable signals. A Fourier analysis over a sliding window of one cycle of the specified frequency is very firstly applied to the three input signals. The discrete version of this block allows specifying the initial magnitude and phase of the output indication.

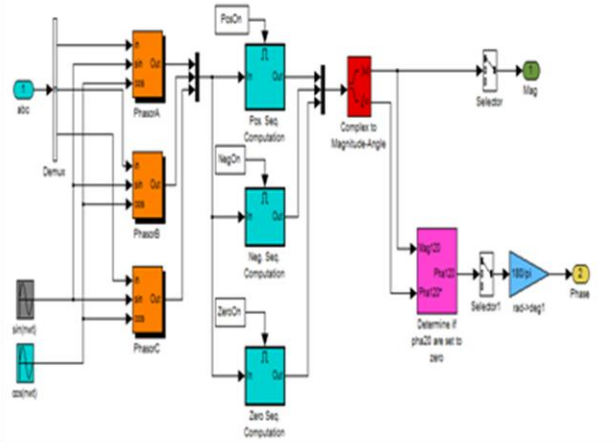

Fig. 18 Three Phase sequence analyzer

E. LC Filter

It is presented that as well as the input is Three Phased and output is also three phases in mediator connect. A three phase series L branch inductance is 2mh and 25µF capacitor are connected in LC filter and three phase series RLC load

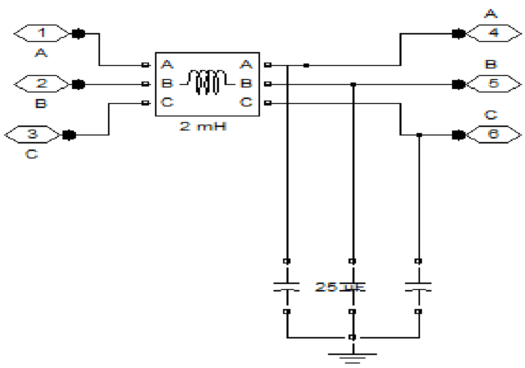

Fig. 19 LC filter

Fig -20 shows that if the control signal of the switch is greater than or equal to the given threshold value, after that it will get ahead of its contribution, in this casing since the switch is closing on to the first input and vice versa, (otherwise will pass third input i.e. Uref).

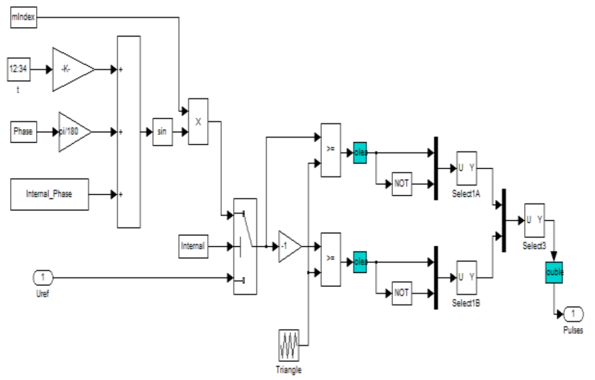

Fig. 20 Discrete PWM generator

VI. SIMULATION RESULTS AND DISCUSSION

In this paper, simulation results for the developed Dynamic Voltage Restorer system connected to the distribution system is presented for both the with and without DVR system conditions. Several different conditions' i.e. voltage rise, voltage dip, single line to ground, double line to ground, triple line to ground etc. simulation result are presented to validate the developed models and control for the proposed DVR system.

A. Simulink Performance of DVR in Voltage Swell and Sags Conditions

1. Response for Voltage Rise of 50% with and without DVR

Fig -21 presents the generation of voltage swell, the supply three-phase voltage amplitudes were increased about 150% of nominal voltage. Here, the performance of DVR for a voltage swell condition was analyzed. Here, the furnish voltage swell up was generated as shown in Fig -22.

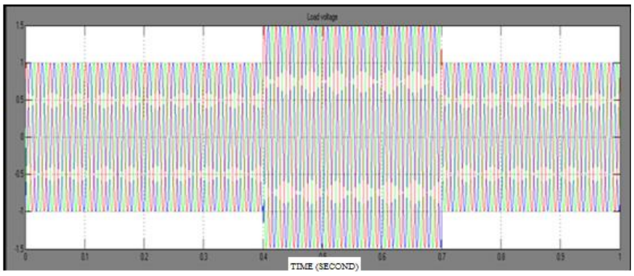

Fig. 21 Three Phase Voltage Swell of 50% without DVR

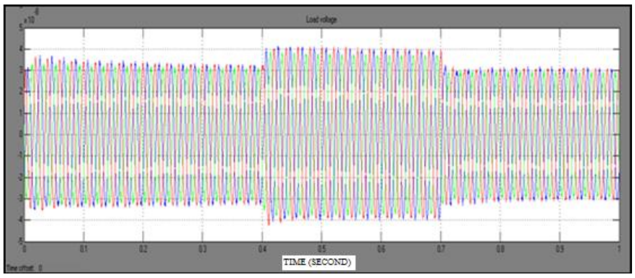

Fig. 22 Three Phase Voltage Swell of 50% with DVR

2. Response for Voltage Rise of 75% without DVR

Here, the supply voltage swell was generated as shown in Fig -25 and the supply three-phase voltage amplitudes were increased about 150% of nominal voltage. But in this case when DVR is not used and voltage rises by 75%, then amplitude of load voltage decreases by 125% as compared to voltage rise of 50%.

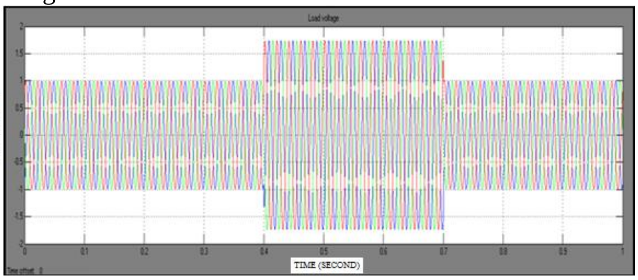

Fig. 23 Three Phase Voltage Swell of 75% without DVR

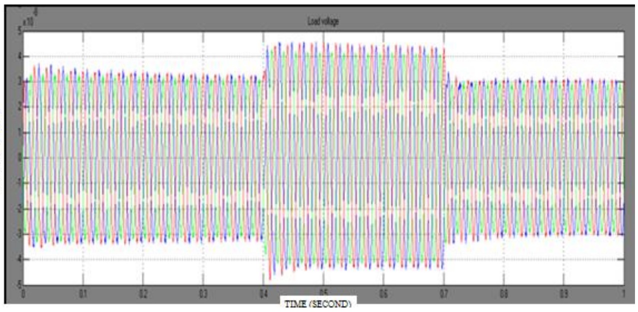

Fig. 24 Three Phase Voltage Swell of 75% with DVR

3. Response for Voltage dips of 50% with and without DVR

In this case when DVR is not used and voltage dip is 50 % then simulation results is the amplitude load voltage descried 125 % as compared to response for voltage of 50% with DVR

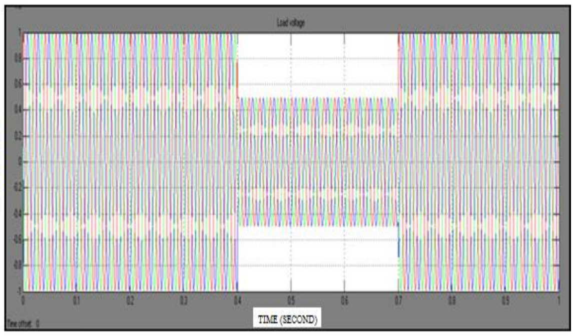

Fig. 25 Three Phase Voltage Sag of 50% without DVR

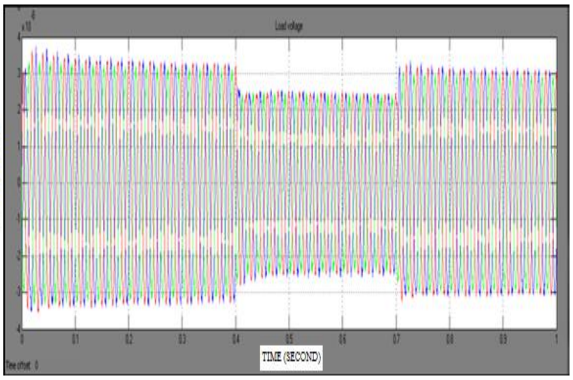

Fig. 26 Three Phase Voltage Sag of 50% with DVR

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4. Response for Voltage dips of 75% with and without DVR

In this case when DVR is not used and voltage dip of 75 % then simulation result is the amplitude load voltage descried 150 % as compared to response for voltage of 75 % with DVR.

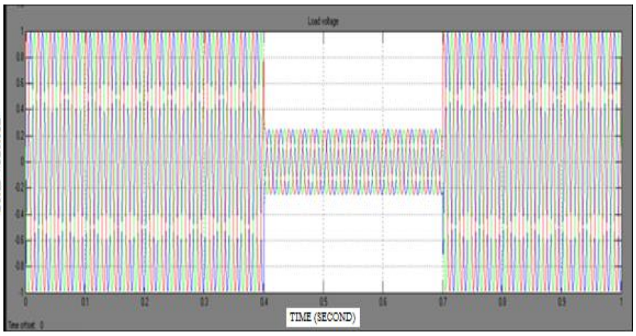

Fig. 27 Three Phase Voltage Sag of 75% with DVR

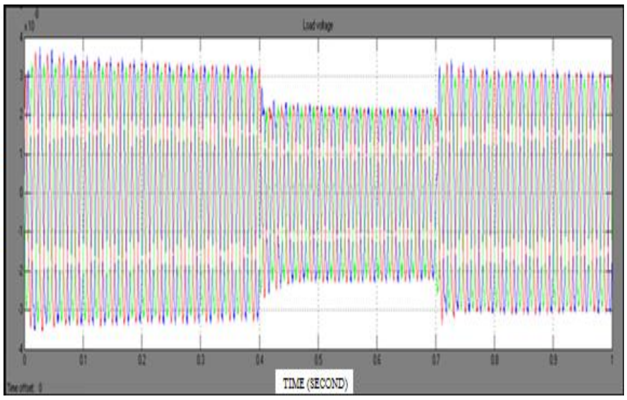

Fig. 28 Three Phase Voltage Sag of 75% With DVR

B. Simulink Model of the Proposed DVR System with different Fault Conditions

1. Simulink Results of Proposed normal System

Result for the above system in which no fault is produced in given below. The output presents the Load voltage and current condition without fault and DVR.

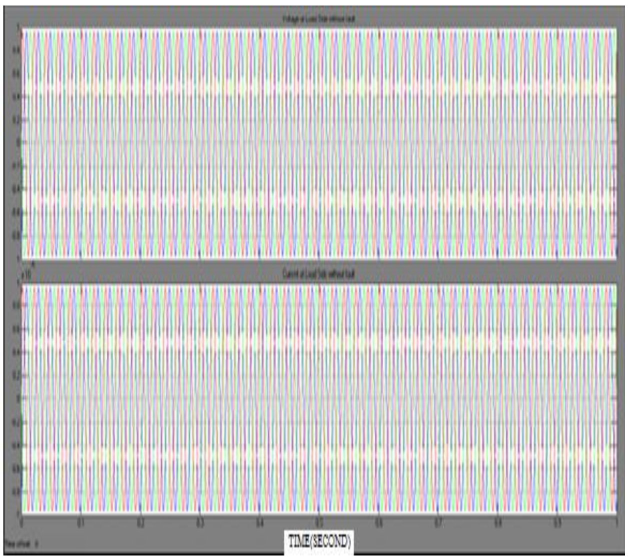

Fig. 29 Output Results of Load voltage, current, for a normal System

2. Single Line to Ground Fault with and without DVR condition

In this model a single line to ground fault is shaped for both the feeders. Here the fault resistance is 0.9 ohms and the ground resistance is 0.001ohms. The fault time is 0.4s to 0.5s. The result of single line to ground fault without DVR

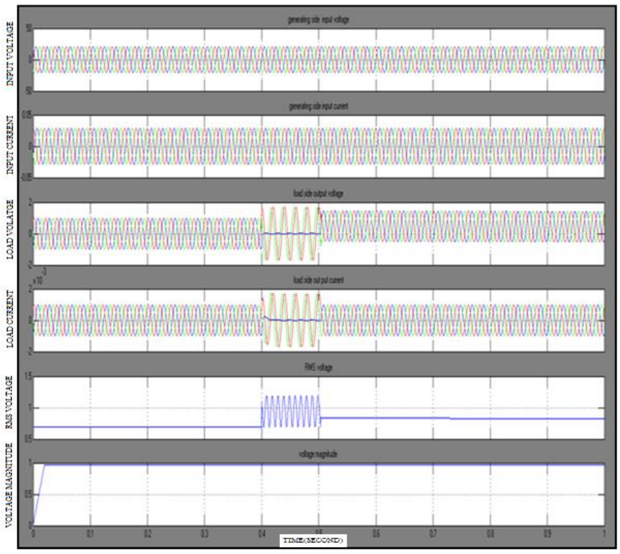

Fig. 30 Output Results of Input voltage, current, Load voltage, current, RMS voltage, voltage magnitude for Single Line to Ground without DVR

The wave shapes of both the load voltage and current i.e. without DVR and with DVR are compared. Where DVR is connected is compensated to large extent for single line to ground fault in the distribution network.

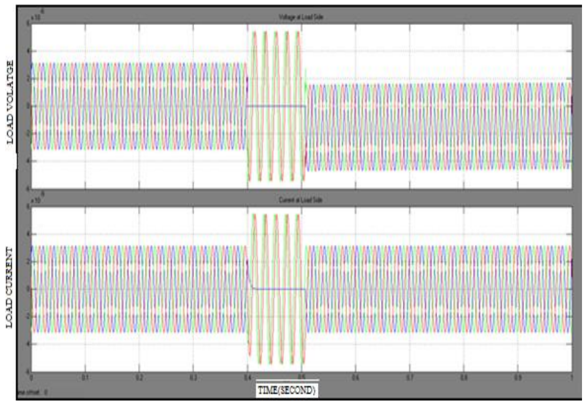

Fig. 31 Load Voltage and Current without DVR

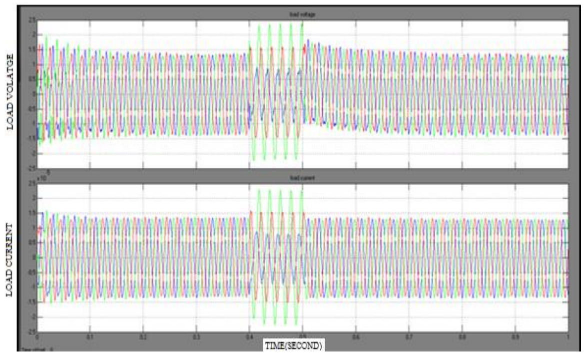

Fig. 32 Load Voltage and Current with DVR

3. Double Line to Ground Fault with and without DVR Condition

In this model a Double line to ground fault is shaped in both the feeders. Here the fault resistance is 0.9 ohms and the ground resistance is 0.001ohms. The fault time is 0.4s to 0.5s. Output Result for Double Line to Ground Fault with DVR.

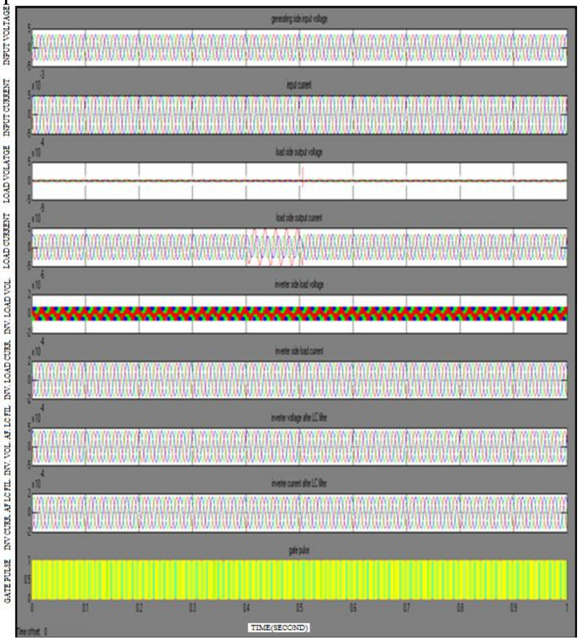

Fig. 33 Output Result of Input voltage, current, Load voltage, current, Inverter voltage, current, Inverter voltage After LC filter, current and gate pulse for Double Line to Ground Fault with DVR

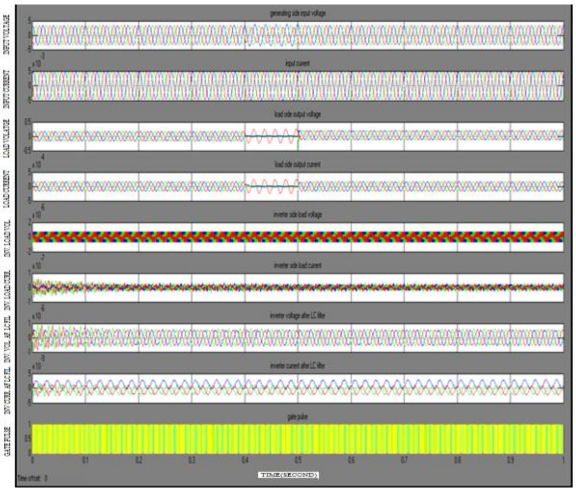

Fig. 34 Output Result of Input voltage, current, Load voltage, current, Inverter voltage, current, Inverter voltage After LC filter, current and gate pulse for Double Line to Ground Fault without DVR

The wave shapes of both the load voltage and current i.e. without DVR and with DVR compared. Where DVR is connected is compensated to large extent for double line to ground fault in the distribution network.

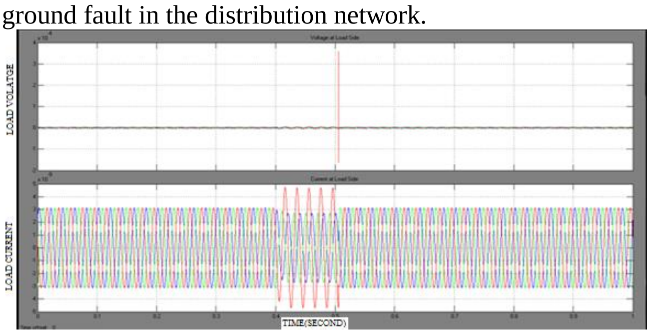

Fig. 35 Load Voltage and Current with DVR

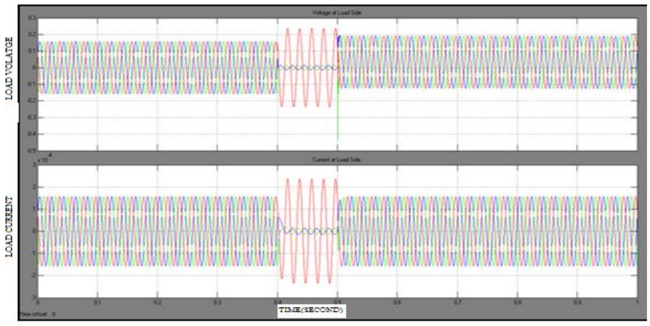

Fig. 36 Load Voltage and Current without DVR

4. Triple Line to Ground Fault with and without DVR Condition

In this system voltage dip is introduced in both the feeders for the period of 0.4s to 0.5s by means of three phases to ground error with fault resistance is 0.9 ohms and the ground resistance is 0.001ohms.

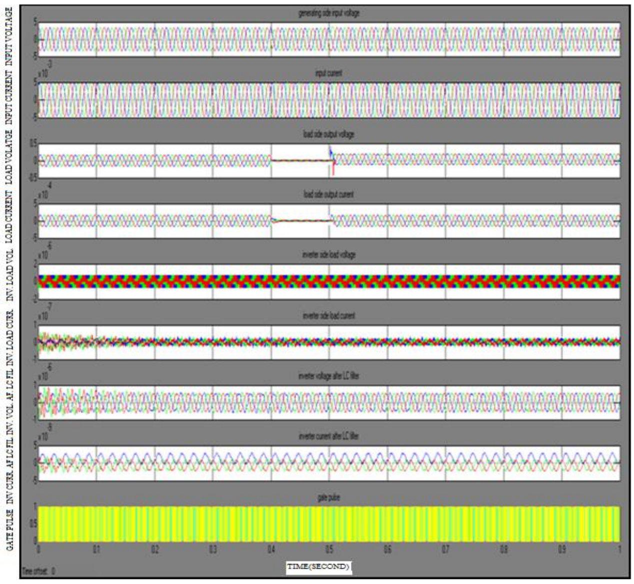

Fig. 37 Output Result of Input voltage, current, Load voltage, current, Inverter voltage, current, Inverter voltage After LC filter, current and gate pulse for Triple Line to Ground Fault without DVR

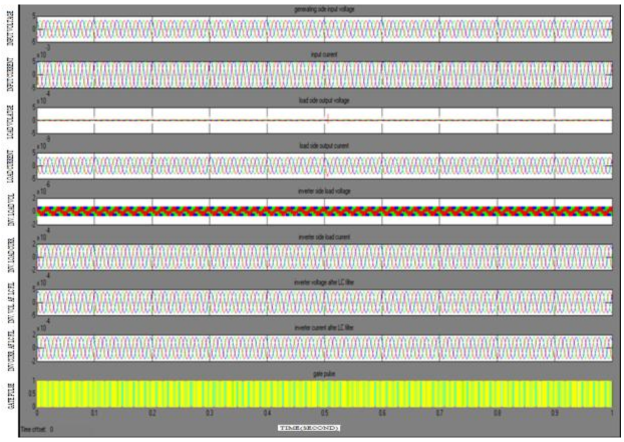

Fig. 38 Output Result of Input voltage, current, Load voltage, current, Inverter voltage, current, Inverter voltage After LC filter, current and gate pulse for Triple Line to Ground Fault with DVR

VII. CONCLUSION AND FUTURE SCOPE OF WORK

A. Conclusion

This report had presented the power quality problems such as voltage sag with the compensation techniques of custom power electronics device DVR. This research work presents comprehensive results for the design and application of DVR for voltage sag. A controller utilizes the error signal which is actually the difference between the reference signal and the actual signal. Voltage source convertor (VSC) was implemented with the help of pulse width modulation. Modeling and Simulation of DVR is done through MATLAB/SIMULINK computer software. The simulation carried out here shows that DVR provide better voltage regulation capabilities. Based on analysis of test system, it is suggested that percentage sag and operating voltage are major factors in estimating the requirement of DC storage capacity. The effectiveness of a DVR system mainly depends upon the amount and stiffness of DC energy storage device. Investigations were carried out for various cases of voltage sags at different transmission voltage levels. Result show that any increase in transmission voltage and voltage sag demands sufficient increase in DC storage capacity. An expression is developed to estimate the required DC storage voltage for specified transmission voltage and percentage sag. In the test system, it is observed that after a particular amount of increases in the load on feeders, the voltage levels at the load terminal decreases

B. Future Scope

The following issues are under recommendation for future work in DVR:

- Change the controller of DVR like fuzzy based controller, ANN based controller and PSO based controller scheme.
- The multi-level DVR can be investigated for future work.
- Use of DVR for interconnecting the renewable source to grid.

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AUTHORS PRFOILE

Raunak Jangid (1985) Bachlor of Engineering in Electrical Engineering (2009). Currently pursuing Master of Technology in Power System from Shrinathji Institute of Technology & Engineering, Nathdwara, Rajasthan. His Research Interests are in Power System, Renewable Source of Energy.

Kapil Parikh (1978) Bachlor of Engineering in Electrical Engineering (2009). Master of Technology in Power System Engineering (2013) from Institute of Technology and Management, Bhilwara, Rajasthan. He is working as Assistant Professer in the Department of Electrical Engineering Shrinathji Institute of Technology & Engineering, Nathdwara; Rajasthan His Research Interests are in Power System, Renewable Source of Energy.

Pradeep Anjana research scholar Malaviya National Institute of Technology Jaipur received B.E. and M.Tech Degree from University of Rajasthan & MNIT Jaipur currently pursuing PhD and area of research is Power Quality of Renewable Energy Sources.