

Design and Implementation of Multilevel QAM Band pass Modems (8QAM, 16QAM, 32QAM and 64QAM) for WIMAX System Based on SDR Using FPGA

Hadi T. Ziboon, Muhannad Y. Muhsin

Abstract— The objective of this paper is to simulate, design and implementation of a proposed system of multilevel bandpass QAM modems (modulation/demodulation) schemes with selectable technique between them based on Software Defined Radio (SDR) using FPGA for WIMAX system. These modems are 8QAM, 16QAM, 32QAM and 64QAM. MATLAB-Simulink tool and M-files are used to design these modems. "Simulink HDL Coder" is used to convert all files to VHDL Codes for hardware implementation using FPGA Altera-Cyclone II Family DE2 board. Simulink HDL Coder proves the capabilities to generate Hardware Description Language (HDL) code to MATLAB model (Simulink and M-file) for complex units of proposed system. The complex units are converted to simple units compatible with Simulink HDL Coder. The experimental results show that there is coincidence between transmitted and received data with average time delay of (0.35-0.40μsec) for different data rate (1.5-3Mbps).

Keywords: FPGA, SDR, Simulink HDL Coder, VHDL and WIMAX.

I. INTRODUCTION

The wireless communications revolution started with the mobile phone at the beginning of the 80's and all the improvements which have led to the multiplication of mobile and wireless communications networks and standards [1]. Wireless communication systems are rapidly evolving through the incessant extension of the old standards with the new generations. A side effect of this rapid growth is an excess of mobile system standards; every major country has its own standards. Therefore, the software defined radio (SDR) concept is emerging as a potential pragmatic solution [2]. SDR is a new communication system architecture in the field of wireless communications. It has played a huge role in guiding the development of communication systems [3,4].

The software radio architecture consists of three major sections RF section, IF section and Baseband section. RF section which includes antenna and RF front-end which are fixed hardware. IF section and Baseband section perform signal processing functions. However, Analog to Digital Converter (ADC) and Digital to Analog Converter (DAC) will be required for trans-receiver. Silicon technology provides common platforms for SDR implement, such as Field Programmable Gate Arrays (FPGAs), Digital Signal Processors (DSPs), General Purpose Processors (GPPs) and Application-Specific Integrated Circuits (ASICs) [5,6].

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MathWorks introduced Simulink HDL Coder, in 2006, which automatically generates synthesizable Hardware Description Language HDL Codes. Simulink HDL Coder with MATLAB facility can be considered as a compact package which includes the analysis, design, implementation and verification of hardware, thus providing a path directly from system models to programming FPGA. The design and implementation of the SDR proposed system based on HDL Simulink Coder give more flexibility and more confidence because of the ability to examine the system performance at any point in the design process.

II. QAM SYSTEM

Quadrature Amplitude Modulation (QAM) is a type of high spectral efficiency modulation technique that is widely used by mobile cellular communications [7]. QAM signals are normally generated by summing two amplitude modulated signals with carriers that are ninety degrees out of phase. The QAM signal is given by:

$$s(t) = A(t) [\cos(\varphi(t)) \cos(2\pi fct) - \sin(\varphi(t)) \sin(2\pi fct)] \quad (1)$$

Then, Equation (1) can be simplified as shown below

$$s(t) = AI(t) \cos(2\pi fct) - AQ(t) \sin(2\pi fct) \quad (2)$$

where the modulating signals

$$AI(t) = A(t) \cos(\varphi(t)) \text{ and} \\ AQ(t) = A(t) \sin(\varphi(t)).$$

However, modulation schemes with high spectral efficiencies are often quite sensitive to noise and can result in high bit error rates, as is the case with high-level QAM constellations. For this reason, many new systems adapt the QAM constellation to the channel conditions. Multilevel Quadrature Amplitude Modulation (M-QAM) extends QAM by making the size of the transmitted constellation variable. The variable constellation size means that the number of bits per symbol is also variable. Therefore, as the number of bits per symbol increases, the rate at which the information can be sent also increases as long as the symbol rate remains constant. This leads to the possibility of variable bit rate operation in a constant bandwidth. Figure (1) shows the constellation of 4QAM, 16QAM, 64QAM. Figure (2) and Figure (3) show the QAM transmitter and receiver block diagram respectively [8, 9].

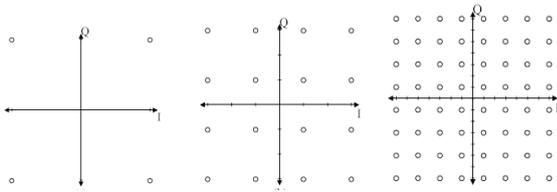


Figure (1): Constellation diagram of 4QAM, 16QAM, 64QAM

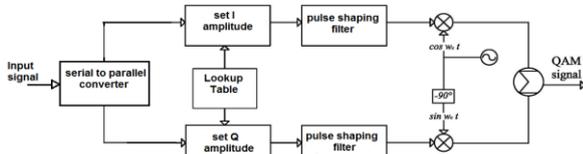


Figure (2) : Block diagram of QAM transmitter

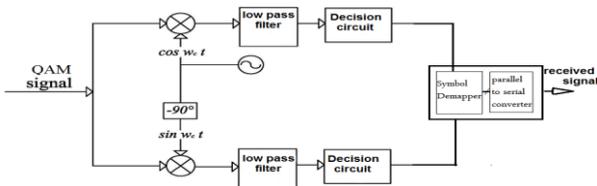


Figure (3): Block diagram of QAM receiver

III. DESIGN AND IMPLEMENTATION PROCEDURE OF THE PROPOSED SYSTEM

Figure (4) shows the block diagram of the proposed system. The main parts and functions of the implemented proposed system are:

1. Transmitter: The transmitter is responsible for generating the symbols of the transmitted data which is transmitted over a wireless channel.
2. Receiver: which is responsible for data reception and demodulation of the received data.

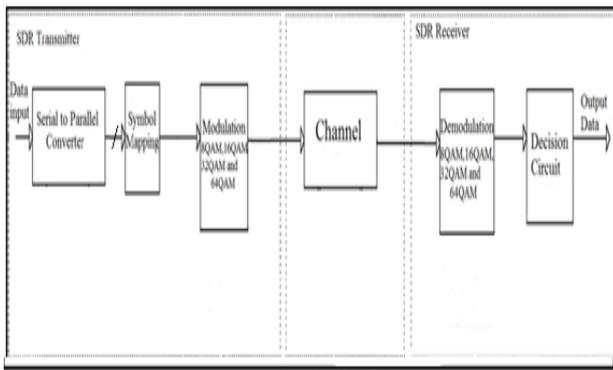


Figure (4) General layout of the proposed system

Figure (5) describes the design and implementation procedure used for the proposed SDR system. The SDR parameters are set up according to IEEE802.16e WIMAX standard. Then, the design is implemented as a model using MATLAB (combination MATLAB-Simulink and M-file) and functional simulation is performed to performance evaluation. When the design behavior becomes persuaded, the next step would be generating VHDL codes for the model as well as generating test benches for simulation purposes. The design behavior is tested once again but this time in digital environment using ModelSim tool provided by Altera. Finally, the generated VHDL netlists are synthesized and downloaded to FPGA board.

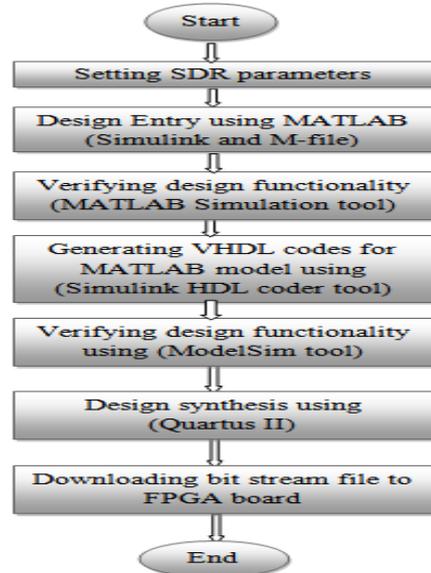


Figure (5): Design procedure of the proposed SDR System

The proposed system was designed based on MATLAB (Simulink and M-file) to satisfy the functionality of the SDR proposed system. However the Simulink HDL Coder is used to convert to VHDL codes. Codes are used to implement SDR proposed system in FPGA hardware platform. Some MATLAB-Simulink blocks and MATLAB codes for M-file, especially those that contain complex functions, modulator, demodulator, filter coefficient parameters and carrier signals specifications can not be converted to VHDL codes directly. To solve these problems, these blocks are redesigned using their basic components such that they can be converted to VHDL codes, change the coefficient parameters and used MATLAB instructions codes suitable for converted to VHDL codes.

The system parameters setting includes specifying the different types of modulation/demodulation and other related system operations that the SDR could handle [10]. Table (1) shows the proposed design system parameters. The SDR system is very flexible and can change its parameters easily.

Table (1): Design system parameters

Item	Font	Size
Modulation type	8QAM, 16QAM, 32QAM, 64QAM	MQAM is used in this system to increase data rate of transmission.
IF frequency	10MHz	Moderate frequency can be used to implement SDR system.
Sampling frequency	100MHz	This value is selected for better simulation results.
Decision circuit	Soft Decision circuit	Multilevel decision circuit used to demodulate the MQAM modulated signal to return the transmitted data.
Arm filter	50 lengths of FIR filter type	Because it has linear phase response.

IV. GENERATION OF VHDL CODES FOR THE PROPOSED SYSTEM

USING HDL SIMULINK CODER

Simulink HDL Coder generates bit-true and cycle-accurate, synthesizable Verilog and VHDL code from Simulink models, M-files of MATLAB codes, and Stateflow charts. The generated HDL code can be simulated and synthesized using industry-standard tools and then implemented on FPGAs or ASICs. Simulink HDL Coder can be used to generate the Hardware Description Language (HDL) code based on Simulink models and Stateflow finite-state machines. The coder brings the Model-Based Design approach into the domain of (ASIC) and (FPGA) development. The time spent by designer to fine tuning algorithms and models can be reduced by using HDL Simulink Coder[11].

The coder generates synthesis scripts for the Synplify family of synthesis tools. In this work, The Quartus II 9.0 web edition used as synthesis software have been used. The default settings of Simulink HDL coder are not compatible with Quartus II (compatible with Synplify synthesis software as mentioned above), therefore a control file (MATLAB file) is used to change the coder settings to be compatible with Quartus II 9.0 web edition synthesis software.

V. VERIFYING DESIGN FUNCTIONALITY USING MODELSIM SIMULATION TOOL

Simulation may be defined as the process of verifying the functional characteristics of models at any level of abstraction. VHDL simulation verifies the functionality of the system i.e., given the expected input and test whether the outputs are as expected or not. A VHDL testbench and data vectors, which have been created by MATLAB Simulink Coder tool and use ModelSim-Altera 6.4a (Quartus II 9.0) Starter Edition simulation tool to simulate the VHDL Codes. ModelSim provides a complete HDL simulation environment that enables verifying the functional and timing models of the design, and the VHDL source code.

VI. DESIGN SYNTHESIS OF THE PROPOSED SYSTEM USING QUARTUS II

Design Synthesis is a process that starts from a high level of logic abstraction (typically Verilog or VHDL) and automatically creates a lower level of logic abstraction of the proposed system. The first step in the synthesis process is compilation. Compilation is the conversion of the high-level VHDL language, which describes the circuit at the Register Transfer Level (RTL), into a netlist at the gate level.

The second step is optimization, which is performed on the gate-level netlist of VHDL Codes to get optimal speed of execution and minimize the area of FPGA (NO. of units of FPGA which is used). Finally, place-and-route (fitter) software will generate the physical layout for a PLD/FPGA chip or will generate the masks for an ASIC.

In this work, Quartus II 9.0 software has been used, providing a complete design environment for System On a Programmable Chip (SOPC) design, which ensures easy design entry, fast processing, and straightforward device programming. Altera-Cyclone II FPGA family- DE2 Kit is used as a target device for implementation purposes.

VII. IMPLEMENTATION OF 8QAM, 16QAM, 32QAM, 64QAM SYSTEMS TECHNIQUE BASED ON FPGA

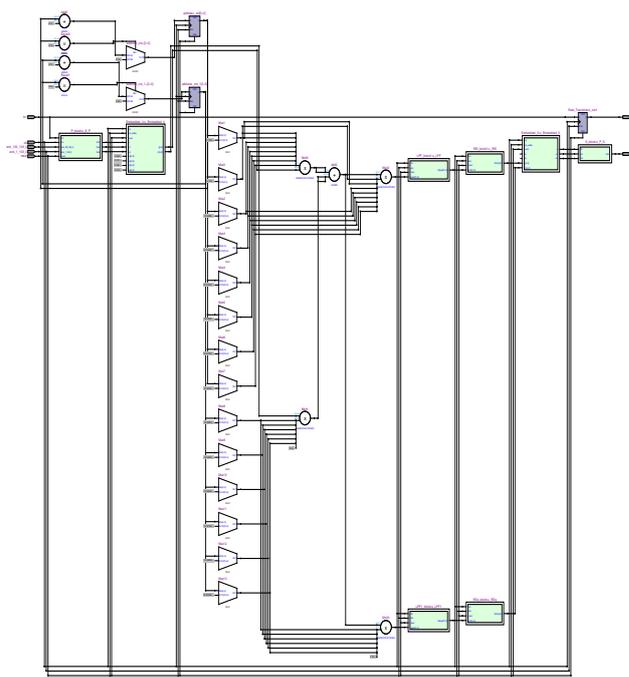


Figure (6) The implementation of the 8QAM technique

Figure (6) shows the implementation of the 8QAM System technique based on Altera- Cyclone II FPGA-DE2 board. The input serial data have been passed in the serial to parallel converter circuit for the 8QAM specification and bassband modulated by embedded4 circuit then multiplied in the IF stage by the carrier signals (digital sin for I-Channel and digital cos for Q-Channel) and they are mixed to transmit 8QAM bandpass modulated signal. in the receiver, the 8QAM bandpass modulated signal has been demodulated by multiplying it by the carrier signals in the receiver IF stage and filtered to extract two channels bassband signals (I&Q) then decision circuits are used for I&Q channels and embedded5 circuit is used to bassband demodulate signals finally, the parallel to serial converter circuit is used to return the serial data. Figure (7) shows the implemented embedded4 circuit (used to bassband modulated signal). Figure (8) shows the implemented embedded5 circuit (used to bassband demodulated signal). Figure (9) and Figure (10) show the implemented decision circuits for I&Q channels respectively.

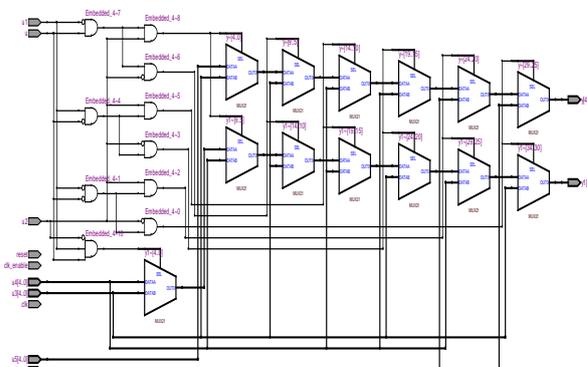


Figure (7) The implemented embedded4 circuit of 8QAM (using for bassband modulated signal)

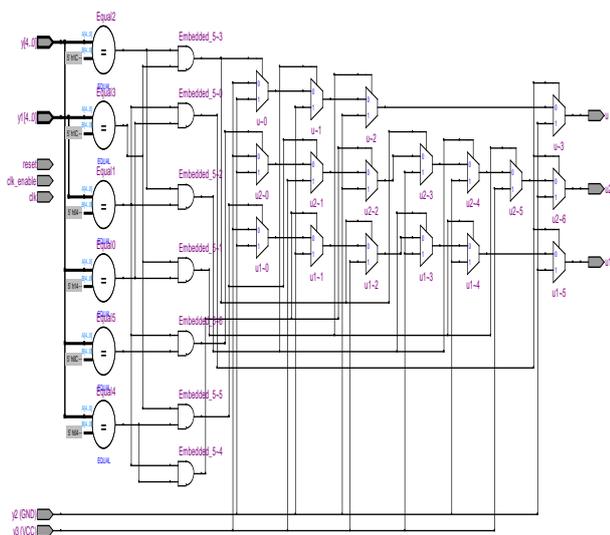


Figure (8) The implemented embedded5 circuit of 8QAM (using for bassband demodulated signal)

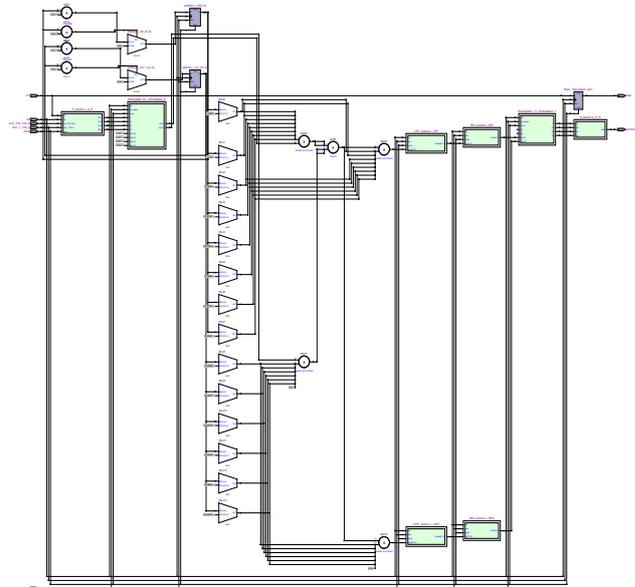


Figure (11) The implementation of the 16QAM technique

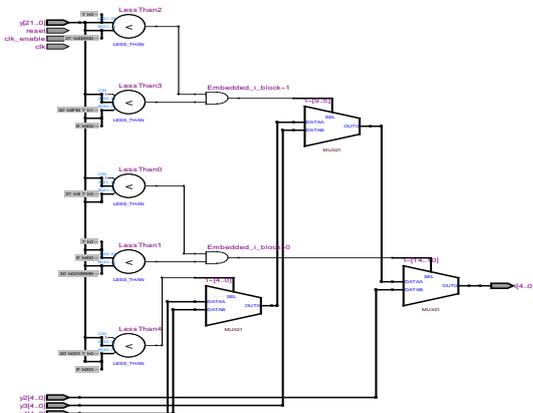


Figure (9) The implemented decision circuit for the I-Channel of 8QAM

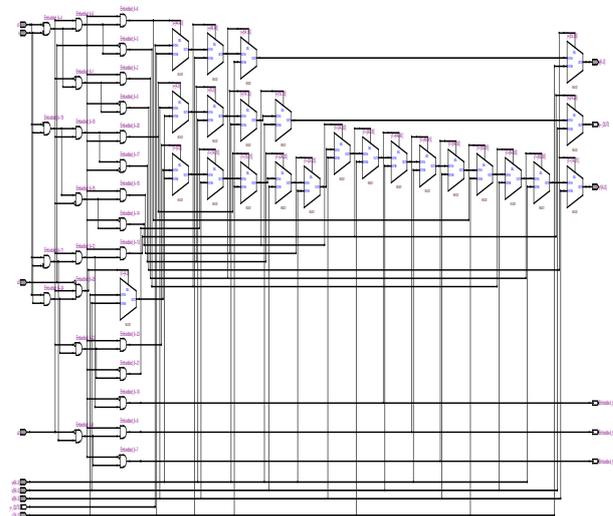


Figure (12) The implemented embedded6 circuit of 16QAM (using for bassband modulated signal)

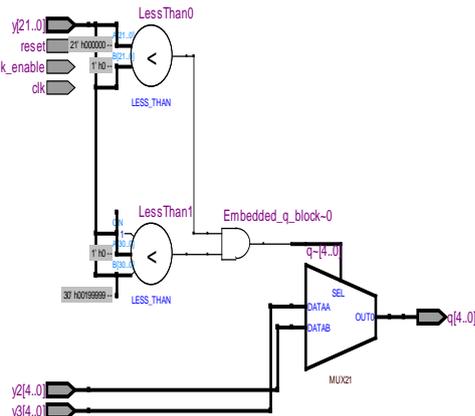


Figure (10) The implemented decision circuit for the Q-Channel of 8QAM

The same procedure, which is mentioned above can be used for implementation 16QAM, 32QAM and 64QAM. Figure (11) shows the implementation of the 16QAM System technique. Figure (12) shows the implemented embedded6 circuit (used to bassband modulated signal). Figure (13) shows the implemented embedded7 circuit (used to bassband demodulated signal). Figure (14) and Figure (15) show the implemented decision circuits for I&Q channels respectively.

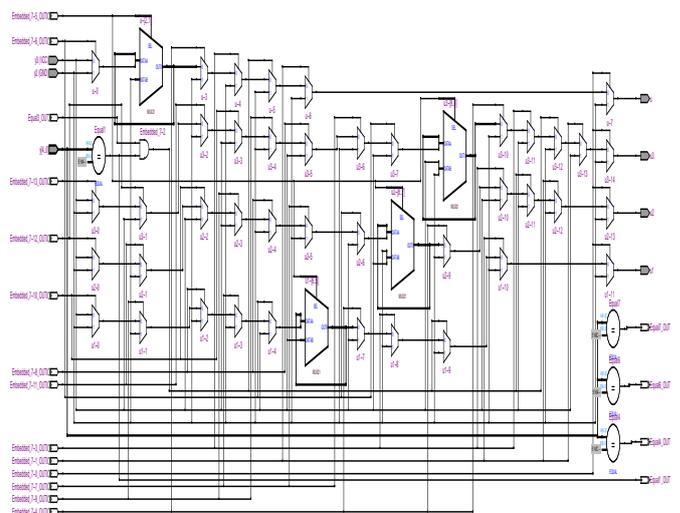


Figure (13) The implemented embedded7 circuit of 16QAM (using for bassband demodulated signal)

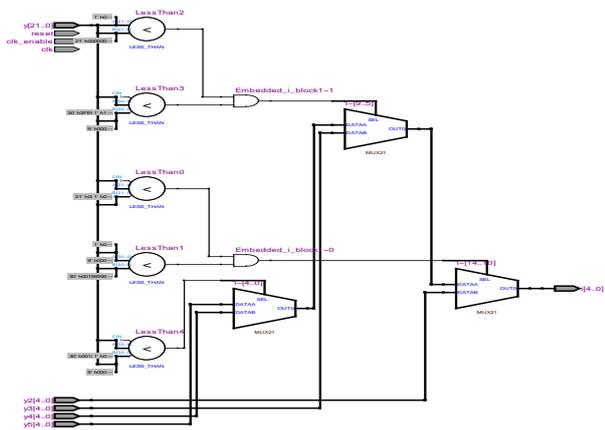


Figure (14) The implemented decision circuit for the I-Channel of 16QAM

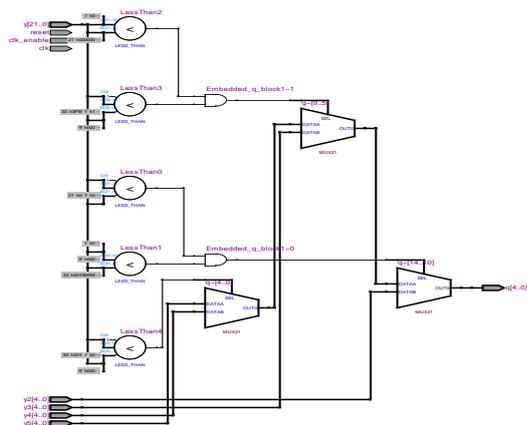


Figure (15) The implemented decision circuit for the Q-Channel of 16QAM

Figure (16) shows the implementation of the 32QAM System technique Figure (17) shows the implemented embedded8 circuit (used to bassband modulated signal). Figure (18) shows the implemented embedded9 circuit (used to bassband demodulated signal). Figure (19) and Figure (20) show the implemented decision circuits for I&Q channels respectively.

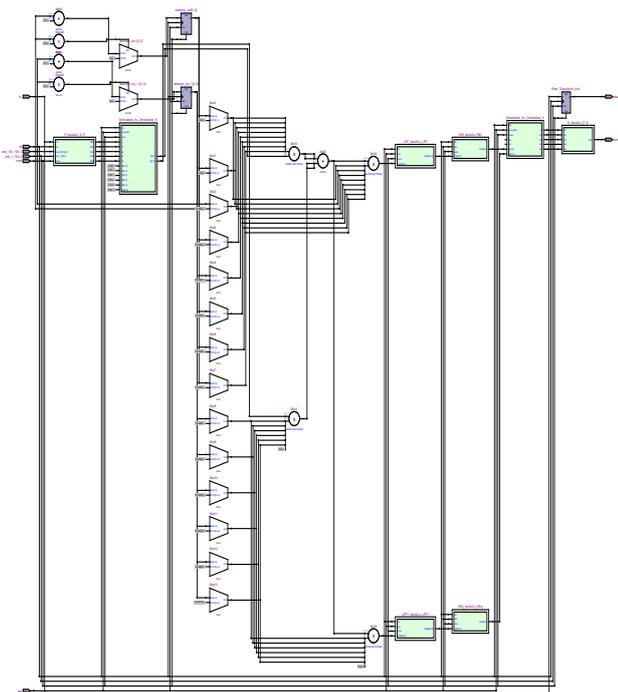


Figure (16) The implementation of the 32QAM technique

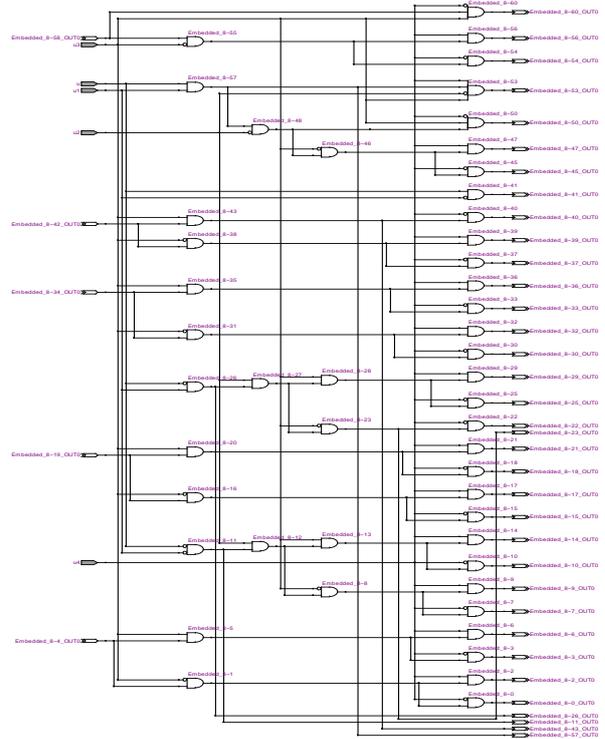


Figure (17) The implemented embedded8 circuit of 32QAM (using for bassband modulated signal)

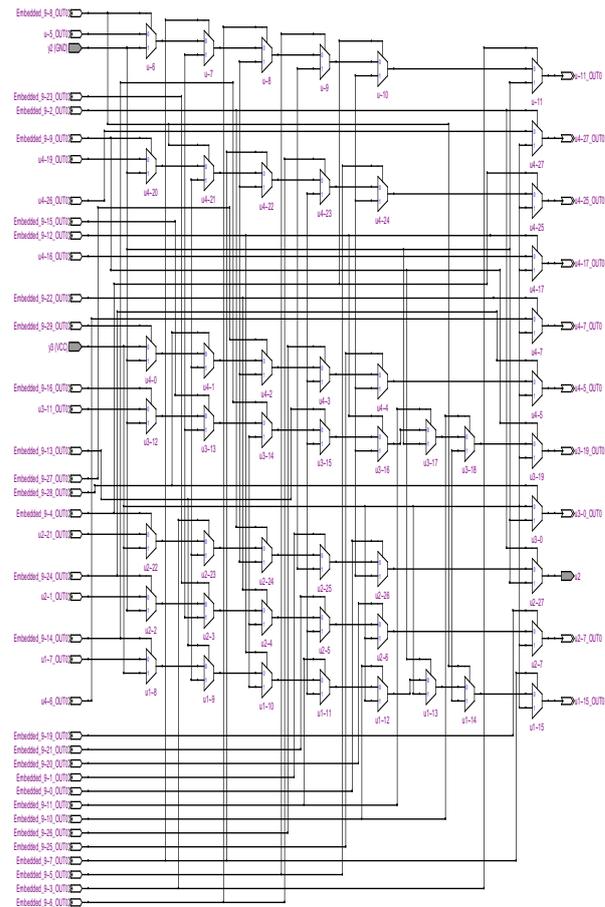


Figure (18) The implemented embedded9 circuit of 32QAM (using for bassband demodulated signal)

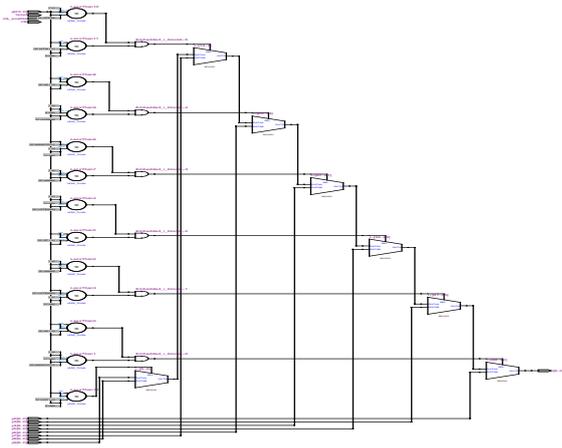


Figure (19) The implemented decision circuit for the I-Channel of 32QAM

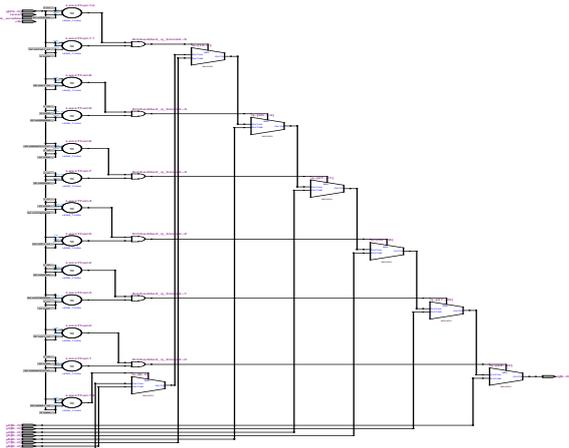


Figure (20) The implemented decision circuit for the Q-Channel of 32QAM

Figure (21) shows the implementation of the 64QAM System technique Figure (22) shows the implemented embedded10 circuit (used to bassband modulated signal). Figure (23) shows the implemented embedded11 circuit (used to bassband demodulated signal). Figure (24) and Figure (25) show the implemented decision circuits for I&Q channels respectively. Figure (26) shows the implemented digital low pass filter used for all modems.

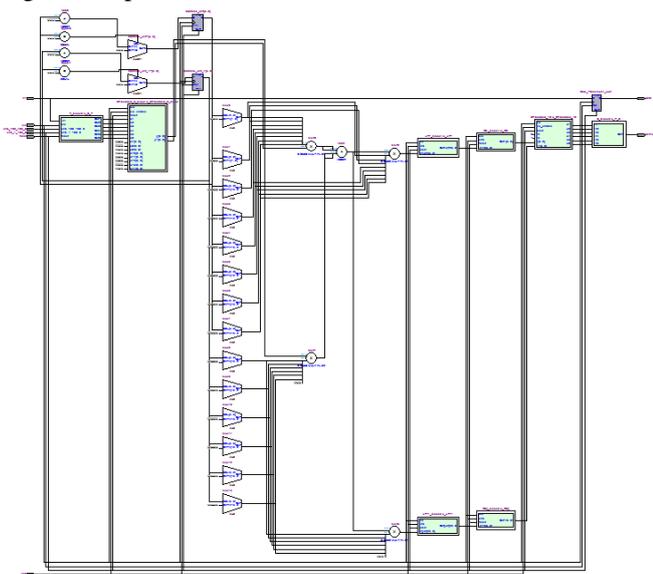


Figure (21) The implementation of the 64QAM technique

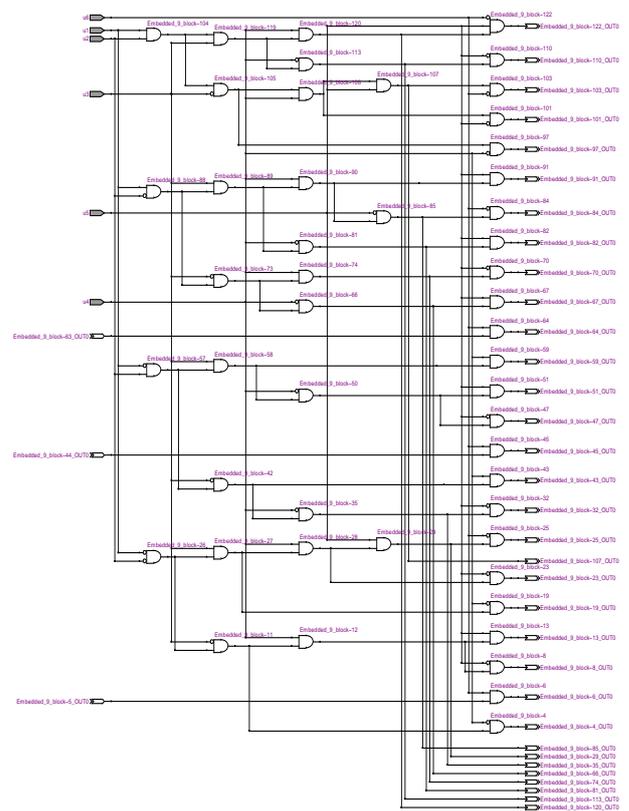


Figure (22) The implemented embedded10 circuit of 64QAM (using for bassband modulated signal)

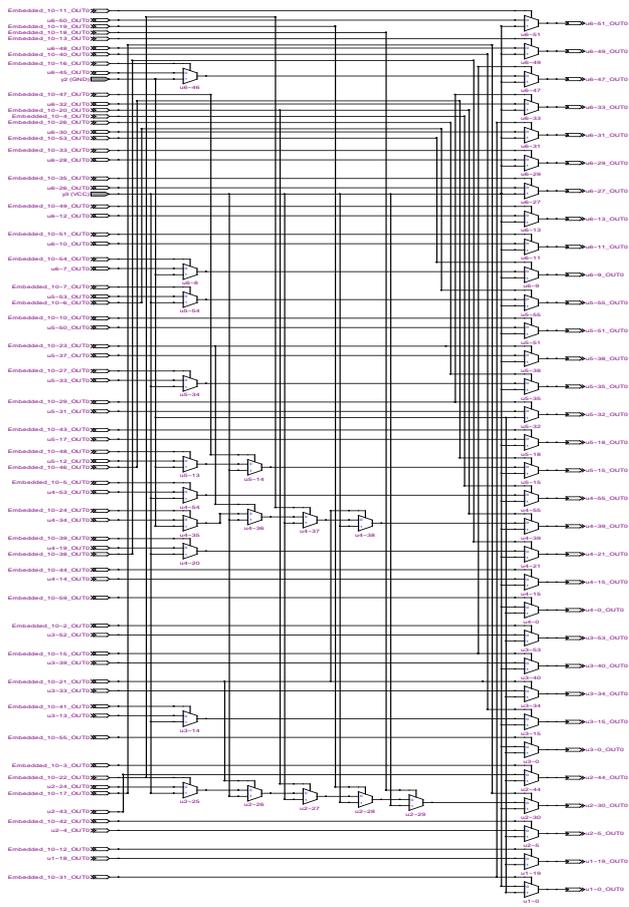


Figure (23) The implemented embedded11 circuit of 64QAM (using for bassband demodulated signal)

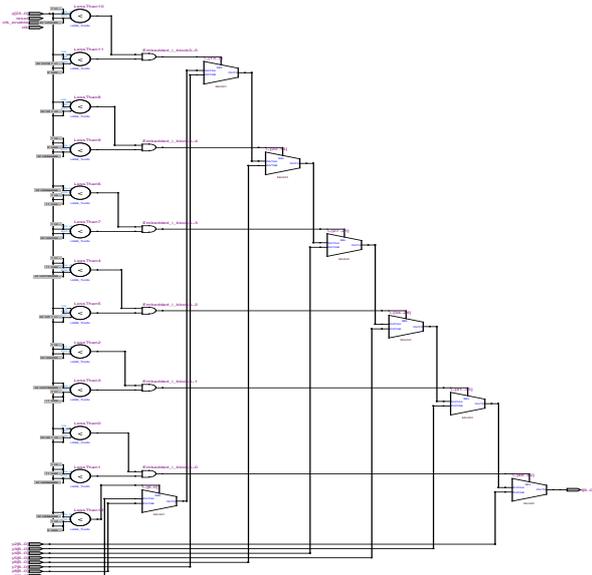


Figure (24) implemented decision circuit for the I-Channel of 64QAM

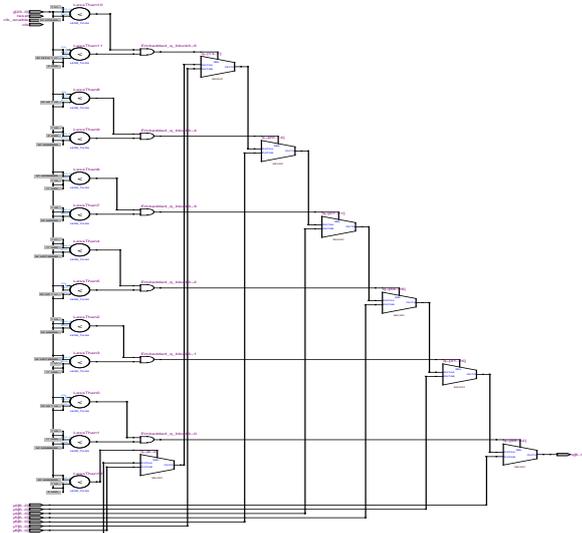


Figure (25) implemented decision circuit for the Q-Channel of 64QAM

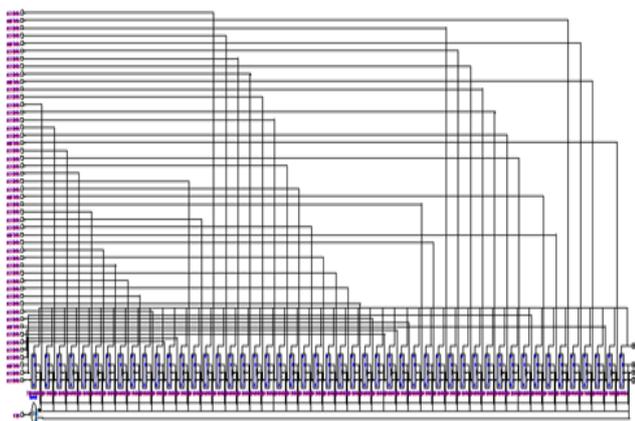


Figure (26) Implemented Digital Low Pass Filter (used for all modems)

VIII. GENERATION OF SIGNALS FOR 8QAM MODEM

Figure (27) shows the input data for I-Channel of the 8QAM modem. Figure (28) shows the sine carrier used for IF stage. Figure (29) shows the baseband signal of the 8QAM modem modulated signal of sine carrier. Figure (30) shows the input data for Q-Channel of the 8QAM modem. Figure (31) shows the cosine carrier used for IF stage.

Figure (32) shows the baseband signal of the 8QAM modem modulated signal of cosine carrier. Figure (33) shows the 8QAM bandpass transmitted signal. Figure (34) shows the received signal (after multiplied by a carrier) before filter for I-Channel. Figure (35) shows the received signal after low pass filter for I-Channel. Figure (36) shows the signal after decision circuit for I-Channel. Figure (37) shows the received signal (after multiplied by a carrier) before filter for Q-Channel. Figure (38) shows the received signal after low pass filter for Q-Channel. Figure (39) shows the signal after decision circuit for Q-Channel. Figure (40) shows the transmitted data and the final output of the QPSK modem. The same procedure was used to generate signals for 16QAM, 32QAM and 64QAM modems. However, their figures are not shown here due to limit the number of pages.

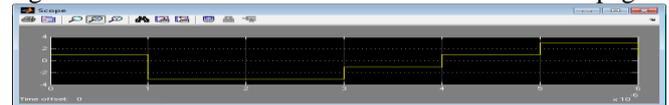


Figure (27) Input data for I-Channel of the 8QAM modem

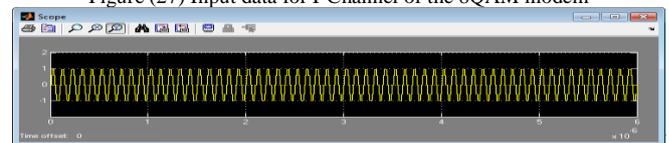


Figure (28) Sin carrier signal of the 8QAM modem

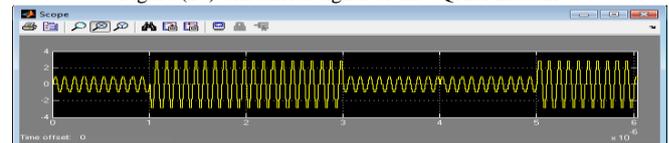


Figure (29) The modulated signal of I-Channel for 8QAM modem

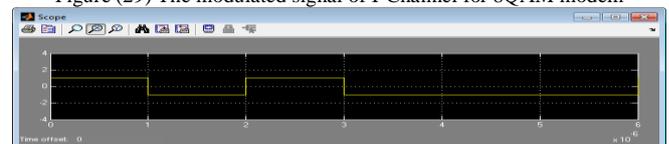


Figure (30) Input data for Q-Channel of the 8QAM modem

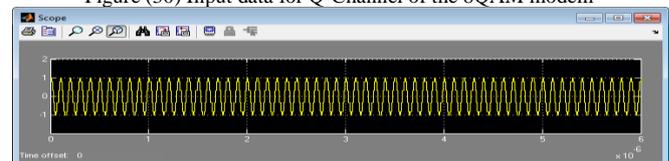


Figure (31) Cos carrier signal of the 8QAM modem

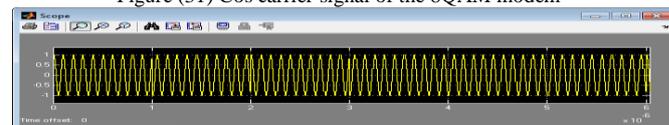


Figure (32) The modulated signal of Q-Channel for 8QAM modem

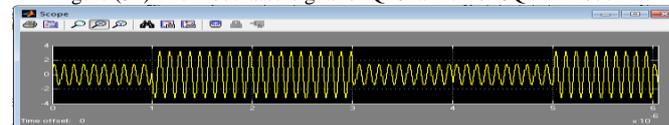


Figure (33) 8QAM bandpass modulated signal

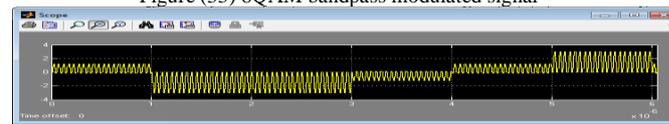


Figure (34) Received 8QAM signal before filter for I-Channel

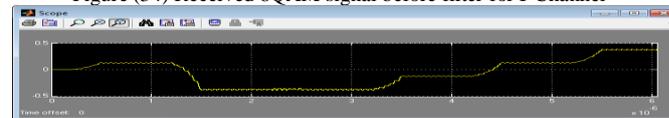


Figure (35) Received 8QAM signal after filter for I-Channel

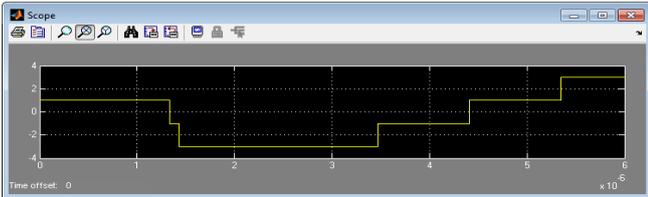


Figure (36) Received 8QAM signal after the decision circuit for I-Channel

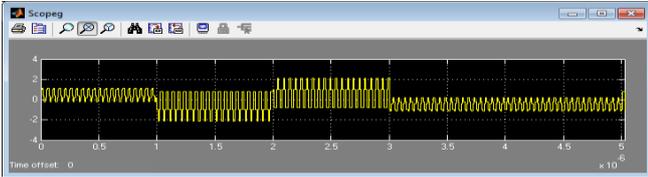


Figure (37) Received 8QAM signal before filter for Q-Channel

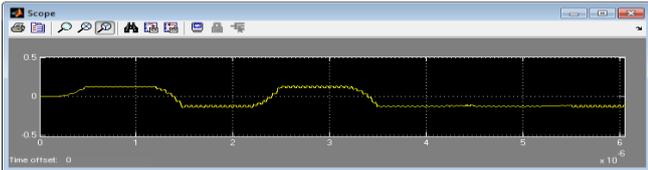


Figure (38) Received 8QAM signal after filter for Q-Channel



Figure (39) Received 8QAM signal after the decision circuit for Q-Channel

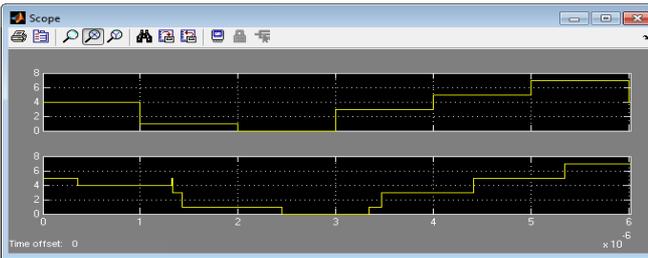


Figure (40): (a) Input data (b) output received data

IX. SIMULATION RESULTS BASED ON MODELSIM

The simulation results obtained by using ModelSim-Altera 6.4a (Quartus II 9.0) represent the second step in the simulation process. Figure (41) shows the input data signal, bandpass modulated signal of the 8QAM modem, demodulated data signal and related control signals for the 8QAM modem. Figure (42) shows more details on the 8QAM bandpass modulated signal that are transmitted over the channel. Figure (43) shows the input data signal, bandpass modulated signal of the 16QAM modem, demodulated data signal and related control signals for the 16QAM modem. Figure (44) shows more details on the 16QAM bandpass modulated signal that are transmitted over the channel. Figure (45) shows the input data signal, bandpass modulated signal of the 32QAM modem, demodulated data signal and related control signals for the 32QAM modem. Figure (46) shows more details on the 32QAM bandpass modulated signal that are transmitted over the channel. Figure (47) shows the input data signal, bandpass modulated signal of the 64QAM modem, demodulated data signal and related control signals for the 64QAM modem. Figure (48) shows more details on the 64QAM bandpass modulated signal that are transmitted over the channel.

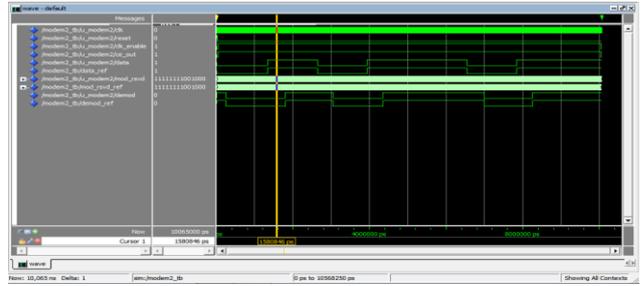


Figure (41) Input data signal, 8QAM bandpass modulated signal, demodulated data signal and related control signals for 8QAM modem

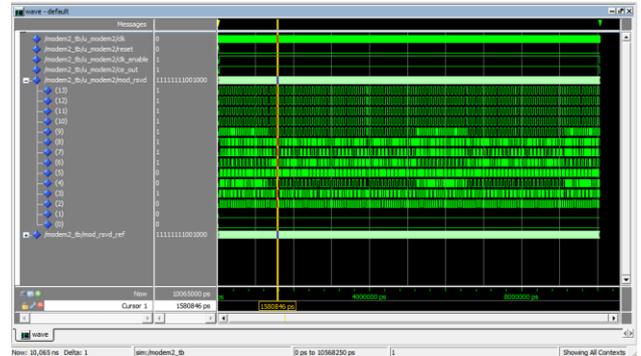


Figure (42) Details on the 8QAM bandpass modulated signal

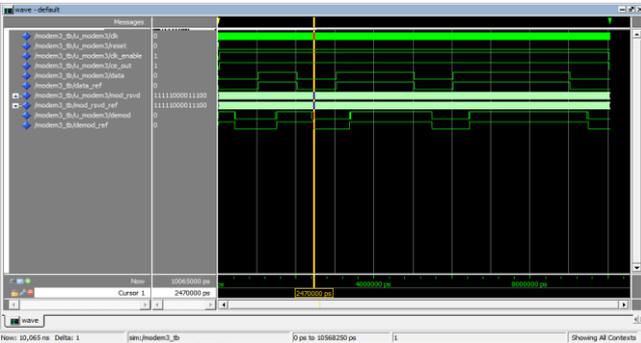


Figure (43) Input data signal, 16QAM bandpass modulated signal, demodulated data signal and related control signals for 16QAM modem

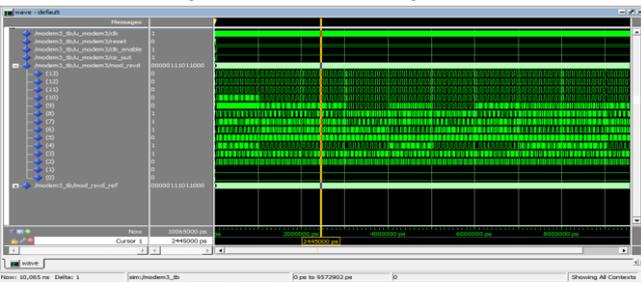


Figure (44) Details on the 16QAM bandpass modulated signal

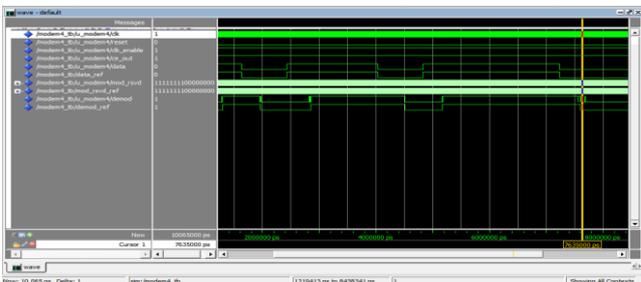


Figure (45) Input data signal, 32QAM bandpass modulated signal, demodulated data signal and related control signals for 32QAM modem

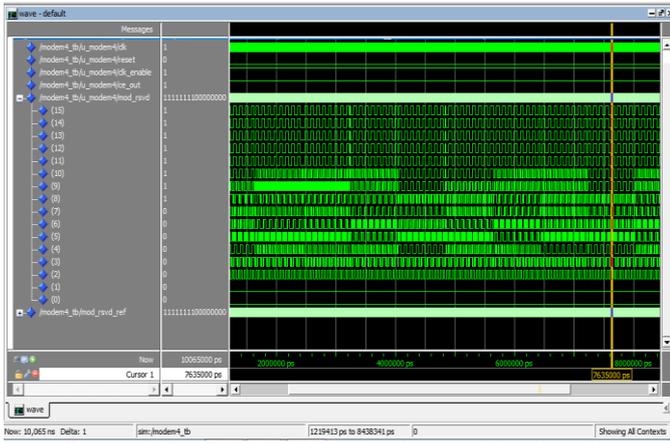


Figure (46) Details on the 32QAM bandpass modulated signal

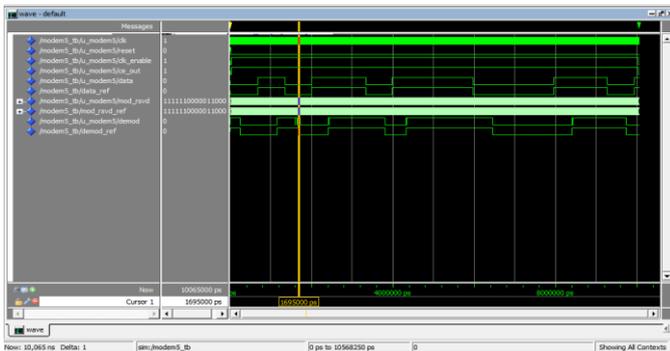


Figure (47) Input data signal, 64QAM bandpass modulated signal, demodulated data signal and related control signals for 64QAM modem

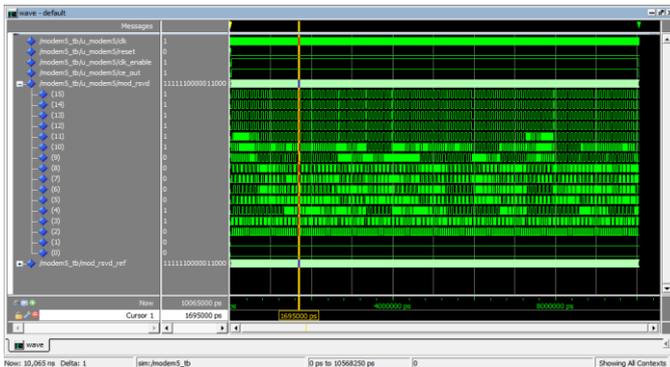


Figure (48) Details on the 64QAM bandpass modulated signal

X. EXPERIMENTAL RESULTS

After compiling the VHDL code by using Quartus II and downloading the bit streams successfully to Cyclone II FPGA family, altera DE2 kit. TTL data from function generator of variable data rate of (1.5Mbps-3Mbps) have been applied as the input to the kit, while the output has been measured by an oscilloscope. Figure (49) shows the input and output data of the 8QAM modem when the control signals are (00) applied to the kit switches (SW0 and SW1) at the input data rate of (1.5Mbps). Figure (50) shows the input and output data of the 16QAM modem when the control signals are (01) applied to the kit switches (SW0 and SW1) at the input data rate of (2Mbps). Figure (51) shows the input and output data of the 32QAM modem when the control signals are (10) applied to the kit switches (SW0 and SW1) at the input data rate of (2.5Mbps). Figure (52) shows the input and output data of the 64QAM modem when the control signals are (11) applied to the kit switches (SW0 and SW1) at the input data rate of (3Mbps).

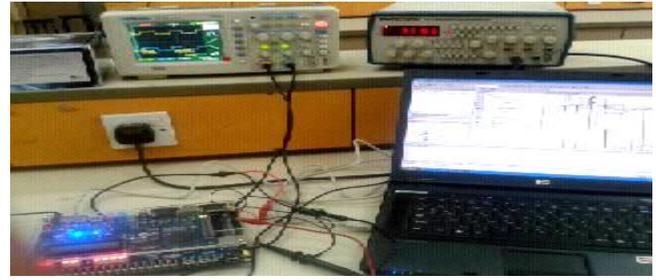


Figure (49) 8QAM modem when control signals are (00)



Figure (50) 16QAM modem when control signals are (01)

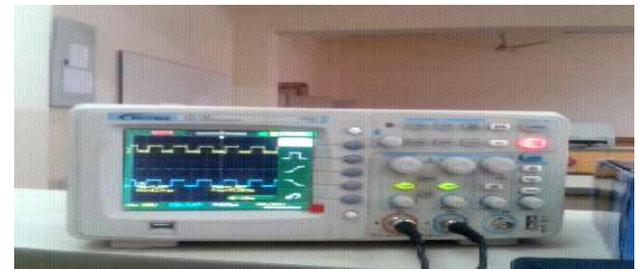


Figure (51) 32QAM modem when control signals are (10)



Figure (52) 64QAM modem when control signals are (11)

XI. CONCLUSIONS

The main important results obtained from this work can be summarized as follows:

1. Software Defined Radio (SDR) has the flexibility to modify the characteristics of a transmitting and receiving radio device, without physically modifying the hardware, due to development in system.
2. FPGA offers flexible solution in IF stage and wideband (WB) modem processing because it provides high speed, high level of integration, low development costs and low power.
3. Simulink HDL Coder proves the capabilities to generate Hardware Description Language (HDL) code to MATLAB model (Simulink and M-file) for complex units of proposed system. The following complex units are designed, implemented and verified.

- a. The optimal FIR filter design with (50) lengths used for all modems.
 - b. Multimode soft decision circuit to determine the regions of the received signal in order to define the final output data. The decision circuit includes 8, 16, 32 and 64 regions.
 - c. Division of input data by the variable factor according to number of bit per symbol. The variable factor is 3,4,5 and 6 and is determined by selectable circuits.
 - d. Symbol mapping (baseband modulators) to convert the input data levels to the level compatible with bandpass modulators of the proposed system.
 - e. Generation bandpass signal for six modems in order to set the IF signal required by SDR systems, As well as the generation of the bandpass signal which has optimal utilized area by FPGA with satisfied the required sampling rate.
4. The combination of MATLAB (Simulink and M-file) and Simulink HDL Coder provides flexible capabilities to analyze, design, simulate, implement and verify. However all these capabilities exist in one system to reduce the time spent on fine tuning to reduce the algorithms and models through rapid prototyping and experimentation and less time on HDL coding.

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