Comparative Study of Delay and Power Dissipation of a Low Power CMOS BPSK Modulator Circuit

Sayani Palit, Madhumita Mukherjee

Abstract-- In this paper we have presented a BPSK modulator using low power CMOS technology. The key design issues in VLSI circuit design are power and delay. Thus in this paper we have focused on LP CMOS with different technologies(16nm, 22nm ,32nm,and 45nm) with the help of TANNER EDA Tool. The value of model parameters are used from Predictive Technology Model(PTM). The T-SPICE simulation results indicate that there is a 59% deduction in Dynamic power For 16nm technology compare to 45nm technology keeping supply voltage constant whereas there is 74.64% reduction in power delay product in 16nm technology compare to 45nm technology.

Index Terms—BPSK, LP CMOS, Power dissipation, PTM

I. INTRODUCTION

Recently the rising demand of high speed transmission data rates of wireless application has the technology development of next generation communication system. The need for higher data rate and lower power is driving current research in the design of a trans receiver for such implants[1].Currently, most modern wireless communication systems adopt direct conversion or low IF receiver architecture which offers many advantages, such as having lower power consumption, Being low cost and using a small sized chip. It has been found that constant-envelop fixed carrier frequency modulation schemes like binary phase-shift-keying (BPSK) are more suitable than amplitude shift keying or frequency shift keying[2]. A constant envelop carrier signal provides stable power transfer at high efficiency. The BPSK modulator is part of the external reader and could easily be implemented using discrete components. Thus BPSK modulator should consume low power and area efficient.

Power reduction in CMOS platforms is essential for any application technology. The trend of CMOS technology improvement contains to be driven by the need to integrate more function within given silicon area, reduce the fabrication cost, increase operating speed, dissipate less power. As the density and operating speed of CMOS chips increase power dissipation has become a critical concern in the design of VLSI circuits, especially in mobile and portable ASIC system. In conventional CMOS circuits, popular approaches to low-power design include the reduction of supply voltage node capacitance and switching activity[3].

With ever increasing level of integrator and the growth of complexity of electronic circuit increasing the demand of portable electronics devices and also dependence on the battery operated devices motivates the VLSI designers to reduce the power dissipation of the VLSI. Circuits so that it can be used for the long time for the given battery supply so that is why reduction of power is the most often used measures of the efficiency of VLSI circuit has come to fore as a primary design goal.

In this paper the simulation of a CMO BPSK is done considering the channel length in the order of 16nm, 22nm, 32nm, 45nm[4]. The results shows that how dissipated power and delay these are two major factors will depends on different design parameters for different channel length. We have also observed the power delay product(PDP),static power of BPSK circuit. Thus using these parameters we can easily analyzed low power CMOS BPSK and their application in the field of VLSI.

The rest of the paper is organized as follows. The section II contains the BPSK modulator circuit. Simulation results and discussion are given in section III and conclusion is presented in section IV.

II. DESCRIPTION OF BPSK MODULATOR CIRCUIT

In BPSK technique, the digital signal is broken up time wise into individual bits (binary digit) thus it is called binary phase shift keying. Mathematical expression for BPSK— A binary phase shift keying (BPSK) signal can be defined by[5] $s(t) = A\ m(t) \cos 2\pi fct \quad 0 < t < T$ ……(1)

Where A is a constant, m(t) is the modulating signal and f_c is the carrier frequency.

Here we have designed Primitive Polynomial; $P(x) =1+x^2+x^3$ in order to generate PN Sequence as a modulating signal for BPSK modulator as this polynomial has the maximum length 7, thus we have to use three cascaded D Flip-Flops in order to generate a PN sequence. To initialize the circuit we have use preset (pre) node in the cascaded D flip-flops as shown in the Fig-1. In this CMOS BPSK modulator circuit a clock pulse is used as a carrier signal. Thus we have connected terminal ‘q1’ which provides PN sequence, modulating signal and the clock (clk) pulse to the input XNOR gate to generate modulated BPSK output waveform as shown in the Fig-1 given below.

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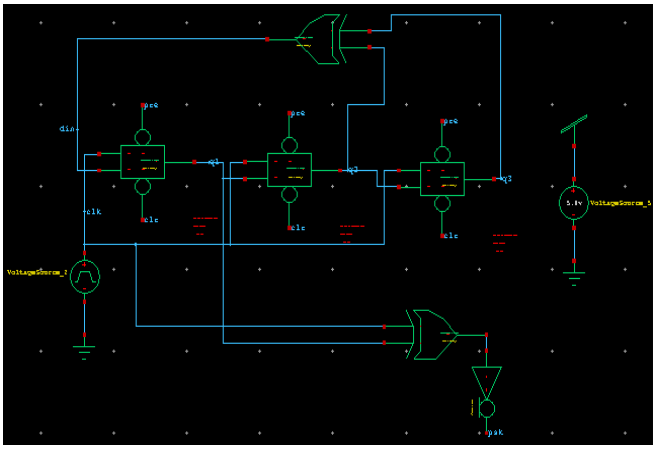


Fig-1: Schematic Diagram Of CMOS BPSK Modulator

signal and the clock (clk) pulse to the input XNOR gate to generate modulated BPSK output waveform as shown in the Fig-1 given below.

III. SIMULATION RESULTS AND DISCUSSION

All simulations are done in TANNER EDA Tool using PTM technology for 16nm, 22nm, 32nm, 45nm. Model parameters are extracted from LP CMOS user manual.
The results clearly shows how delay and power dissipation relate to different design parameters such as supply voltage, width of PMOS and NMOS. In all cases pulse type {PULSE(0 1 0 5n 5n 70n 150n)} input signal is used with rise time(t_r=5ns), fall time(T_f=5ns), initial delay(t_d=0ns), and pulse width(t_{pw}=70ns) and time period(t_{PER}=150ns).We compare our results in 16nm, 22nm, 32nm and 45nm for a low power CMOS. The static power and current of the CMOS BPSK modulator is varying with the supply voltage and aspect ratio. Using symbol generation method we have design the circuit.

A. Simulation Waveform

Transient characteristics of CMOS BPSK modulator is shown in Fig-2.This snapshot is taken from EDA Tanner Tool. Here in this waveform we can clearly see that when PN sequence (Q1, modulating signal) obtains the value '1' then modulated BPSK waveform is similar to the clock(carrier) and when it achieves '0' then the modulated output waveform 180 degree phase shifted of carrier signal.

B. Delay Modeling For Cmos Bpsk

In our circuit we have calculated the propagation delay by calculating the time from the 50% of the rising/falling input to 50% of the falling/rising of the output waveform .

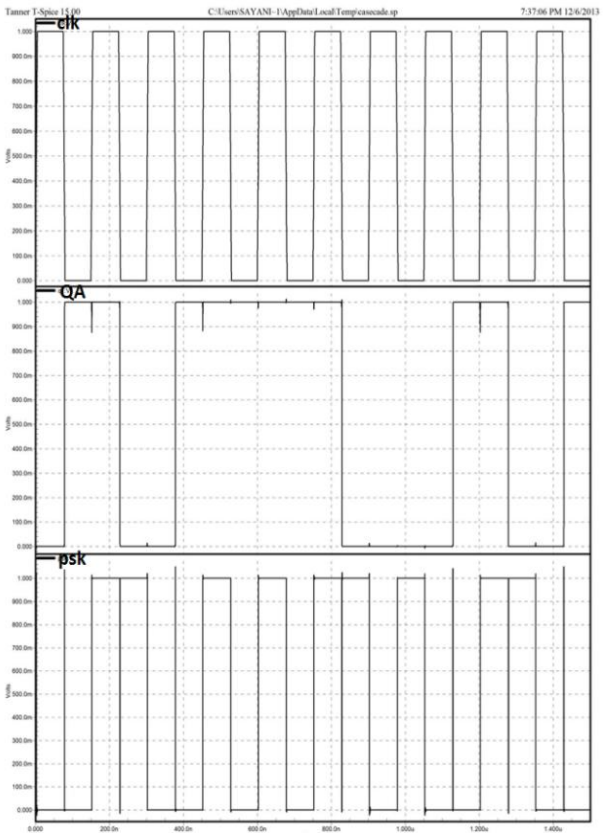


Fig-2:Transient Characteristics of CMOS BPSK

Transient response of CMOS BPSK modulator is shown in Fig-2 i.e. input and output waveform with respect to time in ns .Delay for 0 to 1 transition to Propagate the output is given in equation no(2)[6].

$$t_{pLH}=C_L V_{DD}/\{w/L\mu c_{OX}(V_{DD}-V_T)^2\} \quad \text{.....(2)}$$

Here propagation delay for low to high is similar for high to low propagation delay(t_{pHL}), w is the width of PMOS/NMOS,L is the channel length of PMOS/NMOS,V_{DD} is the Supply Voltage and V_T is the Threshold Voltage. The average propagation delay is given by equation (3)[7]

$$t_p=1/2(t_{pHL}+t_{pLH}) \quad \text{.....(3)}$$

propagation delay has some key dependency parameters such as supply voltage ,channel length of the device, load and parasitic capacitance of CMOS devices. By increasing supply voltage we can reduce propagation delay and make the working circuit faster in switching as shown in the table(2) given below. By reducing the aspect ratio of the device we can reduce the propagation delay. As we know with the increased load capacitance propagation delay is also increased, so to avoid the problem we have varied the aspect ratio of the device keeping the supply voltage constant and negligible load capacitance to obtain the lowest propagation delay as shown in the Fig-4(a,b) .

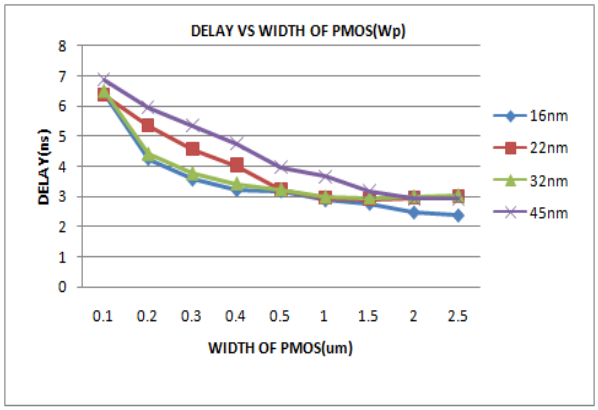


Fig-4(a): Propagation Delay time (tp in ns) vs. Variation of Wp (um) when V_{DD}=1V

Fig-4(a) shows that the propagation Delay is changing with the variation of width of NMOS for 16nm, 22nm,32nm and 45nm.

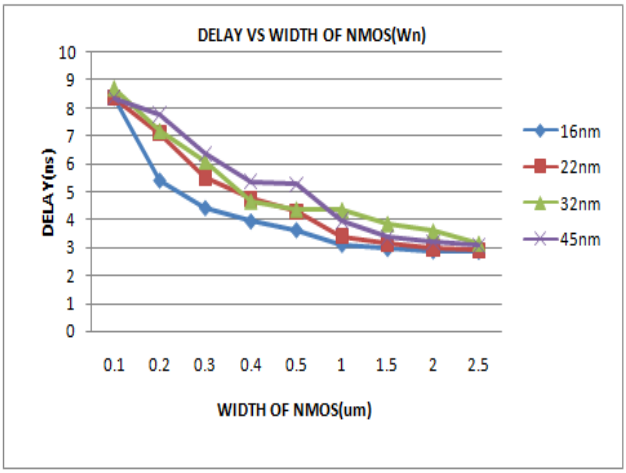


Fig-4(b):Propagation delay time (t_p in ns) vs. Variation of W_n(um) when V_{DD}=1v

Fig-4(a) shows that the propagation Delay is changing with the variation of width of NMOS for 16nm, 22nm,32nm and 45nm.

C. POWER MODELING FOR CMOS BPSK

Two types of power occur in CMOS BPSK modulator circuit, which are given below[8]:

Static Power Dissipation: when circuit is in idle state, no switching takes place but some amount of leakage current flows thus the power dissipation occurs. The main component of leakage current is sub-threshold leakage current (I_{sub}).the table(2) shows the static power of BPSK modulator circuit with respect to the variation of technology and supply voltage[9].

Table-1: Static power of CMOS BPSK modulator varying with supply voltage for different technology. (W_n=2W_p)

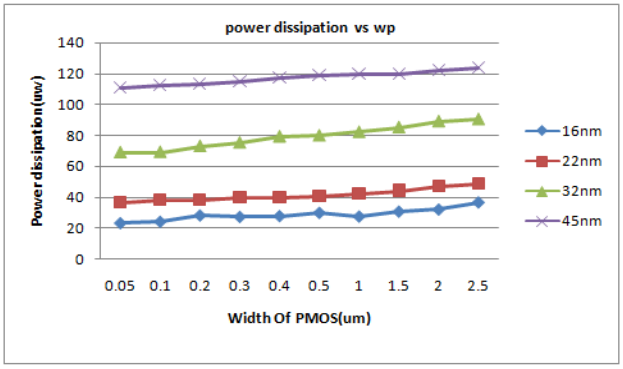
Supply Voltage(v) V_{DD}	Static Power(uw)			
	16nm	22nm	32nm	45nm
1	0.7084	0.1794	0.147	0.1679
1.5	13.97	3.247	1.265	0.5354
2	174.99	56.32	31.76	13.063
2.5	2462	1133	961.33	595.5

BPSK modulator static power is dependent on supply voltage. The table-1 shows the variation of static power with supply voltage for different technology. We assuming Wn=2 Wp.

Dynamic Power Disspation: This type of power dissipation occurs due to the charging and discharging of load and parasitic capacitors .the equation(4) shows the mathematical expression for the dynamic power[7].

$$P_{Dynamic} = \alpha C_L V_{DD}^2 f + \sum_{i=1}^{\infty} \alpha_i C_i V_{DD} (V_T - V_{DD}) \ldots\ldots (4)$$

Where C_L=Load capacitance, V_{DD}=Supply voltage, f=Operating Clock Frequency, α=Switching activity of gate(probability of 0 to 1 switch in a cycle)In this expression the Dynamic power indicates the average dynamic power of a complex gate due to output load capacitance and parasitic capacitance[10]. Here in our working circuit we have only considered the parasitic capacitance of CMOS devices. Table(2) shows the reduction of power dissipation and the power delay product with the dissipation we have varied the width of the CMOS devices keeping the supply voltage constant in different technology as shown in the fig -5(a,b).



Variation of W_p (um) when V_{DD}=1v

Fig-5(a) shows that the power dissipation is changing with variation of width of PMOS for 16nm,22nm,32nm, and 45nm. With the variation of width of PMOS and constant supply voltage power dissipation is increased linearly but after a certain range of width of PMOS changes of power dissipation is very less.

Table2: Delay, Power dissipation and power delay product relate with supply voltage(W_n=2W_p)

V_{DD}	16nm			22nm			32nm			45nm		
	Pd uw	t_p ns	PDP fJ	Pd uw	t_p ns	PDP fJ	Pd uw	t_p ns	PDP fJ	Pd uw	t_p ns	PDP fJ
1	42.22	3.133	132.27	55.34	3.212	177.76	101.22	3.196	323.49	152.54	3.4153	520.83
1.5	132.8	2.227	295.78	143.87	2.388	343.42	266.4	2.3523	626.65	427.75	2.6871	1149.4
2	596.7	2.009	1199.12	363.50	2.214	804.78	518.51	2.328	1207.06	934.07	2.5576	2388.97
2.5	2964	1.989	5895.39	2936.24	2.2001	6459	2912.54	2.225	6479	2503.5	2.545	6578.91

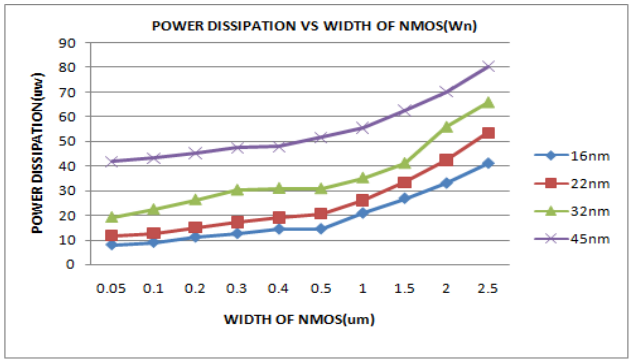


Fig-5(b): Power Dissipation (Pd in uW) vs. Variation of Wn (um) when V_{DD}=1v

Fig-5(b) shows that the power dissipation is changing with variation of width of PMOS for 16nm,22nm, 32nm, and 45nm.The table-1 shows that variation of supply voltage Vdd how propagation delay(t_p) and power dissipation(Pd) and power delay product(PDP=Dynamic power * propagation delay in fJ i.e., 10^-15J) will change for different technology.

IV. CONCLUSION

a) While keeping the supply voltage constant and varying the width of NMOS and PMOS then we find that we have achieved minimum propagation delay and minimum power dissipation in 16nm technology. Thus with increasing the channel length we find that both propagation delay and power dissipation is increased so for 45nm technology we have achieved the maximum delay and power dissipation.

b) While keeping the supply voltage constant and varying the width of NMOS and PMOS then we find that we have achieved minimum propagation delay and minimum power dissipation in 16nm technology. Thus with increasing the channel length we find that bothpropagation delay and power dissipation is increased so for 45nm technology we have achieved the maximum delay and power dissipation.

c) While varying the supply voltage we find the static power for 16nm technology is maximum in comparison to other three technologies we have discussed. Thus with the increasing channel length static power is decreased so for 45nm technology the static power is minimum among these four technology.

d) Power dissipation will decreased by decreasing supply voltage (i.e. Pd is proportional to the square of the Vdd).. Thus from table-2 keeping the width of the PMOS twice than NMOS and find that at maximum supply(V_{DD}) voltage we are getting the maximum power dissipation whereas at minimum supply voltage(V_{DD}) we are getting the lowest power dissipation for all the four technologies we have discussed.

e) As the propagation delay is inversely proportional to supply voltage thus from the experimental result reveals that at lowest supply voltage we are getting the maximum propagation delay whereas minimum propagation delay obtained from highest supply voltage for all four technologies as shown in the table-2.

f) Table-2 reveals that power delay product is increased with the increased technology with the variation of supply voltage and keeping the width of the PMOS twice than the width of NMOS.

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