An Area Efficient Low Power High Speed Pulse Triggered Flip Flop Using Pass Transistor

G.Sai Manoj, T.Sreevatsav, V.Vidya Priyanka, S.V.K.S. Prasad, P.Rajesh

Abstract: ***The performance of flip-flop is an important element to determine the efficiency of the whole synchronous circuit. This paper presents an efficient explicit pulsed static single edge triggered flip flop with an improved performance and overcomes the drawbacks of the implicit type pulsed flip flops. The proposed flip flop is having a structure of explicit pulse-triggered with a modified true single phase clock latch based on signal feed through scheme. The proposed flip-flop is compared with existing explicit pulsed single edge triggered flip-flops in terms of power, speed and area. Simulation results based on PTM 90nm CMOS technology reveal that the proposed design features the best power, area and delay performance in several FF designs under comparison.***

Index Terms*: *Explicit, Edge-Triggered, Feed through, Latch, Synchronous

I. INTRODUCTION

Flip-Flop (FF) is basically used as a memory elements in Digital circuits like Microprocessors. In the present scenario, power consumption is a major challenge in Digital design. FF is divided into two stages, one stage is the clock system and the other is a latch that which stores data. In a conventional FF, Clock system consumes 50% of the total power which is due to the fact that the dynamic power in a MOS circuit is directly proportional to the switching activity [1], [2]. To overcome this problem a Pulse-triggered Flip-Flop (P-FF) is introduced because a single latch is better than conventional master slave FF and transmission Gate (TG). P-FF divides into two stages [3]. First one is a Pulse-Generator (PG) for signal and other is a Latch for storage of data. Triggering is classified into two types, they are narrow pulse and wide pulse. If it is narrow pulse, then it is an Edge-triggered FF. Depending on the method of pulse generation, P-FF designs can be classified as implicit or explicit [4]. In an implicit-type P-FF, the Pulse generator is a built-in logic of the latch design, and no explicit pulse signals are generated. In an explicit-type P-FF, the designs of pulse generator and latch are separate. Implicit pulse generation is often considered to be more power efficient than explicit pulse generation. However, they suffer from a longer discharging path, which leads to inferior timing characteristics [7]. Explicit pulse generation, on the contrary, incurs more power consumption but the logic separation from the latch design gives the FF design a unique speed advantage.

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Its power consumption and the circuit complexity can be effectively reduced if one pulse generator is shares a group of FFs (e.g., an n-bit register). The rest of the paper is organized as follows. Section II presents the Conventional and proposed D Flip Flop designs with their functionality. Section III gives the Simulated waveforms and performance comparison of Explicit type Flip-Flops. Finally, conclusions are drawn in section IV

II. EXPLICIT-TYPE P-FF DESIGN WITH SIGNAL FEED-THROUGH SCHEME

A. Conventional Explicit type P-FF Designs

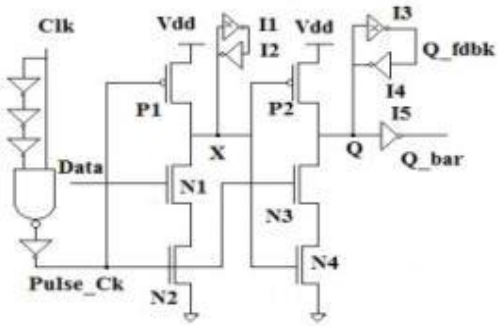

Fig-1: ep-DCO

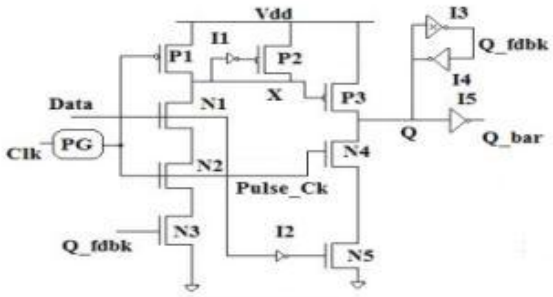

Fig-2: CDFF

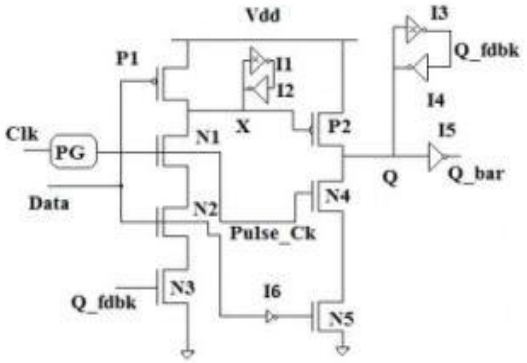

Fig-3: SCDFF

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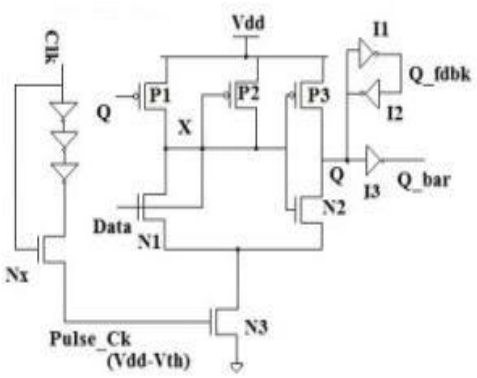

Fig-4: MHLFF

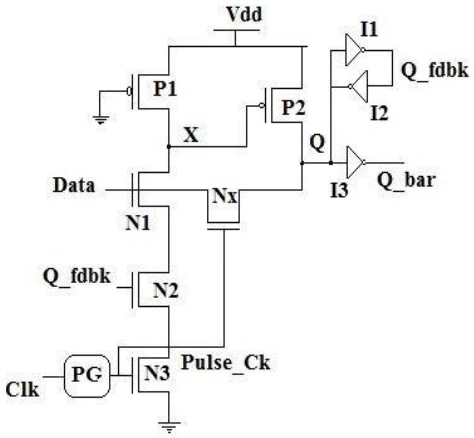

Fig-5: Proposed STSFF

Some conventional explicit-type P-FF designs, which are used as the reference designs in later performance comparisons, are first reviewed. Fig.1 shows data-close-to-output (ep-DCO) FF Design. It contains a PG of a three inverters connected to a NAND gate and a semi dynamic TSPC structure latch design [10]. Back-to-Back end connected inverters as Keeper Logic or Keeper Device. In this P-FF Design, Inverters I1 and I2 which hold internal node X valve and I3, I4 are used to latch data. In presence of static input '1', the internal node X is discharged on every rising edge of pulse signal and gives large switching power dissipation. To overcome this problem a Conditional Discharge FF (CDFF) design is introduced in Fig.2 and extra nMOS is used to feed back the signal Q-fdbk to the input stage so that no discharge occurs at static input data '1' and circuit is further simplified by replacing keeper logic at internal node X with a inverter plus pull-up pMOS transistor only [8]. Fig.3 shows almost similar to CDFF but with changed position of static latch i.e., Data and PG are interchanged their position and node X having keeper logic as two back-to back end inverters. It will be a long Data-to-Q delay. To overcome this delay a Modified Hybrid Latch FF (MHLFF) in Fig.4 which is also a static latch is discussed. The Keeper logic at node X is removed. MHLFF Design having two drawbacks (i) Node X is predischarged, a prolonged 0 to1 delay is expected. (ii) Node X is crosses the voltage level and its valve may drift extra dc power.

B. Proposed STSFF Design

Observing previous Four Flip-Flops, they required same time for 0 to 1 or 1 to 0 data transitions. Fig. 2 is unique from previous four circuits for improving the data transition. STSFF is differentiated by mainly three changes from the previous existing P-FF's. (i) Weak pMOS gate terminal connected to ground which rises a pseudo-nMOS logic style. (ii)A pass transistor controlled by pulse clock and also connected with a data, which makes transition faster. (iii) Pull down nMOS transition is removed from second stage of latch. Total four transistors has been removed from the keeper device and two nMOS transistor are removed which will reduces the delay and improving the speed. Pass transistor provide driving current to node Q during 0 to 1 transition and discharging node Q during 1 to 0 transition.

C. Working Principle of STSFF

In Presence of clock Pulse and no data is present, then the output node Q will stay at same level and also provides driving effect by passing current through transistor Nx. If input data is inverted and output feed is inverted, then pull-down transistor is off at node X. If data changes from 0 to 1, then node X discharges and turns on the pull down transistor which switches Q to high value results to reduces the delay by greater extent. Here all circuits are PG are single edge triggered Flip-Flop. Proposed STSFF can may PG is replaced by dual edge triggered. In, Dual Edge the operation will be occurs at both rising and falling edge.

III. SIMULATION RESULTS

The Schematics of various explicit type flip flops are drawn by using S-Edit in Tanner Tools. To compare the performances of the proposed comparator with the previous works, each circuit was designed using 90nm technology with V_{DD}=1V, f_{CLK}=500MHz and Temp=27^0C, and simulated with HSPICE. The Avanwaves for the flip flops are shown below.

A. Simulation waveforms

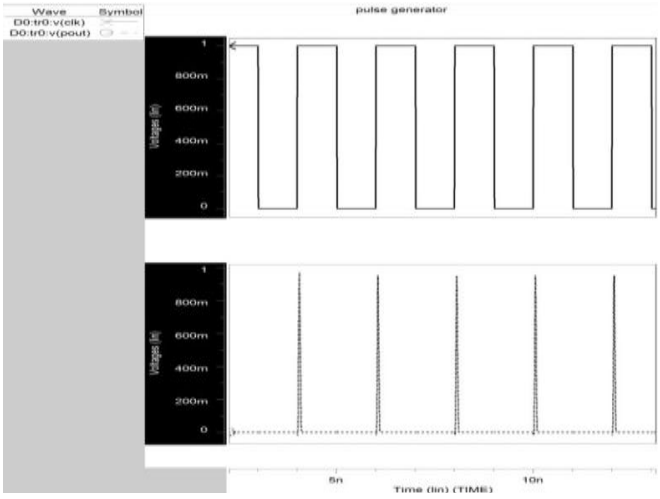

Fig-6: Pulse Generator Output

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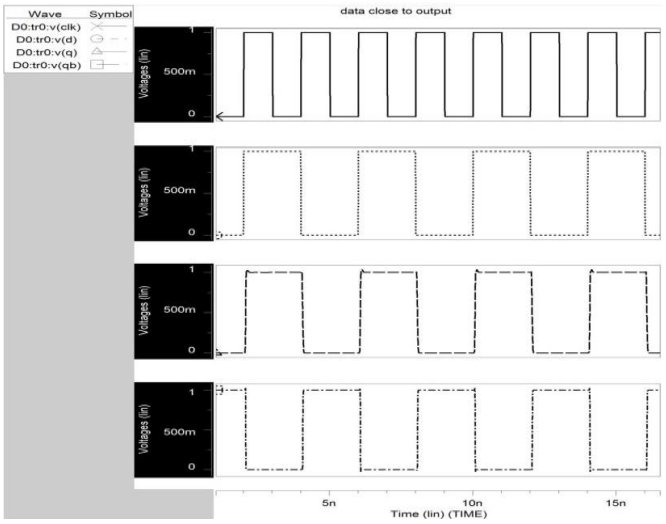

Fig-7: Simulated waveform of ep-DCO

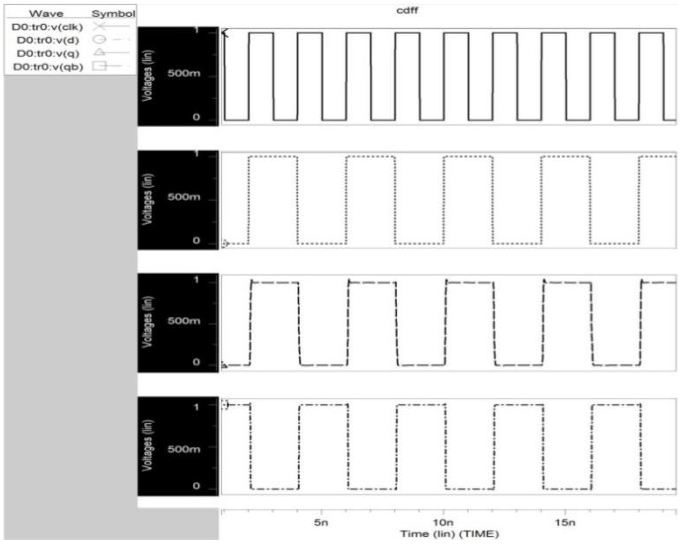

Fig-8: Simulated waveform of CDFF

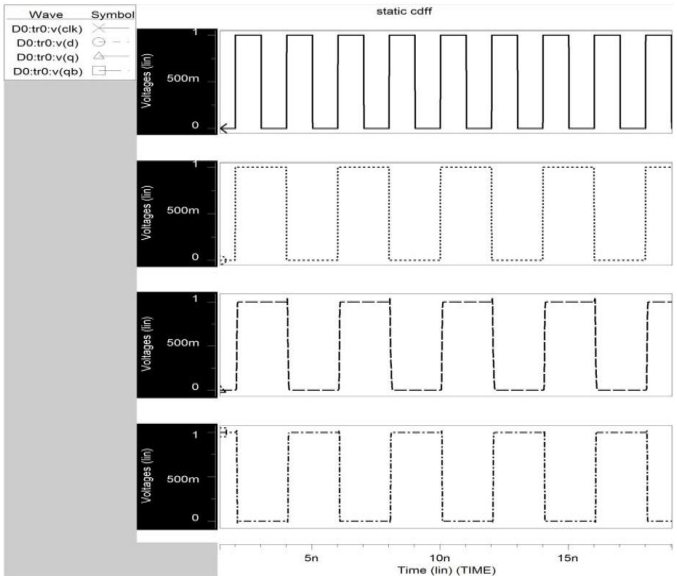

Fig-9: Simulated waveform of SCDFF

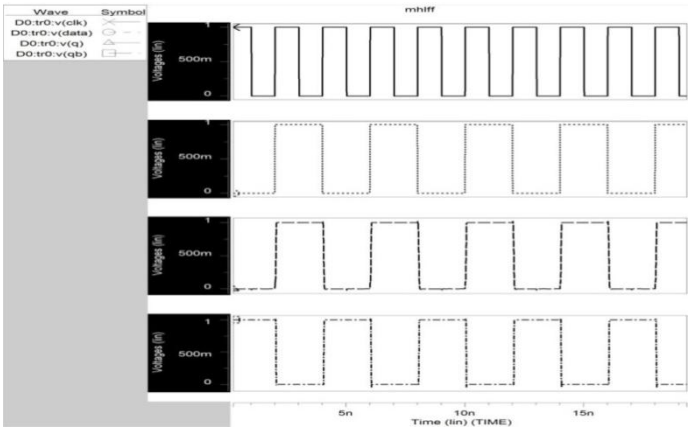

Fig-10: Simulated waveform of MHLFF

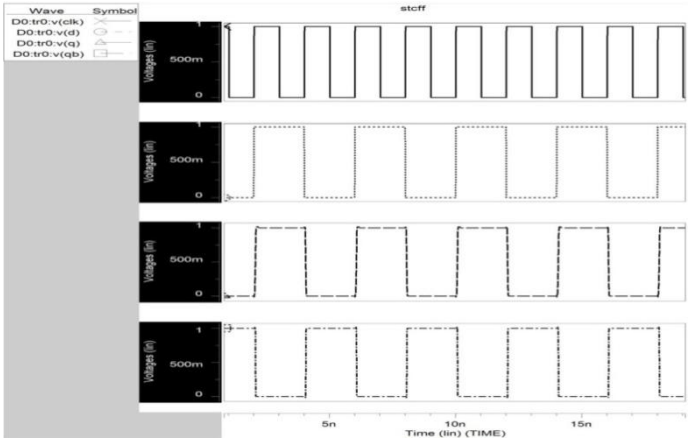

Fig-11: Simulated waveform of MHLFF

B. Performance Comparison

I. Power, Delay and Width Comparison

Flip Flop Type	∑Width(µm)	Delay(ps)	Power(µw)
ep-DCO	11.8	65	16
CDFF	13.4	65	15.7
SCDFF	14.6	59	15.4
MHLFF	11.9	37	18.3
STSFF (Proposed)	9.82	56	13.5

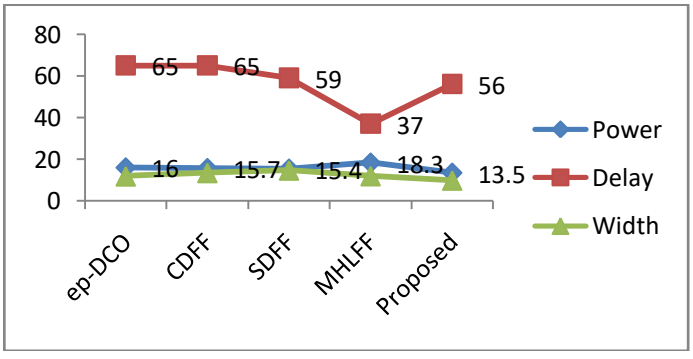

Chart-1: Power, Delay and Width Graphs

IV. CONCLUSION

In this paper, a novel low-power pulse-triggered FF is designed by employing two new design measures. The first one successfully reduces the number of transistors stacked along the discharging path by incorporating a PTL-based AND logic. The second one supports conditional enhancement to the height and width of the discharging pulse so that the size of the transistors in the pulse generation circuit can be kept minimum. Simulation results indicate that the proposed design achieves low power and high speed with less area when compared with conventional flip flops.

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