A High Efficiency DC/DC Boost Converter for Photovoltaic Applications

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Abstract— In this paper, a non isolated interleaved, dc/dc boost converter with a high efficiency is proposed for using in photovoltaic system applications. For realizing zero voltage soft switching (ZVS), two active clamp circuits are used for each phases of the boost converter. By utilizing a voltage doubler configuration at the converter's output terminal and connecting the secondary side of coupled inductors in series, high conversion ration can be achieved. The capacitor is also connected in series with output capacitors to transfer leakage energy to the output. Interleaved structure is used in input side to minimize current ripple and reduce magnetic component. So, the converter not only operates with a higher voltage gain, but also is able to operate more efficiently and can be used in photovoltaic (PV) applications.

Keywords-high voltage gain; interleaved DC-DC boost converter; photovoltaic system; soft switching performance.

I. INTRODUCTION

Chiefly, utilizing high performance dc-dc boost converters is an essential factor in renewable energy sources in high power applications. High efficiency, high voltage gain and being non-isolated are the main features for renewable energies applications [1]. Ideally, a boost converter can reach a very high voltage gain with an unlimited duty cycle, however the turn off period of switches will be small when the duty cycle gets increased. The ripples in the current waveform corresponding to power devices get increased and as a result the power losses increase. Furthermore, the voltage stresses across for both switch and diode are identical to the output voltage [2]. The interleaved structure can be considered as a feasible solution to enhance the performance, mitigate ripples in the current, reduce the size of the passive components and also accelerate the transient response [3-4]. The coupled inductor is utilized to reduce not only the duty ratio but also the voltage stress across the switches. Therefore, for applications for which a high voltage gain is needed, the boost converter with the coupled inductor can be more efficient compared to the conventional design [5]. Different active and passive soft switching interleaved step-up converters in which coupled inductor is utilized are proposed for loss reduction purposes. [6-8].

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However, most of them are considered for the Power Factor Correction (PFC) applications and not an appropriate option for PV systems for which a DC-DC boost converter with a high step-up gain is required.

Some interleaved converters are proposed by adding capacitor cells to the typical interleaved boost converter [9-10]. However, a considerable number of capacitors are required to reach a high voltage gain that increases the complexity in the converter. Different types of interleaved converters with coupled inductors are well investigated in [11-13], which can reach high step-up gain by an appropriate topology. Unfortunately, the maximum numbers of interleaved phases are only two in these converters and cannot be designed for any number of phases. Also, the voltage stress across the diode in the output is greater than the output voltage.

In this paper, an efficient interleaved converter is proposed for PV system applications. The interleaved structure in input side and cascaded configuration in output side is utilized therefore, there would not be any problem with a high amount of current and voltage in the input and output. By utilizing the active clamp design, both the clamp and main switches work in the zero voltage soft switching condition. A snubber capacitor in series with output capacitors is inserted to recycle the leakage energy. So, switching losses are reduced significantly. When a coupled inductor is utilized in fly-back condition the other coupled inductor operates in forwarding condition to transfer energy to output side, due to interleaved control. The proposed topology and operational stages are discussed in section II. In the third section of this paper, the design guidelines of the converter are given. In section IV the simulation result and waveforms are illustrated.

II. PROPOSED CONVERTER TOPOLOGY

The topology of the proposed converter is shown in Fig. 1. The main switches S_1 and S_2 work in the interleaved control. The active clamp circuits are composed of auxiliary switches S_{C1} and S_{C2}, and clamp capacitors C_{C1} and C_{C2}, which are utilized to recycle the leakage energy and suppress the turn-off spike voltage on the main switches, and realize zero voltage soft switching. There are two coupled inductors, which L_{1a} and L_{2a} with n_1 turns which have been coupled with their corresponding inductors L_{1b} and L_{2b} with n_2 turns. The L_{m1} and L_{m2} are the magnetizing inductors, and L_{k1} and L_{k2} are the leakage inductances of coupled inductors. N represents the turn ratio n_2/n_1. The couples reference are marked by "*" and "•". The C_{o1}, C_{o2} and C_{o3} are the output capacitors and D_{o1}, D_{o2}, D_{o3} and D_{o4} are the output diodes. Moreover, the capacitor C_{o3} works as snubber capacitor, to recycles the leakage energy in the coupled inductor. There are 16 main stages in one switching period. Because of the

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symmetrical structure of the converter, only half of 16 stages are considered. The steady state profiles are depicted in Fig. 2. In Fig.3 corresponding circuit of each stage is illustrated.

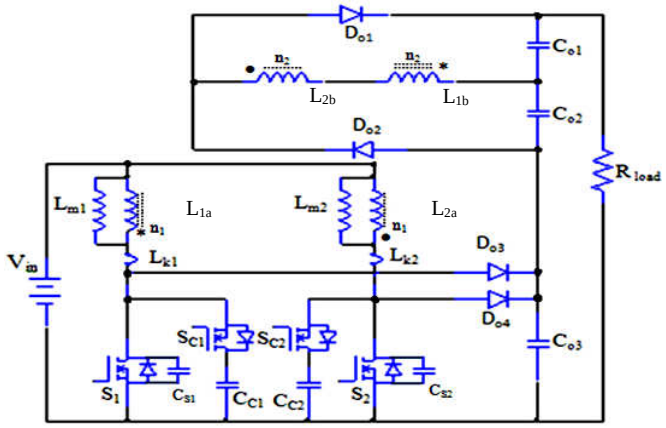

Figure 1. proposed ZVT boost converter.

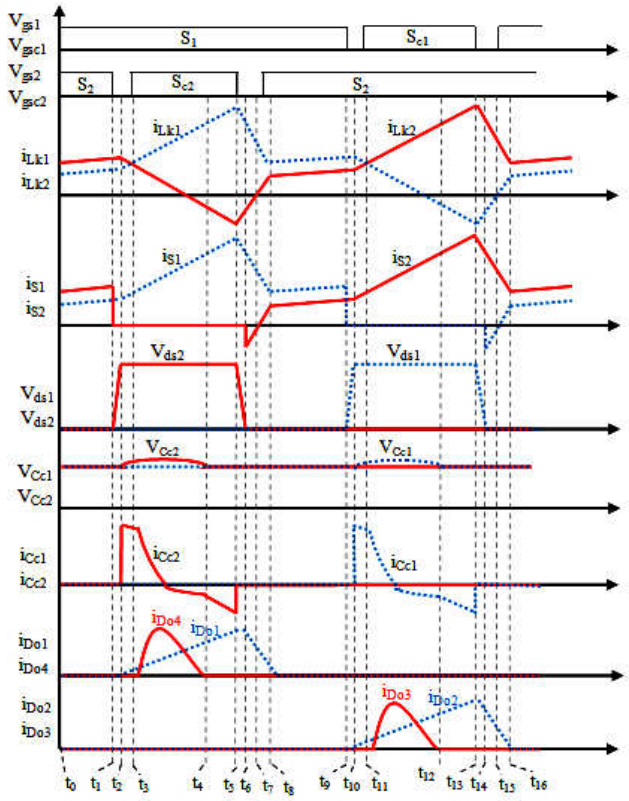

Figure 2. Key waveforms of proposed converter.

Time interval [t_0, t_1]: the main switches S_1 and S_2 conduct, and the clamp switches $S_{C1}$and S_{C2} are in OFF state. All diodes are in reverse biased. The current flowing though the magnetizing inductors L_{m1} and L_{m2} increases by input voltage linearly.

$$i_{Lm1}(t) = I_{Lm1}(t_0) + \frac{V_{in}}{L_{m1} + L_{k1}}(t - t_0) \qquad (1)$$

$$i_{Lm2}(t) = I_{Lm2}(t_0) + \frac{V_{in}}{L_{m2} + L_{k2}}(t - t_0) \qquad (2)$$

Time interval [t_1, t_2]: at the beginning of this time interval, the main switch S_2 goes to the OFF state, then the corresponding capacitor C_{S2} is energized by the current i_{Lm2}. Capacitor C_{S2} causes the main switch S_2 gets OFF with ZVS condition. At t_2, voltage of main switch S_2 becomes equal to clamp capacitor C_{C2}.

$$v_{ds2}(t) = \frac{I_{Lm2}(t_1)}{C_{s2}}(t - t_1) \qquad (3)$$

Time interval [t_2, t_3]: at t_2, charging of switch S_2 leads to diode D_{o1} and the inverse-parallel diode of the switch S_{C2} begin to conduct, and the leakage energy transfer to output. The coupled inductor L_1 works as transformer and forward mode and the coupled inductor L_2 works as flyback converter to supply energy to the load in the output. The leakage inductance L_{k2} and the capacitor C_{C2}, make a resonance circuit. The circuit operation at this stage is according to the following formula:

$$i_{Lk2}(t) = I_{Lm2}(t_2)\cos\omega_1(t - t_2) \qquad (4)$$

$$v_{CC2}(t) = V_{O3} + Z_0\, I_{Lk2}(t)\sin\omega_1(t - t_2) \qquad (5)$$

$$i_{s1} = i_{Lk1} = I_{Lm1}(t) + N\, i_{Do1} \qquad (6)$$

Where $\omega_1 = \dfrac{1}{\sqrt{L_{k2}.C_{C2}}}$

Time interval [t_3, t_4]: at t_3, the switch S_{C2} conducts in ZVS condition, as its inverse-parallel is conducting. The voltage across the capacitor C_{C2} will be equal to the voltage across the output capacitor C_{o3}. Therefore, the diode D_{o4} begins to conduct.

Time interval [t_4, t_5]: at t_4, the current of diode D_{o4} falls to zero and then the current of clamp capacitor C_{C2} becomes equal to the current leakage inductance L_{k2} [33].

Time interval [t_5, t_6]: at the beginning of this time period, the clamp switch S_{C2} gets OFF. While the voltage across the capacitor C_{S2} drops, the voltage across the S_{C2} rises with a same degree. Thus, the switch S_{C2} gets off with ZVS performance. The capacitor C_{C2} is disconnected from converter and the L_{k2} starts to resonance with the C_{S2}.

$$i_{Lk2}(t) = I_{Lk2}(t_5)[1 - \sin\omega_2(t - t_5)] \qquad (7)$$

$$v_{dS2}(t) = V_{dsS2}(t_5) - \frac{I_{Lk}(t_5)}{C_{S2}.\omega_2}[1 - \cos\omega_2(t - t_5)] \qquad (8)$$

Where $\omega_2 = \dfrac{1}{\sqrt{L_{k2}.C_{s2}}}$

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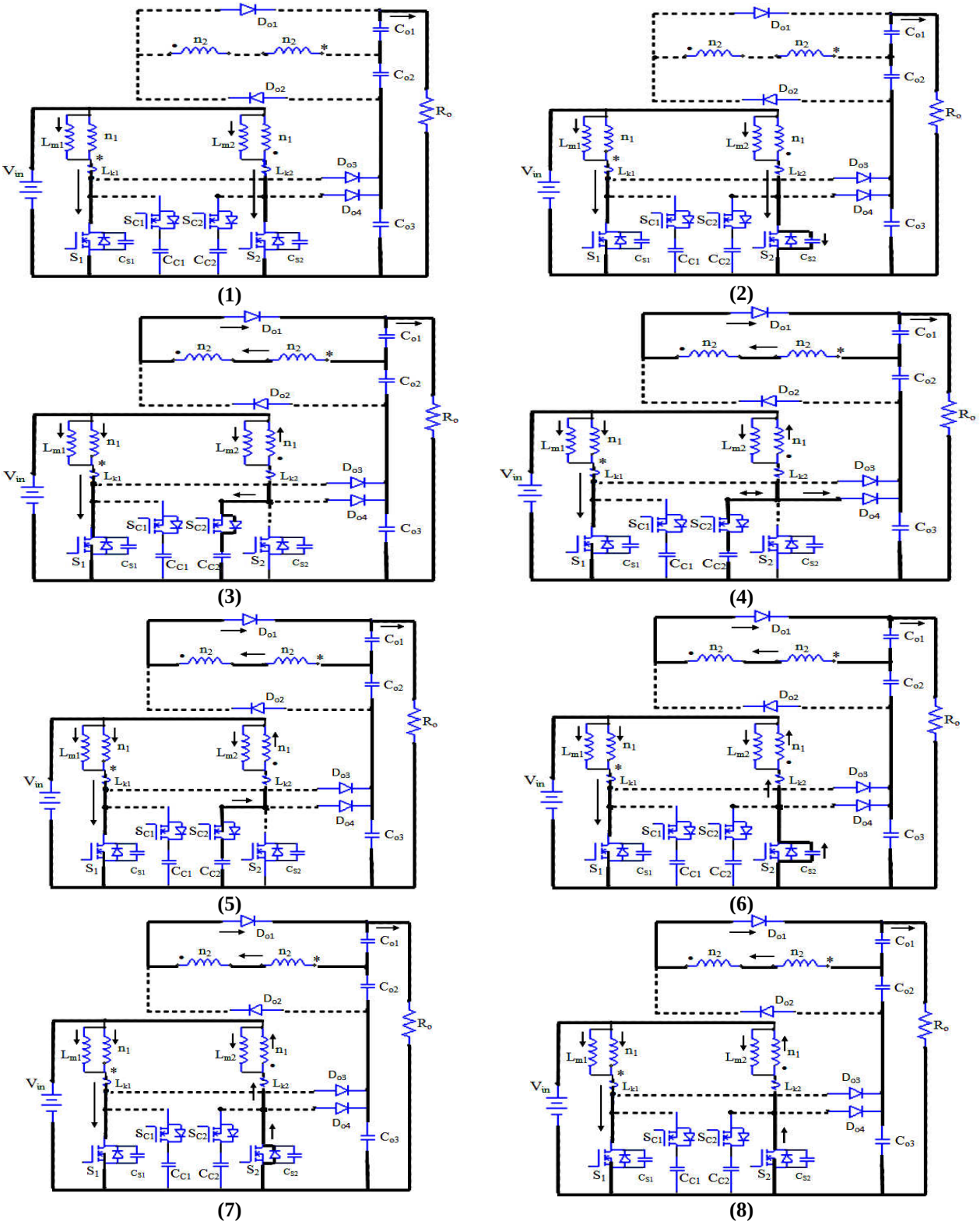

Figure 3. Different stages of the converter: (1) interval 1 (t_0 - t_1), (2) interval 2 (t_1 - t_2), (3) interval 3 (t_2-t_3), (4) interval 4 (t_3 - t_4), (5) interval 5 (t_4 - t_5), (6) interval 6 (t_5 - t_6), (7) interval 7 (t_6 - t_7), (8) interval 8 (t_7 - t_8)

Time interval [t_6, t_7]: Initially, the voltage across the switch S_2 is zero. Therefore, the corresponding diode of the switch S_2 starts to operate in the conducting mode. The current through L_{k2} increases linearly, which controls declining rate of the output diode D_{o1}.

$$i_{Do1}(t) = i_{Do1}(t_6) - \frac{V_{Co1}}{N^2 (L_{k1} + L_{k2})} \qquad (9)$$

Time interval [t_7, t_8]: at the beginning of this interval, the main switch S_2 will be ON with ZVS soft switching performance due to its inverse-parallel diode which conducts. At t_8, the leakage current L_{k2} reaches zero and the diode D_{o1} goes to the OFF state while the current is zero. The input voltage will charge two main inductors. A same pattern occurs in the rest of the switching time.

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III. DESIGN GUIDELINES

If the leakage inductance is zero (ideal condition), conduction resistance as well as the voltage drop are negligible. The voltage of the clamp and output capacitors can be acquired using equations (10) and (11):

$$V_{Cc} = V_{Co3} = \frac{V_{in}}{1-D} \tag{10}$$

$$V_{Co1} = V_{Co2} = \frac{N V_{in}}{1-D} \tag{11}$$

Where D is the duty cycle for the main switch. The output voltage is summation of the output capacitors. Therefore, the voltage gain is:

$$M = \frac{V_{out}}{V_{in}} = \frac{2.N+1}{1-D} \tag{12}$$

Equation (13) indicates the equality of the voltage across the clamp capacitors and the voltage stress across the power switches.

$$V_{stress\_main\ \&\ clamp} = \frac{V_{in}}{1-D} = \frac{V_{out}}{2N+1} \tag{13}$$

The voltage stress across the switches is proportional to the coupled inductor's turn ratio. Therefore, by selecting a proper turn ratio the voltage switch stress can be reduced. All active switches are turned off with ZVS due to parallel capacitors C_{S1} and C_{S2}.

The clamp switches are in the ON state under ZVS condition as their corresponding inverse-parallel diodes are conducting when switches S_{C1} and S_{C2} turn on. To meet the ZVS ON state of main switches, all the energy in parallel capacitor of the main switch has to be transferred to leakage inductance. Therefore, when the main switch is in the ON state, the stored energy in the leakage inductance has to be greater than the amount of energy in the parallel capacitor. Therefore, the zero voltage switching-ON performance of main switches is obtained from energy consideration:

$$2 L_K \frac{I_{in}^2}{4} \geq C_{S1} \left(\frac{V_{out}}{2N+1}\right)^2 \tag{14}$$

As a result:

$$L_K \geq \frac{2 C_S V_{out}^2}{(2N+1)^2 I_{in}^2} \tag{15}$$

The relationship of leakage inductance versus input current in different turn ratio is plotted in Fig. 4. The required leakage inductance in ZVS condition decreases as the input current increases. Equation (16) shows the proper determination of the clamp capacitor [14]:

$$C_C \geq \frac{(1-D)^2}{2\pi^2 L_K f_s^2} \tag{16}$$

The magnetizing inductor and the output capacitor are determined by considering a permissible percentage of ripple in the inductor current and proper voltage ripple on the output capacitor voltage [15].

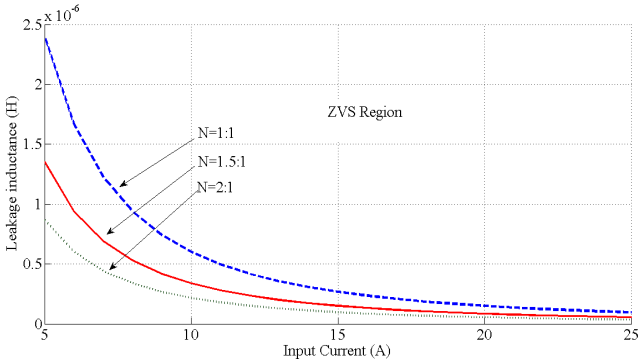

Figure 4. Relation of leakage inductance, and input current, and turns ratio.

IV. SIMULATION RESULTS

A PV array is used instead of the dc source of proposed converter in simulation. The parameters of PV modules are presented in table I. Four PV modules are connected in series and parallel to obtain high power level. Table II shows converter parameters. In order to achieve maximum power from PV array, average current control and maximum power point tracking (MPPT) control have been used. The voltage in MPP is computed by using IncCon MPPT method described in [16] and it is compared with extracted PV voltage. The difference between them is used as an input for voltage controller [17-24]. By comparing the output of current controller with carrier wave, appropriate pulse for the gate of main switch is generated. The phase difference between each gate signal is 180°, because there are two phases in proposed interleaved boost converter [25-32].

Fig. 5 illustrates control algorithm of the converter topology. The gate signals of the clamp switches S_{C1} and S_{C2} are complement with the gate signals for main switches S_1 and S_2. Fig. 6 shows the voltage, current and power profiles of output PV array without and with MPPT and with irradiance change. The currents of leakage inductances and input current are illustrated in Fig. 7. The ripple in the input current is not considerable because of the interleaved design. The voltage and current of clamp capacitor are shown in Fig. 8. Fig. 9 indicates the switching transition of the main and the clamp switches. It is shown that all power switches of converter are operating with zero voltage soft switching performance for the entire switching period that mitigates the power losses. The voltage and current profiles of the diode D_{o1} are depicted in Fig. 10.

TABLE I. PV MODULE CHARACTERISTICS

Model: RECAE220-us	
Max. output power, P_{max} (W)	220
Open circuit voltage, V_{OC} (V)	36.6

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MPPT voltage, V_{MPPT} (V)	28.7
Short circuit current, I_{SC} (A)	8.2
MPPT current, I_{MPPT} (A)	7.7

TABLE II. KEY PARAMETERS OF THE CONVERTER

Input Voltage, V_{in} (V)	59	Magnetizing inductor, L_m (uH)	130
Output voltage, V_{out} (V)	520	Output capacitors, Co (uF)	50
Output power, P_{out} (W)	880	Turns ratio, N	1:1
Main switches frequency, f_s (KHz)	100	Leakage inductances, L_{k1} and L_{k2} (uH)	1.5
Clamp Capacitors, C_{C1} and C_{C2} (uF)	3	Parallel capacitors, C_{S1} and C_{S2} (nF)	1

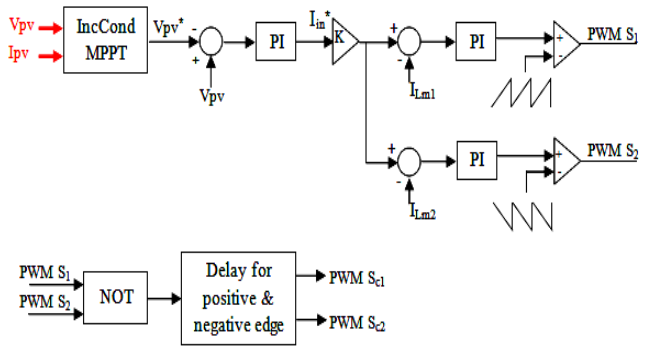

Figure 5. Control algorithm of the proposed converter

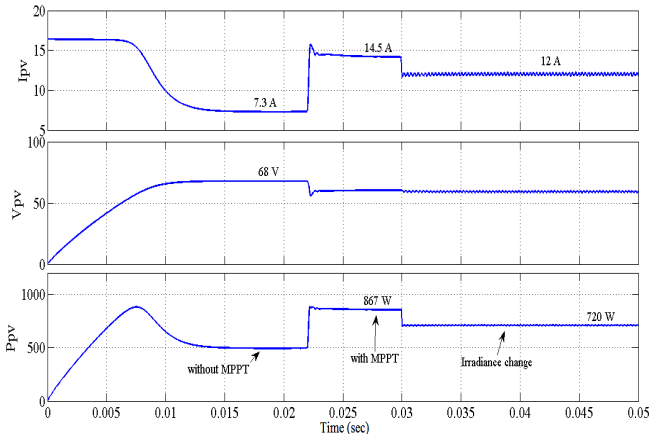

Figure 6.Voltage, current and Power of PV at without and with MPPT and irradiance change.

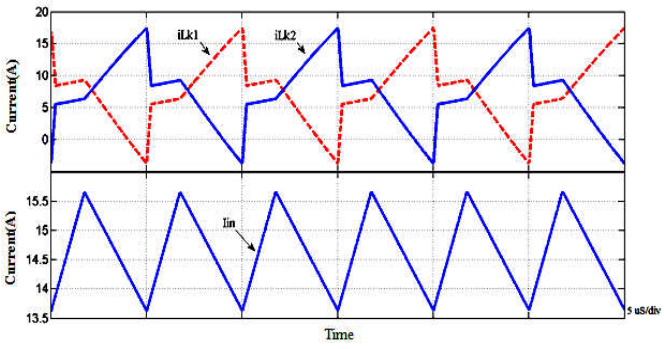

Figure 7. Input current i_{Lk1}, i_{Lk2}, and I_{in}

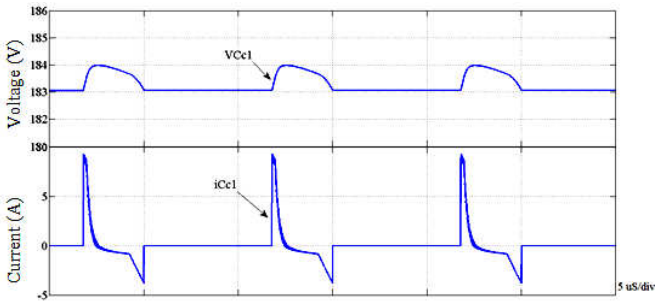

Figure 8.Voltage and current of the clamp circuit.

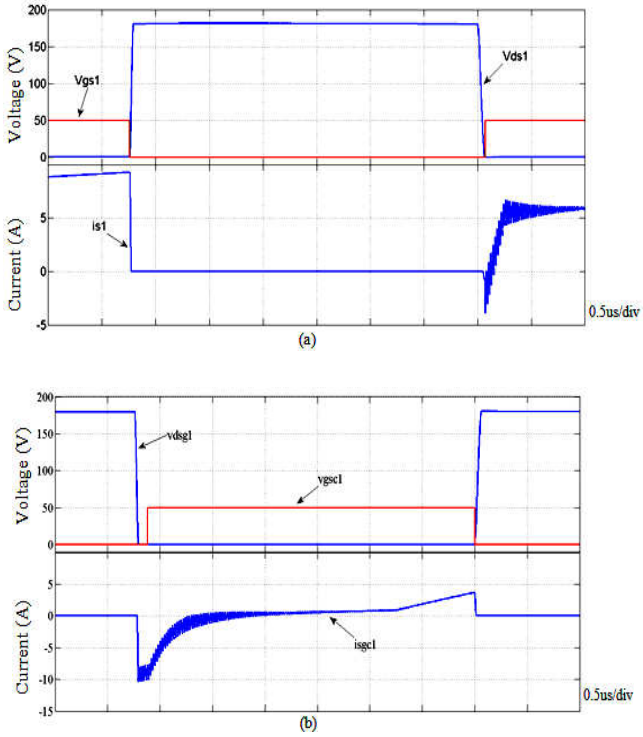

Figure 9. ZVT performance of (a) main switch, (b) clamp switch.

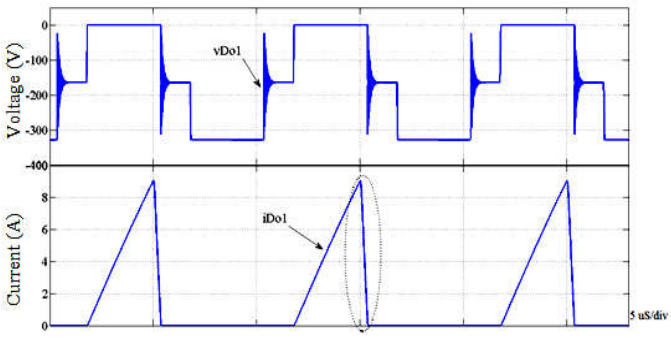

Figure 10.Voltage and current of diod D_{o1}.

The voltage stress across the diode is $\frac{2N}{2N+1}V_{out}$, which is less than the output voltage. The declining rate of the current through diode is controlled by leakage inductance. A comparison of measured efficiency at different levels of load for this proposed converter and the converter introduced in [13], is given in Fig. 11. There is approximately 3%

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improvement in efficiency compared with the converter proposed in [13] at 880W full load under the same testing scenario. The efficiency is enhanced with a less complicated configuration in comparison to the converter in [13].

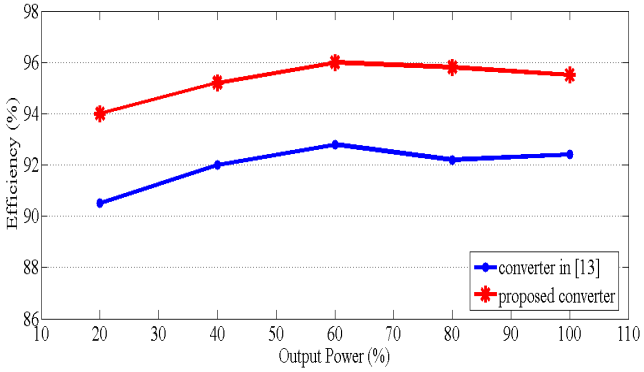

Figure 11. Measured efficiency comparison at different percent loads.

V. CONCLUSION

An efficient high voltage gain ZVS non-isolated converter with interleaved structure in input and voltage doubler structure in output of for PV system has been proposed in this paper. Zero voltage soft switching performance is realized by active clamp circuit to mitigate the power losses. The proposed converter also uses switches with low turn on resistance and voltage rate. Furthermore, due to interleaved operation the input current ripple can be mitigated. The steady state waveforms and stages analysis and design guidelines are discussed. At last, simulation results of converter with PV array 880W, 59V, 520V are presented. Simulation results confirm that the proposed interleaved converter is an appropriate option for conversions in which the high voltage gain and efficiency are two important factors.

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