Design and Implementation of PLL for Frequency Demodulation

MA. Jihan S. Abdaljabar, HaithamK.Ali

Abstract: ***Frequency modulation is widely used in radio transmissions, especially, in the broadcasting of VHF frequencies to provide medium for high quality audio transmissions. Phase locked loop, PLL FM demodulator or detector is a form of FM demodulator that has gained widespread acceptance in recent years. In this paper, PLL FM detectors were designed from the PLL integrated circuits where the frequency demodulation was obtained directly from the PLL circuit by taking the center frequency of the PLL todesign the FM carrier frequency. The PLL was operated as a complete IF strip, limiter, and detector employed in FM receivers. The essential parts of the FM demodulation system, which are (demodulator unit), (RF unit) and (audio unit),were designed by hardware and the designed parts were examined. As a result the output waveform for every part was measured in order to ensure that the design is compatible with the required conditions.***

Keyword: FM demodulator, IF strip, PLL, RF unit.

I. INTRODUCTION

A phase-locked loop or phase lock loop (PLL) is a control system that generates an output signal whose phase is related to the phase of an input signal. While there are several differing types, it is easy to initially visualize as an electronic circuit consisting of a variable frequency oscillator and a phase detector. The oscillator generates a periodic signal. The phase detector compares the phase of that signal with the phase of the input periodic signal and adjusts the oscillator to keep the phases matched. Bringing the output signal back toward the input signal for comparison is called a feedback loop since the output is 'fed back' toward the input forming a loop. Keeping the input and output phase in lock step also implies keeping the input and output frequencies the same. Consequently, in addition to synchronizing signals, a phase-locked loop can track an input frequency, or it can generate a frequency that is a multiple of the input frequency. These properties are used for computer clock synchronization, demodulation, and frequency synthesis . Phase-locked loops are widely employed in radio, telecommunications, computers and other electronic applications. They can be used to demodulate a signal, recover a signal from a noisy communication channel, generate a stable frequency at multiples of an input frequency (frequency synthesis), or distribute precisely timed clock pulses in digital logic circuits such as microprocessors.

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Since a single integrated circuit can provide a complete phase-locked-loop building block, the technique is widely used in modern electronic devices, without put frequencies from a fraction of a hertz up to many gigahertz's[1]

II. APPLIATION OF PLL

1. For higher phase lock precision, a new principle, the equivalent phase comparison frequency (EPCF) between signals in different frequencies. Using the new PLL based on EPCF, higher phase comparison and phase lock precision can be achieved with simple electrical circuits. Evidently, this principle is based on the analysis of time and phase, rather than on frequency simply. Quite high resolution can be achieved for phase processing method based on the principle of EPCF. [2]

2. This application describes an innovative slip frequency phase lock loop (PLL) which measures the rotor frequency ω_R and the rotor speed ω_m of a doubly-fed induction generator (DFIG). This information is required in implementing sensorless control of DFIGs by rotor-side voltage-source converters. For decoupled P-Q control, it is necessary to align the rotor γ-δ axes to the axes of the stator. A new γ-δ axes aligner is also proposed. The information extracted is: (i) the rotor position ($\omega_m t+\delta_m$), (ii) the rotor speed ω_m, (Hi) the rotor frequency ω_R. Proofs of concepts and proofs of decoupled P-Q control of a wind turbine driven DFIG are presented from simulation studies. [3]

3.Applying the PLL system as a multiplier of direct digital synthesizers (DDS) output frequency in hybrid frequency synthesizers was analyzed. Increasing of DDS output frequency helps to reduce the division ratio in the feedback loop and, as consequence, decrease the phase noise level. It was proved that the PLL multiplier makes a significant contribution to the phase noise level of the hybrid synthesizer. The comparison of noise performances of the hybrid synthesizer and two-loop PLL system was performed. [4]

4.This application use single-sideband frequency up-conversion was used to translate the AFM signal from the position sensitive detector to a fixed intermediate frequency of 10 MHz In this way, we fully benefit from the excellent noise performance of PLL-based FM demodulators still avoiding the intrinsic bandwidth limitation of such systems. Furthermore, the system becomes independent of the cantilever's resonance frequency. To investigate if the additional noise introduced by the single-sideband up converter degrades the system noise figure we present a model of the AM-to-FM noise conversion in the PLL phase detector. Using this model, we can predict an upper corner frequency for the demodulation bandwidth above which the converted noise from the single-sideband upconverter becomes the dominant noise source and therefore begins to deteriorate the overall system performance. The approach is

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validated by measured data obtained with a PCB-based prototype implementing the proposed demodulator architecture. [5]

III. BLOCK DIAGRAM OF THE DESIGNED SYSTEM

The block diagram of the PLL FM demodulator was designed as shown in figure (4.1). The input FM signal and the output of the VCO applied to the phase detector circuit. The output of the phase detector was filtered using a low pass filter, then the amplifier used for controlling the VCO. When there is no carrier modulation and the input FM signal is in the center of the pass band (i.e. carrier wave only) the VCO's tune line voltage will be at the center position. When deviation in carrier frequency occurs (that means modulation occurs) the VCO frequency follows the input signal in order to keep the loop in lock. As a result the tune line voltage to the VCO varies and this variation was proportional to the modulation of the FM carrier wave. This voltage variation was filtered and amplified in order to find the demodulated signal. As shown in figure (1) .

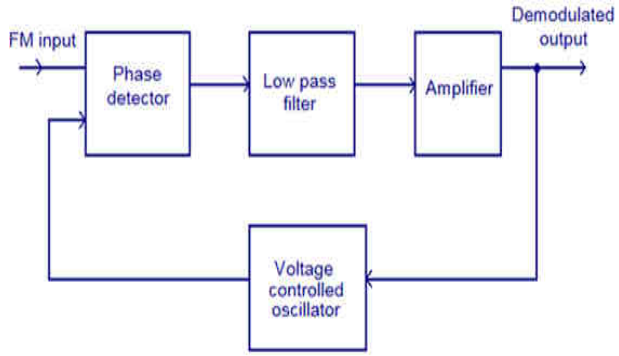

Figure (1) : block diagram of the designed system

The circuit diagram of the PLL FM demodulation was connected as shown in figure (2)

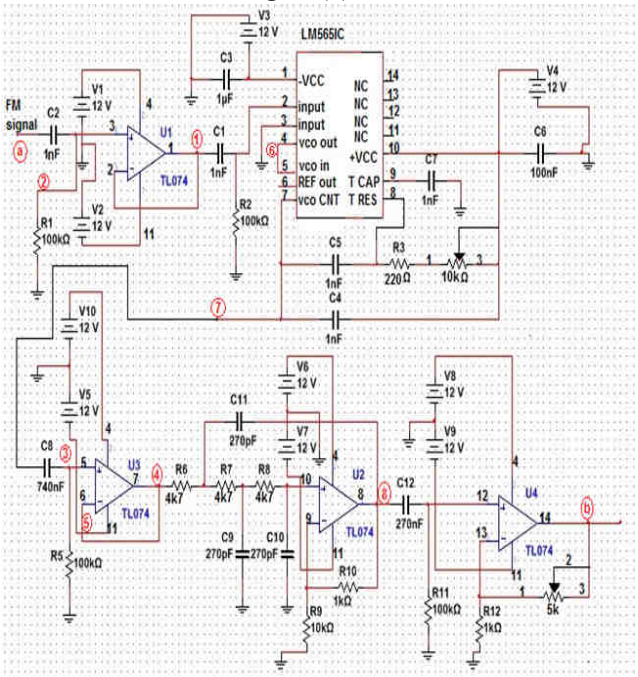

Figure (2) : The circuit diagram of PLL as FM demodulator

The implementation of the designed system is shown in figure (3)

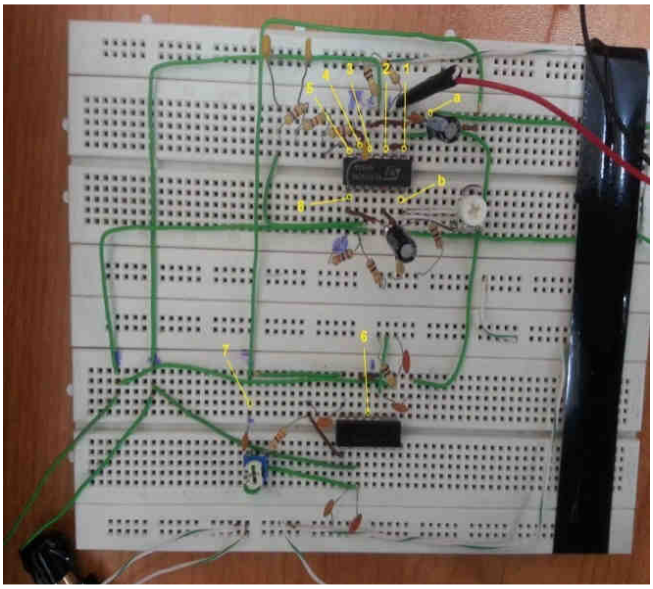

Figure (3) : The implementation of the designed system

The information of FM signal is given by the table (1)

Table (1) Information of the FM Signal

	Frequency *f* (KHz)	amplitude (V)p
Message signal m(t)	30	5
Carrier signal	170	1
FM signal	----	0.1

The FM signal which is used in testing the designed system shown in figure (5):

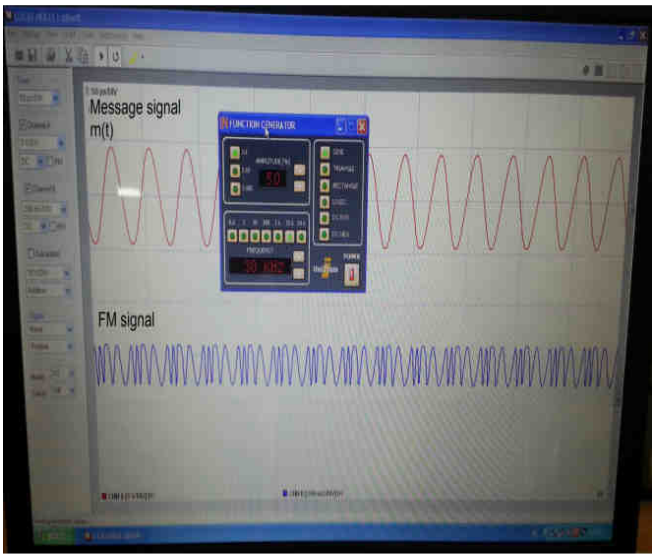

Figure (5): FM signal

Simulation of the designed circuit

In order to be sure that our system is working it's important to measure the output at each points of figure (3) The FM signal in figure (5) is applied to the designed system at point (a) and the output of this point shown in figure (6).

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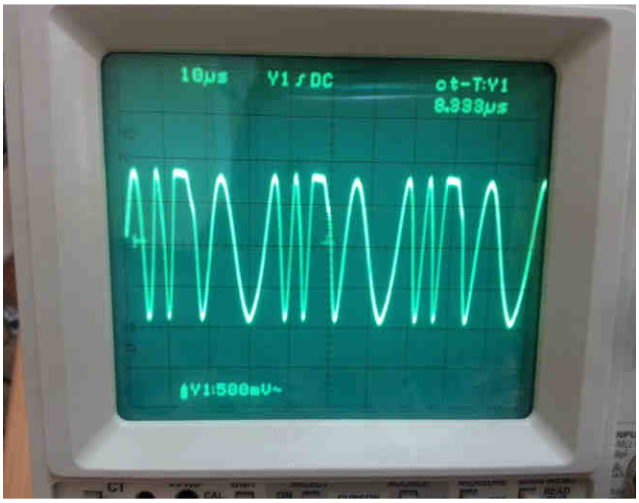

Figure (6): point (a) FM signal

The output of the signal at point (b) shown in figure (7).

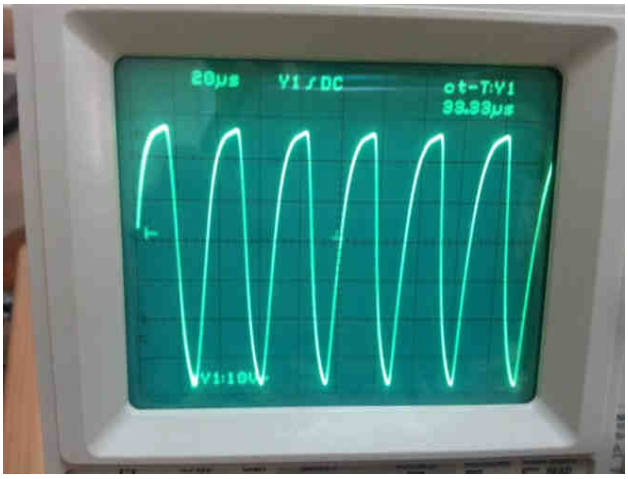

Figure (7) : point (b) output of the signal

The output of the signal at point (2) is shown in figure (8).

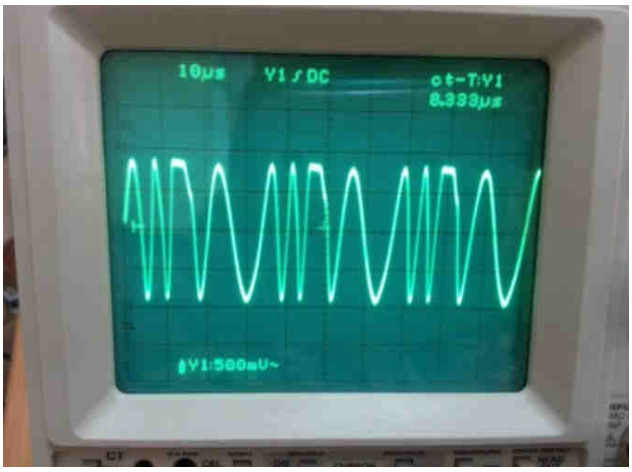

Figure (8) : point (2) FM signal after capacitor

The Buffer circuits helps in overcoming the impedance matching problem. for example if we want to send a signal from one devise to other ,if there is no impedance matching between this two then signal is not transferred. Now if we use buffer in between these two devises then the buffer, without changing the signal shape or value, simply transferred the signal.

Figure (9) is the output of the buffer circuit or point (1).

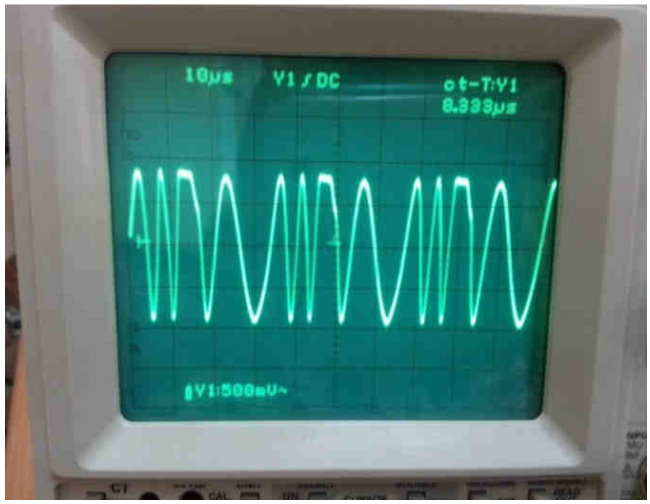

Figure (9): point (1) output of the buffer circuit

At this point (6) of (LM565IC), we can see the carrier signal that the voltage control oscillator (VCO) producesit, as illustrated in Figure (10)

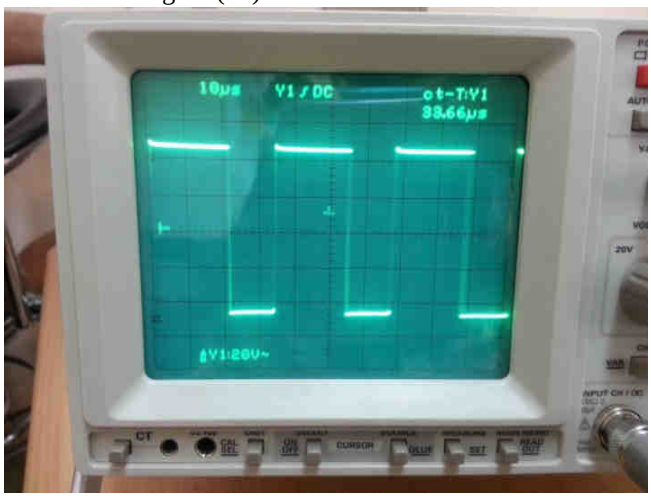

Figure (10) : point (6) the carrier signal that the voltage control oscillator (VCO) produce

At point (7), we can say that the FM signal is demodulated as shown in the Figure (11).

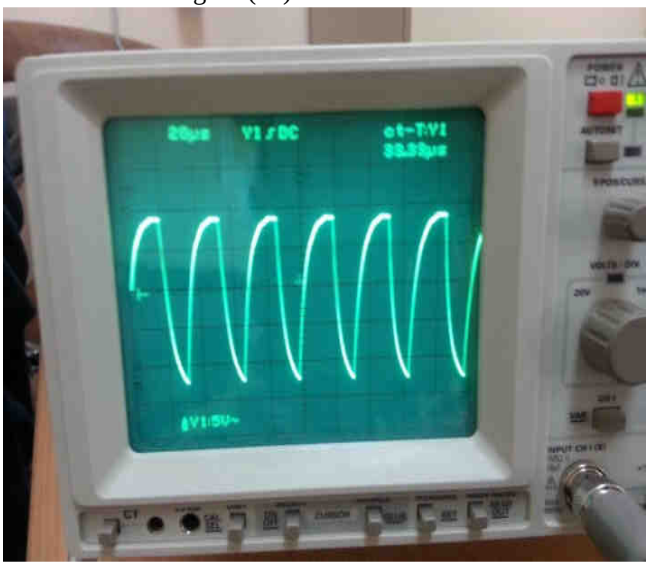

Figure (11) : point (7) the FM signal is demodulated

Figure (12) shows the output of point (3).

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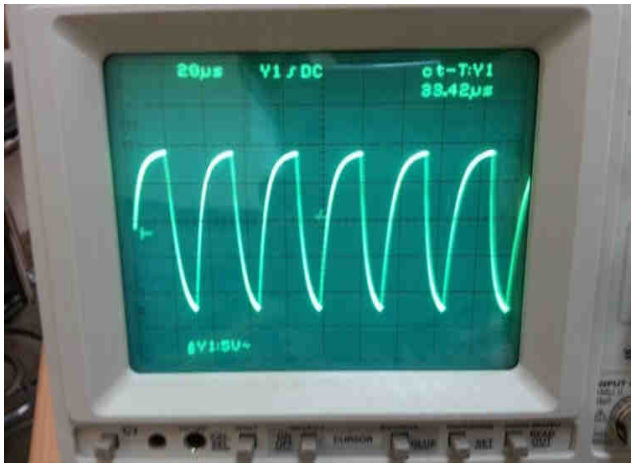

Figure (12) : point (3) message signal at the input of the buffer circuit

Figure (13) is the output of point (5).

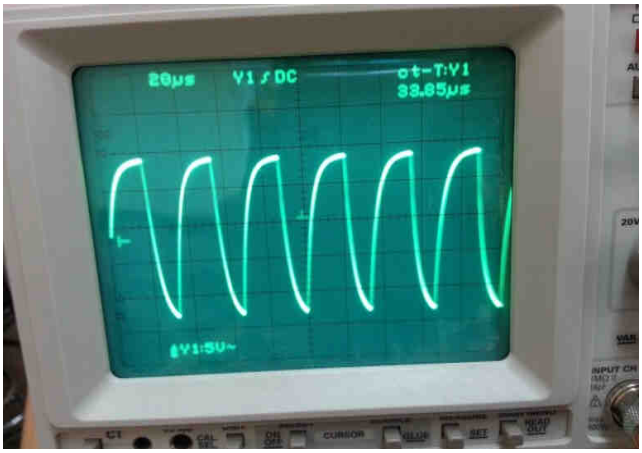

Figure (13) : point (5) message signal at the negative pin of the buffer circuit

Figure (14) represents **(sallen key low pass filter),** which is used after a buffer circuit, and it is used for elimination high frequency (it means that, it only allow low frequency).

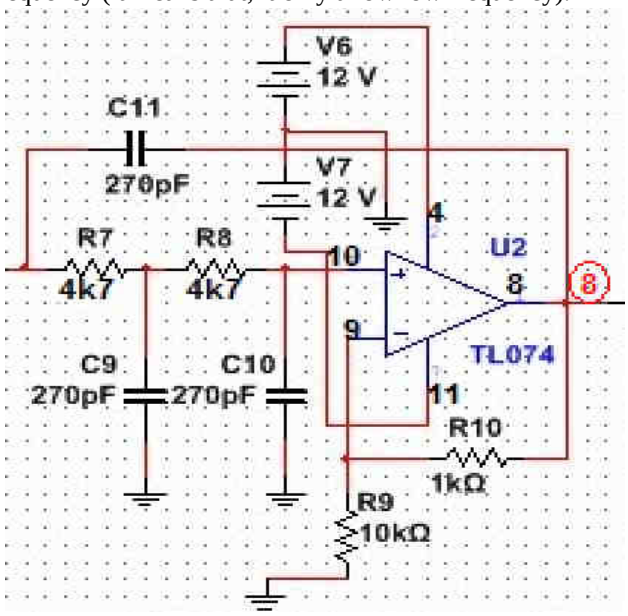

Figure (14): circuit of the sallen key low pass filter

Point (8) of (TL074IC) is the output of the **sallen key low pass filter** which illustrated in Figure (15)

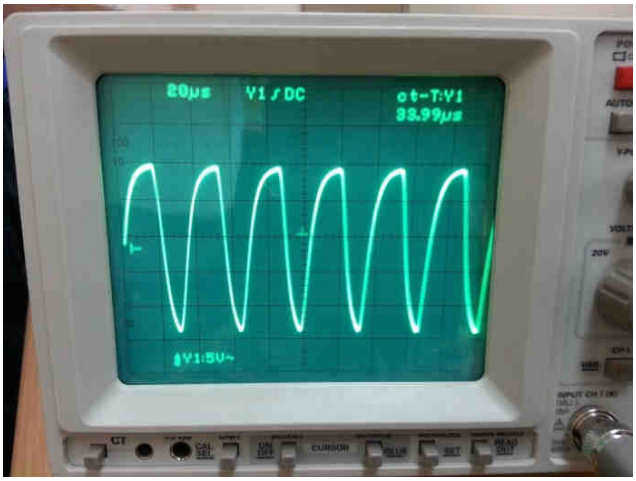

Figure (15) : pin (8) output of the sallen key low pass filter

Afterthe **sallen key filter**, we have an **operational amplifier** circuit, which is used to amplify or attenuate the amplitude of the message signal due to the (variable resistor) as shown in Figure (16)

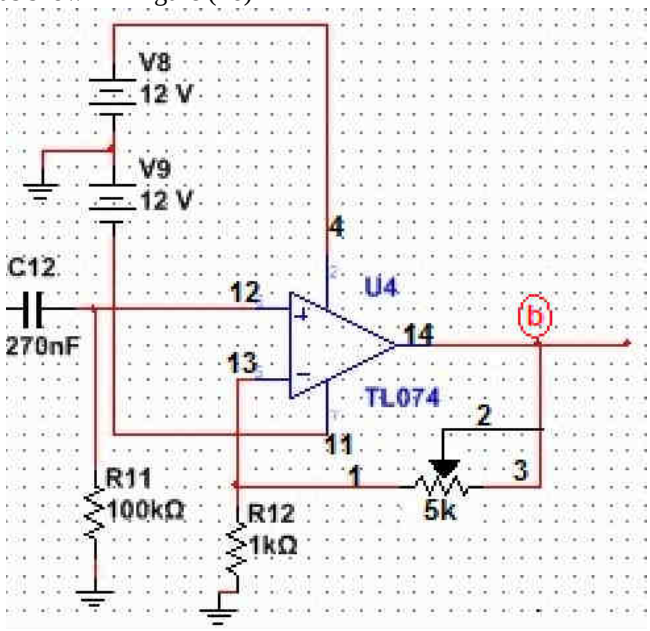

Figure (16) : circuit diagram of the operational amplifier

Figure (17) show the output of the point (b).

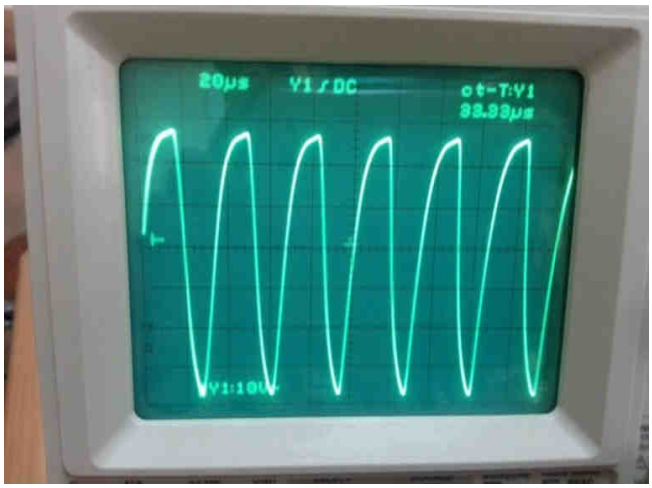

Figure (17): point (b) output of the amplifier

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V. CONCLUSION

The PLL FM demodulator is one of the more widely used forms of FM demodulator or detector. This paper aimed to design each part of the PLL FM demodulator which represents the design of the phase detector, the low pass filter, and the voltage controlled oscillator. The overall system was connected together and the output was measured at each point of the circuit using the oscillator, a distortion problem was found at the Vcout signal , the results of the loop filter, even though the output singles in general were acceptable and near to the ideal signals .

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