Power proficient Application Specific Communication Infrastructure for Advance SoC

Naveen Choudhary, M. S. Gaur, V. Laxmi

Abstract*— Networks-on-Chip is getting established as a communication infrastructure for future advance and complex SoC plateforms, composed of a large number of homogenous or heterogeneous processing resources. Application specific SoC design presents the prospects for incorporating custom NoC architectures that are more suitable for a specific application, and may not be suitable for regular topologies. The precise but often different communication requirements among IP-cores of the SoC call for the design of application-specific topology of SoC for better performance with respect to communication energy, latency, and throughput. In the presented work, a methodology for the design of customized irregular topology for SoC with complex communication behavior is proposed. The proposed methodology uses the aforementioned knowledge of the application's communication attribute to produce an power optimized network and corresponding routing tables.

***Index Terms*— SoC, on-chip networks, application specific NoC, interconnection network.**

I. INTRODUCTION

The supreme issue in designing the future complex Systems-on-Chip (SoCs) will be due to the global interconnects. The global interconnects are liable to increase the complexity of the the SoC as the requirement for the number of cores on a single chip increases. Moreover this will cause severe synchronization faults, unpredictable delays and high power spending. In view of these problems, the structured Network-on-Chip [1]-[4] is proposed as the effective solution in the complex Soc research domain. Early works in NoC (Network-on-Chip) [2], [3], [5] advocated the use of standard topologies such as meshes, tori, k-ary n-cubes or fat trees under the assumption that the wires can be well structured in such topologies. However most SoCs, especially application-specific SoC, are heterogeneous in nature, with each core having varying size, functionality and communication attributes. For such application specific Soc, the standard topologies can lead to communication infrastructure that defectively matches the application's communication attribute. This may leads to large wiring complexity after floor-planning, as well as major power and area overheads.

For application specific SoCs mostly the system is designed with static mapping of tasks to processors and hardware cores and hence the communication attributes of such SoC can be well characterized at design time itself. Therefore it is anticipated that SoCs with irregular topology/communication infrastructure tailored to the application's communication necessities to have an edge over the SoCs with regular topology. Due to limited buffer space in NoC, it is utmost necessary to ensure deadlock free communication. Therefore the routing chosen for such SoC should ensure deadlock avoidance. The communication deadlock in NoC happens due to the cyclic wait dependencies caused by classic flow-control schemes in order to prevent buffer overflows. Deadlock-avoidance based approaches have traditionally been preferred over deadlock-recovery schemes [6] as they tend to be more efficient. Traditionally, the proof of deadlock-freedom has mostly been carried out on the assumption of the regular construction pattern [6]-[8] and is therefore far more complex in irregular topologies with non uniform structure. There are, however, deadlock free topology independent routing algorithms such as up*/down* [9], L-turn [10], down/up [11], and prefix-routing [12]. These algorithms are based on turn prohibition, a methodology which avoids deadlock by prohibiting a subset of all turns in the network.

The foremost issue for successful acceptance of the Network-on-Chip paradigm is in reducing the power/energy requirements during communication among the cores. In [13]-[15] Hu and Marculescu has addressed the energy-aware mapping algorithm issues to minimizes the total communication energy cost for a 2-D mesh NoC architecture under real-time performance constraints. Inspired by these works, in this paper a genetic algorithm based methodology is proposed for the design of power proficient customized irregular Networks-on-Chip. The presented methodology make use of the predefined application's communication attributes to design an power proficient network topology along with desired routing tables for deadlock free communication. It is worth highlighting here that the topology and routing table generation are tightly coupled aspects of NoC topology generation and can lead to suboptimal solutions if optimized in separation. The experimental result undoubtedly demonstrate the applicability of the proposed methodology

This paper is organized as follows. Communication Model and Architecture for Complex application specific SoC are presented in Section II.

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The proposed power proficient methodology for futuristic complex SoC design is presented in Section III. The genetic algorithm for optimization used by the proposed methodology in Section III is described in Section IV. Section V presents the experimental results followed by a brief conclusion in Section VI.

II. COMMUNICATION MODEL AND ARCHITECTURE FOR COMPLEX APPLICATION SPECIFIC SOC

The basic platform for the proposed methodology including the basic communication model assumed along with the associated NoC architecture and routing function are described in this section.

The mapping of tasks in *Task graphs* [15] to the actual physical cores/tiles/hardware resources in the *NoC topology graph* (NoC) can be done with the help of intermediate mapping to *Core Graph* as exhibited in Figure 1.

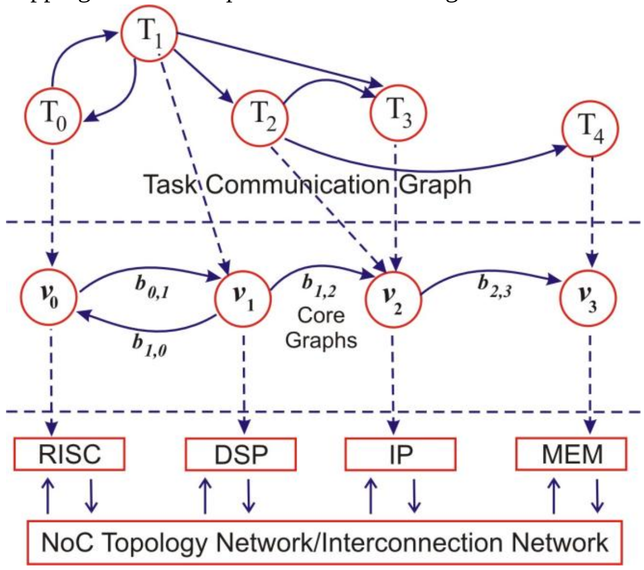

Fig. 1. Application specific communication model for NoC.

Definition –Core Graph: *Core Graph is a directed graph, G (V, E) with each vertex* $\nu_i \in V$ *representing an IP core and a directed edge* $e_{i,j} \in E$*, representing the communication between the cores* ν_i *and* ν_j*. The weight of the edge* $e_{i,j}$ *denoted by* $b_{i,j}$*, represents the desired average bandwidth requirement of the communication from* v_i *and* v_j*.*

Definition- NoC topology graph: *NoC topology graph is a directed graph N (U, F) with each vertex* $\upsilon_i \in U$ *representing a node/tile in the topology and a directed edge* $f_{i,j} \in F$ *represents direct communication channel between vertices* υ_i *and* υ_j*. Weight of the edge* $f_{i,j}$ *denoted by* $b_{i,j}$ *represents the available link/channel bandwidth across the edge* $f_{i,j}$*.*

The energy model proposed in [15] can be extended for irregular topology as follows

$$E_{bit}(t_i, t_j) = n_{hops} \times Er_{bit} + \sum_{k=1}^{n_{hops}-1} El_{bit}^{k}$$

Where $E_{bit}(t_i, t_j)$ is the average dynamic energy consumption for sending one bit of data from tile t_i to tile t_j, n_{hops} is the number of routers the bit traverses from tile t_i to tile t_j, Er_{bit} is the energy consumed by router for transporting one bit of data and El_{bit} is the energy consumed by link/channel for transporting one bit of data. The second term of the summation in above equation basically represents the bit energy consumed by each channel in the route the bit traverses from communication source core to the intended destination cores in its routing path.

For optimized chip layout, floorplanning according to desired metric like area can be done as a first step with the help of available floorplannning tools such as B*-Trees [16]

The presented work uses the escape path based routing function as proposed by [17]. To provide deadlock free communication in the NoC, the up*/down* routing [9] and Left-Right routing [10] were used. These routing functions assign direction to the channels of the NoC with the help of a spanning tree of the give NoC topology.

In [17], a generic methodology for designing adaptive routing function for Irregular NoC was proposed. The proposed methodology allow messages to follow minimal paths, in most cases, reducing message latency and increasing network. Moreover the methodology enforces the deadlock free route to be followed only when the minimal path is occupied by other traffic/packet. This methodology assumes that all the physical channels in the NoC can be split into two virtual channels i.e. original virtual channel and the new virtual channel. Moreover the presence of a given deadlock free routing functions based on turn prohibition [8] for the given irregular NoC is also assumed. The methodology further proposes to extend the given routing function in such a way that newly injected messages can use new channels without any restriction as long as the original channels are used exactly in the same way as in the original routing function. In this paper original channels are made to use deadlock free paths based on up*/down* (Left-Right) deadlock free routing functions and new channels are allowed to follow the shortest available path to the destination. The modified routing function allows a packet arriving on a new channel following shortest path to be routed to any channel without any restrictions but preferably with higher priority to new channels as new channel assure shorter paths and higher adaptively (flexibility). If no new channels are available due to congestion, one of the original channels following up*/down* (Left-Right) must be provided. However, once a packet acquires an original channel following up*/down* (Left-Right) path, it is not allowed to do transition to a new channel anymore to avoid deadlock situation.

III. POWER PROFICIENT DESIGN METHODOLOGY

Based on the routing scheme presented by Silla et. al. [17], a novel genetic algorithm based methodologies referred as *SPF* (*shortest-paths-first*) for power proficient NoC communication Infrastructure generation is presented in this section. The presented methodologies generate an power proficient customized NoC topology along with the required routing tables to provide deadlock free communication according to the communication requirement of the application under consideration.

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In both the presented methodologies, information from the floorplan and *Core Graph* exhibiting the chiplayout and traffic characteristics respectively are taken as inputs as exhibited in Figure 2. Assuming over the cell routing [18], the link length among the nodes in the chip layout can be taken according to Manhattan distance. In the proposed methodologies, the channel length is not permitted to exceed the maximum permitted channel length (emax) due to constraint of physical signaling delay. This also prevents the algorithm from inserting wires that span long distances across the chip. Also, the cores of the generated topology are not allowed to exceed a given maximum permitted node-degree (ndmax). This constraint prevents the algorithm from instantiating slow routers with a large number of I/O-channels that would otherwise decrease the achievable clock frequency due to internal routing and scheduling delay of the router.

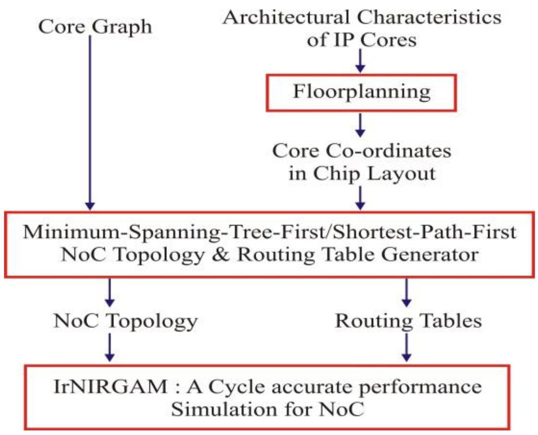

Fig. 2. Network construction using GA based proposed methodology

Energy Aware Topology Extension Phase: While keeping the constraints on nd_{max} and e_{max}, the topology is generated by laying the shortest energy path for each traffic characteristics (edges corresponding to pair of nodes in the *Core Graph*) with respect Manhattan distance from the area optimized floorplan. .Due to constraints on nd_{max} and e_{max}, the order in which such shortest energy/power paths are generated basically decides the total communication power/energy requirement of the generated topology. The optimized order of traffic characteristics of the application is found using a *genetic algorithm* (refer next section). The routing tables of nodes/routers in the discovered shortest energy path are updated with the routing table entry type tag as *shortest path*.

Deadlock Avoidance Phase: A *minimum spanning tree* (*MST*) using Prim's algorithm is generated on the nodes of the *Core Graph* according to the information regarding the Manhattan distance from the floorplan with the constraints on nd_{max} and e_{max} firmly kept. The core with maximum communication requirement is assumed as the root of the tree. The minimum spanning tree in the topology helps in classifying all the channels/links of the topology as "up" ("Left") or "down" ("Right"). Lastly the proposed methodology uses the modified Dijkstra's algorithm according to *up*/down** (*Left Right*) rule for finding deadlock free escape routing paths from each node in the *shortest power path* to the corresponding destination in the generated NoC and tags them as *up*/down** (*Left-Right*).

While taking routing decision the output channels tagged as *shortest path* are selected with higher priority and *up*/down** (*Left Right*) tagged channels are selected only when no output channel corresponding to shortest path is free.

As shortest power paths in the topology are generated first in *SPF* and so there can be a possibility that not enough number of free ports is available to construct the minimum spanning tree later. In such case a minimum number of ports per core need to be reserved before finding the *shortest power paths*. However experiments showed that if communication requirement are uniformly distributed over the *Core Graph* then such problems are rare if any.

IV. POWER PROFICIENT GENETIC ALGORITHM

A genetic algorithm [19] based heuristic is used to find the best order of the *traffic characteristics* to generate the *shortest power/energy paths* in topology such that the communication energy requirement of the application is optimized. Genetic algorithm is a search technique used in determining exact or approximate solutions to optimization and search problems. Genetic algorithms are a particular class of evolutionary algorithms that uses techniques inspired by evolutionary biology such as inheritance, mutation, selection, and crossover. The proposed genetic algorithm explores the search space extensively to generate an irregular network/topology with optimized communication power/energy requirement for the given application. The proposed genetic algorithm formulation is as follows.

A. Solution Space

In formulation of the proposed methodology, each chromosome is represented as an array of genes. Maximum size of the gene array is equal to the number of edges in the *Core Graph*. Each gene of the chromosome represents a *traffic characteristic* (*an edge corresponding to a pair of nodes in the Core Graph*)

B. Initial Population

A large population (i.e. 500 chromosomes) of chromosome is initially generated. The chromosomes of the initial population are generated by assigning *traffic characteristics* of the application to the chromosome's gene array in some random order. The initial population is later sorted according to the increasing order of total communication energy requirement of the generated topology (chromosome). It is worth highlighting here that the communication energy consumption by a chromosome varies depending on the *traffic characteristics order* (*order of elements in gene array*) of the chromosome.

C. Crossover

In each generation, crossover is performed on 50% of the population with the bias towards the *Best Class* of the chromosome population. For achieving crossover of two chromosomes, a random *crossover* point is selected. Two new chromosomes are created by the crossover operation. The new chromosomes are created by copying the *traffic characteristics* (*genes*) from their respective parents till *crossover point* or from *crossover point* to the end of the chromosome and then the remaining *traffic characteristics* (*genes*) are copied according to the order of *traffic characteristics* (*genes*) in the other chromosome such that there are no duplicate

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traffic characteristics in the created chromosomes. Figure 3 shows an example crossover operation.

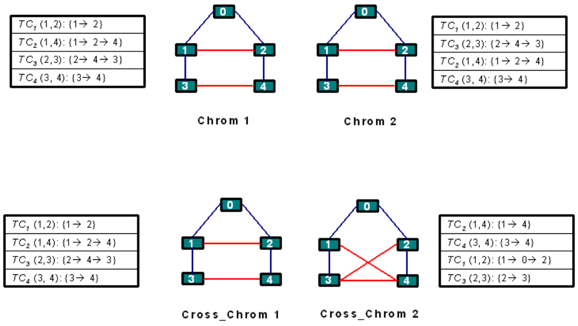

Fig. 3. Example Crossover operation assuming ndmax = 3

D. Mutation

In each generation, mutation is performed on 40% of the population to avoid the solution from getting stuck up in the local minima. Two types of mutations with probability of 50% each are performed in each generation. In first type of mutation a gene in the gene array of the chromosome with highest energy requirement is swapped with a randomly selected gene of the chromosome. In second type two randomly selected genes in the gene array of the chromosome are swapped. Figure 4 shows an example mutation operation.

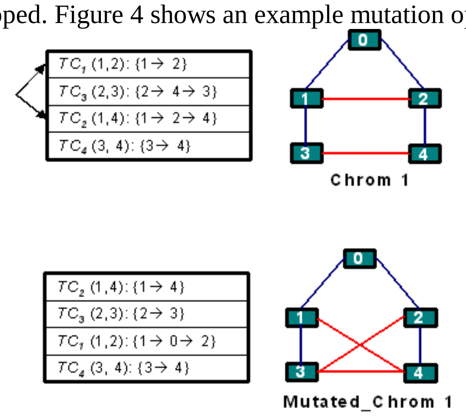

Fig. 4. Example Mutation operation assuming nd_{max} = 3

E. Fitness Measure

The cost function used to measure the fitness of the chromosomes in the population can be formulated as under.

$$Cost = Ec_i / X$$

Where X is maximum chromosome power/energy requirement among all the chromosomes in the population, Ec_i is the energy requirement for chromosome c_i. Fitness of chromosome is regarded as high if its cost approaches 0. It may be noted that, the best 10% chromosomes (referred as *Best Class*) in any generation are directly transferred to the next generation so as not to degrade the solution between the generations. After power proficient genetic algorithm is made to run for a required number of generations, the NoC topology and routing tables corresponding to the *best* output chromosome are accepted as the customized power/energy optimized application specific NoC.

V. EXPERIMENTAL RESULTS

The generated power proficient application specific topology was evaluated with respect to the communication energy consumption with applied traffic load on the NoC simulation framework. In order to obtain a broad range of different irregular traffic scenarios, multiple *Core Graphs* using TGFF [20] were randomly generated with diverse communication requirement of the IP Cores. For performance comparison, a NoC simulator *IrNIRGAM*, extended version of *NIRGAM* [21] supporting irregular topology with the facility of supporting escape path routing for avoiding deadlock condition, was implemented. *IrNIRGAM* is a discrete event, cycle accurate simulator. *IrNIRGAM* supports irregular topology framework with source and table based routing in a wormhole switching based architecture wherein an IP Core is directly connected to a dedicated router. In *IrNIRGAM*, input buffered routers can have multiple virtual channels (VCs) and uses wormhole switching for flow control. The packets are split into an arbitrary number of flits (flow control units) and forwarded through the network in a pipelined fashion. A Round-Robin scheme for switch arbitration is used in the router nodes to provide fair bandwidth allocation while effectively preventing scheduling anomalies like starvation. For performance comparison on experimental set, the *IrNIRGAM* was run for 10000 clock cycles with applied packet injection interval to evaluate the network performance with varying traffic load. The energy consumption by the flits reaching their corresponding destination and flit latency were used as performance metric. The energy consumption by router in transmitting a bit is evaluated using the power simulator orion [22] (for 0.18µm technology. Similarly the dynamic bit energy consumption for inter-node links (El_{bit}) can be calculated using the following equation.

$$El_{bit} = (1/2) \times \alpha \times C_{phy} \times V_{DD}^2$$

Where α is the average probability of a 1 to 0 or 0 to 1 transition between two successive samples in the stream for a specific bit. The value of α can be taken as 0.5 assuming data stream to be purely random. C_{phy} is the physical capacitance of inter-node wire under consideration for the given technology and V_{DD} is the supply voltage.

A. Experiments on SPF and Regular NoC with Random Benchmarks

To compare the performance of the proposed methodology with regular NoC, the performance of the proposed methodology with up*/down* and Left-Right routing function were compared with 2D-Mesh NoC with XY and OE routing for the packet injection intervals according to the application's traffic characteristics. The sizes of the tiles are kept same in the proposed methodologies as in regular 2D-Mesh. Fig. 5 shows the performance comparison of *SPF* with 2D-Mesh averaged over 50 generated power proficient irregular topologies with varying number of cores from 16 to 81, nd_{max} = 4 and e_{max} was taken as 2 times the length of the core. The *SPF* with up*/down* (Left-Right) routing shows reduced average flit latency in the range of 10 (9.4) clocks to 20.9 (18.4) clocks and 13.8 (13.2) clocks to 76 (69) clocks in comparison to 2D-Mesh with XY and OE routing respectively. The average per flit communication energy comparison of *SPF* with 2D-Mesh shows reduction in the range of 18.8% (18.5%) to 29.2% (25.8%) and 25.2% (24.6%) to 54.7% (53%) in comparison to XY and OE routing respectively for up*/down* (Left-Right) routing.

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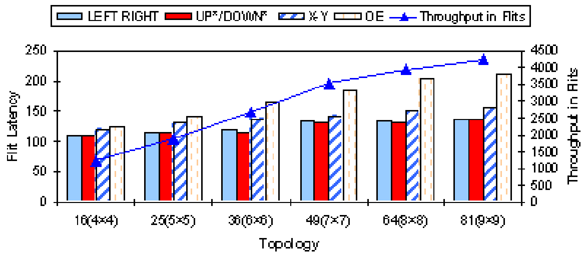

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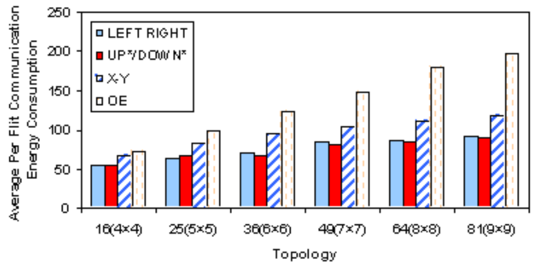
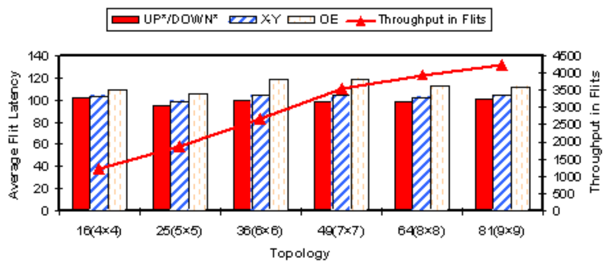


(b)

Fig. 5. SPF performance comparison with 2D-Mesh (a) Average flit latency (in clock cycles) and (b) Average communication energy consumption per flit (in pico joules)

B. Experiments on SPF and Regular NoC with Smart Mapping



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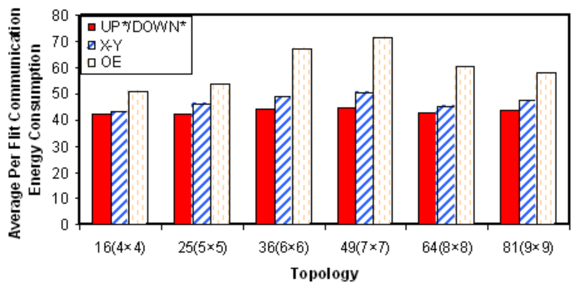


(b)

Fig. 6. *SPF* and *2D-Mesh* performance comparison for smart application to Core mapping (a) Average flit latency (in clock cycles) and (b) Average communication energy consumption per flit (in pico joules)

In [13], a methodology for smart mapping of application to cores of 2D-Mesh Regular NoC with the objective to minimize total communication energy was proposed. The proposed SPF methodology with up*/down* routing function for generating irregular NoC was compared with the technique proposed in [13] for equivalent tile sizes and application to core mapping.

The performance results as illustrated in Figure 6 shows reduction in flit latency in the range of 1.7 clocks to 5 clocks and 7.5 clocks to 20.4 clocks for SPF methodology for equivalent throughput in comparison to the 2D-Mesh with XY and OE routing respectively for the intelligent mapping. Similarly SPF for equivalent throughput showed reduction in average per flit communication energy in the range of 1.6% to 10.9% and 17% to 37% in comparison to 2D-Mesh with XY and OE routing respectively for the smart mapping.

C. Experiments on SPF and Regular NoC with Multimedia System

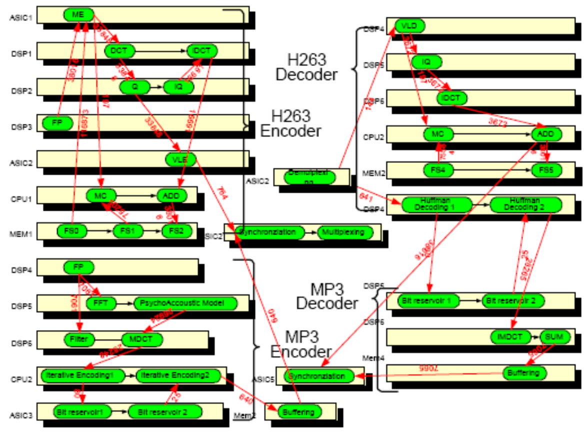
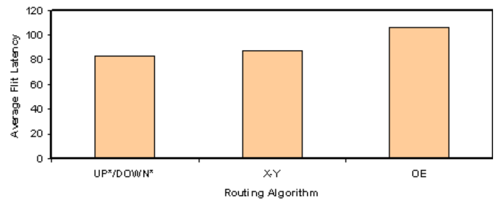
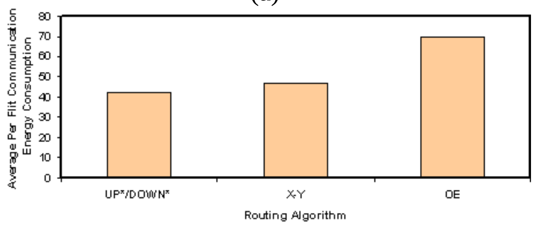


Fig. 7. Communication Trace Graph for *MMS*



(a)



(b)

Fig. 8. *SPF* and *2D-Mesh* performance comparison for *MMS* (a) Average flit latency (in clock cycles) and (b) Average communication energy consumption per flit (in pico joules)

To evaluate the potential of the proposed algorithm for real applications, a generic Multi Media System (*MMS*) application was considered. *MMS* is an integrated video/audio system which includes an h263 video encoder, an h263 video decoder, an mp3 audio encoder and an mp3 audio decoder. The application was partioned into 40 distinct tasks and then these tasks were assigned and scheduled onto 25 selected IPs. These IPs range from DSPs, generic processors, embedded DRAMs to customized ASICs. The communication trace graphs as shown in Fig. 7 for the same were obtained from the work presented by Hu et al. [13].

The performance analysis of the proposed methodology in comparison to regular mesh topology for the stream of information satisfying the communication trace graph of Fig. 7 are summarized in Fig. 8.

Fig. 8 shows reduction in latency on average of 4.2 clocks and 22.5 clocks in support of *SPF* methodology for equivalent throughput in comparison to the *2D-Mesh* with XY and OE routing respectively with smart task to core mapping as proposed in [13] for the *MMS* as shown in Fig. 7. Similarly *SPF* for equivalent throughput showed reduction in average per flit communication energy of 9% and 39% in comparison to *2D-Mesh* with XY and OE routing respectively with smart task to core mapping.

VI. CONCLUSION

The presented work proposes a methodology for the design of power proficient customized Irregular topology for the application specific complex SoC's communication infrastructure. A genetic algorithm based methodology is proposed for generating the optimized power proficient NoC The proposed methodology uses up*/down* and Left-Right routing as escape path for deadlock prevention. However the proposed methodology is adaptable with any of the topology agnostic routing algorithms where generic routing rules based on turn prohibition can be enforced. It is highlighted that the combined treatment of the routing and topology/network generation as done in the presented methodology offers a huge potential of optimization for future application-specific NoC/SoC architectures.

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