

Analysis and Simulation of Active Clamped Quasi-Resonant DC Link Inverter

Bal Mukund Sharma, A. N. Tiwari, K. P. Singh

Abstract—This paper proposes a simulation developed to use pulse width modulation (PWM) technique with the active clamped quasi-parallel resonant dc link (ACQPRDCL) inverter in order to increase the advantages of the PWM which allows to reduce the switching losses of the power devices. The new ACQPRDCL ensures zero crossing for a time period, and at any time required for soft switching (SS) and PWM operation of the inverters, respectively.

The principle of operation is analyzed and verified by PSPICE simulations.

Index Terms— PWM, ACQPRDCL, ACQPRDCL inverter, soft switching, soft switching inverter, simulation.

I. INTRODUCTION

Resonant techniques are used generally to provide soft switching in soft switching inverters (SSI). In fact, this is not a new idea because resonant circuits had been used to achieve the forced commutation of thyristors for many years. SS inverters are divided into two broad categories namely pole commutated and resonant dc link inverters (PCI and RDCLI). While PCI basically has one resonant tank per pole or leg and a capability of PWM operation, RDCLI has one common tank on dc link but not the PWM operation capability. Moreover, PCI has more components and a higher cost than its RDCLI counterpart [1-14].

Soft switching inverters have been proposed to minimize the switching losses. One of the most successful and popular soft switching topologies is the resonant bank in the DC link and a control strategy called sigma delta modulation technique proposed by recent papers. One of the biggest problem of the resonant link inverters is that the control strategy of the inverter is not capable of offering facilities of PWM technique such as improving the output voltages of the inverter by increasing the switching frequency. So far a few studies have been reported to overcome this problem [1-14].

A lot of research on RDCLI having the cheapest solution for SS has been presented in recent years. RDCLI inverters are divided into two major groups namely basic resonant and parallel resonant dc link inverters (BRDCLI and PRDCLI). The inverter is connected to the voltage source via an inductor, there is not the PWM operation capability, and the inverter voltage stress is very high in the BRDCLI basically.

To restrict the voltage stress, the active and passive clamped (AC and PC) BRDCLI inverters have been improved. Also, the quasi resonant (QR) subgroups of these inverters

have been presented to provide the PWM operation capability for these inverters, which can generally operate with discrete pulse modulation (DPM) [1]-[3], [6], [8]-[10],[14].

In this study, a new ACQPRDCL circuit for SS inverters is presented. It ensures that dc link voltage falls to zero at any time required and stays at zero for a time period needed. Thus, it provides SS and PWM operation for the inverters. Also, the new ACQPRDCL operates under SS, is implemented by using only one auxiliary active switch, and so has a simple structure and ease of control. The proposed inverter is analyzed and simulated which is illustrated in Fig.1. The simulation results obtained from the normal PWM inverter were compared with the results obtained from the proposed ACQPRDCL inverter.

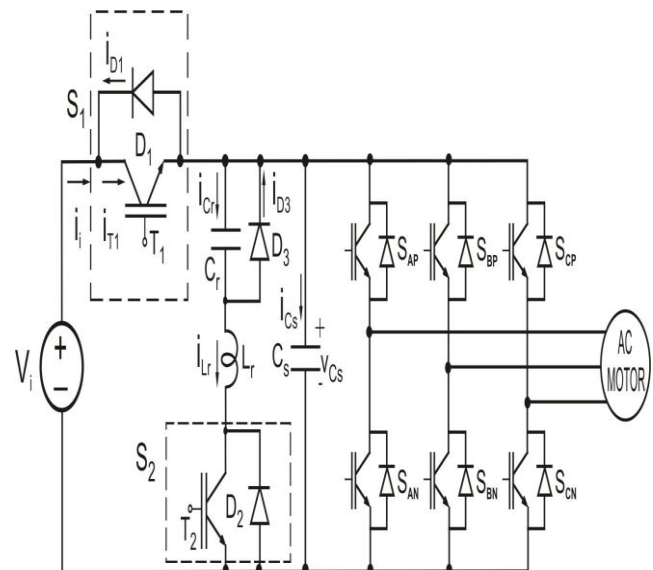


Fig.1 The circuit configuration ACQPRDCL inverter.

II. OPERATION AND ANALYSIS OF THE ACQPRDCL

The proposed ACQPRDCL inverter shown in Fig.2 consist of a dc link switch S_1 , auxiliary switch S_2 , resonant inductor L_r , resonant capacitor C_r . D_F , T_{inv} and I_o are the equivalent elements of the inverter feeding an ac motor as a load. To simplify the analysis, all the components (semiconductor switches, diodes, inductors and capacitors) are assumed ideal.

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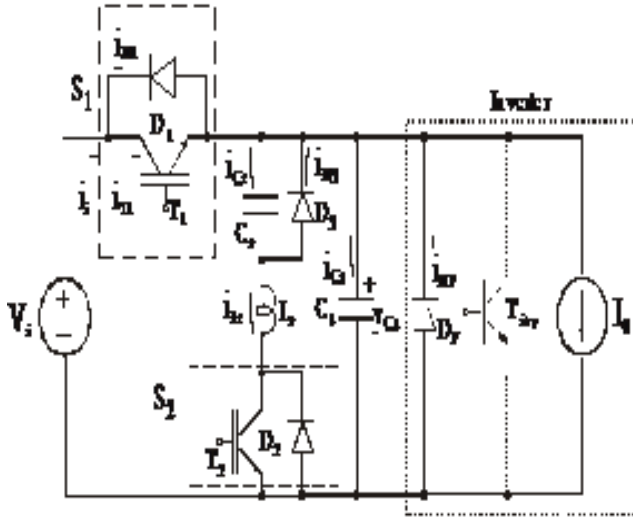


Fig.2 Equivalent circuit of the proposed

ACQPRDCL inverter for explanation of the link operation.

To illustrate the soft switching characteristics of the proposed technique the operation can be divided in to nine operating intervals. The operating waveforms in different intervals of operation are shown in Fig.3.

Interval 1 ($t_0 - t_1$): At $t=t_0$, as the switch T_1 is in the on state and the turn on signal is applied to the gate T_2 and this mode starts. For this mode, the following equations can be written as

$$i_{Lr} = \frac{V_i}{Z_1} \sin(\omega_1(t-t_0)) \quad (1)$$

$$v_{Cr} = -V_i \cos(\omega_1(t-t_0)) + V_i \quad (2)$$

Interval 2 ($t_1 - t_2$): The switch T_1 turned off at the beginning of this mode. A parallel resonance starts via the resonant path $C_r - L_r - T_2 - C_s$. For this resonance

$$i_{Lr} = (I_{Lr1} + \frac{C_e}{C_s} I_0) \cos(\omega_2(t-t_1)) + \frac{V_i - V_{Cr1}}{Z_2} \sin(\omega_2(t-t_1)) - \frac{C_e}{C_s} I_0 \quad (5)$$

$$v_{Cr} = -\frac{C_e}{C_r} [(V_i - V_{Cr1}) \cos(\omega_2(t-t_1)) - Z_2 (I_{Lr1} + \frac{C_e}{C_s} I_0) \sin(\omega_2(t-t_1)) - (V_i - V_{Cr1})] - \frac{I_0}{C_r + C_s} (t-t_1) + V_{Cr1} \quad (6)$$

$$v_{Cs} = \frac{C_e}{C_s} [(V_i - V_{Cr1}) \cos(\omega_2(t-t_1)) - Z_2 (I_{Lr1} + \frac{C_e}{C_s} I_0) \sin(\omega_2(t-t_1)) - (V_i - V_{Cr1})] - \frac{I_0}{C_r + C_s} (t-t_1) + V_i \quad (7)$$

are obtained. In these equations

$$C_e = \frac{C_r C_s}{C_r + C_s} \quad (8)$$

$$\omega_2 = 1/\sqrt{L_r C_e} \quad (9)$$

$$Z_2 = \sqrt{L_r / C_e} \quad (10)$$

are valid. The voltage of the capacitor C_r falls to zero and so the diode D_F starts conducting under ZVS at the end of this interval at t_2 .

Interval 3 ($t_2 - t_3$): At $t=t_2$, as the diode D_F is turned on, a serie resonance starts via $C_r - L_r - T_2$ -DF. For this resonance

$$i_{Lr} = I_{Lr2} \cos(\omega_1(t-t_2)) - \frac{V_{Cr2}}{Z_1} \sin(\omega_1(t-t_2)) \quad (11)$$

$$v_{Cr} = V_{Cr2} \cos(\omega_1(t-t_2)) + Z_1 I_{Lr2} \sin(\omega_1(t-t_2)) \quad (12)$$

are obtained. When the current i_{Lr} of the inductor drops to zero and T_2 is turned off under ZVS and ZCS at t_3 , this mode is finished.

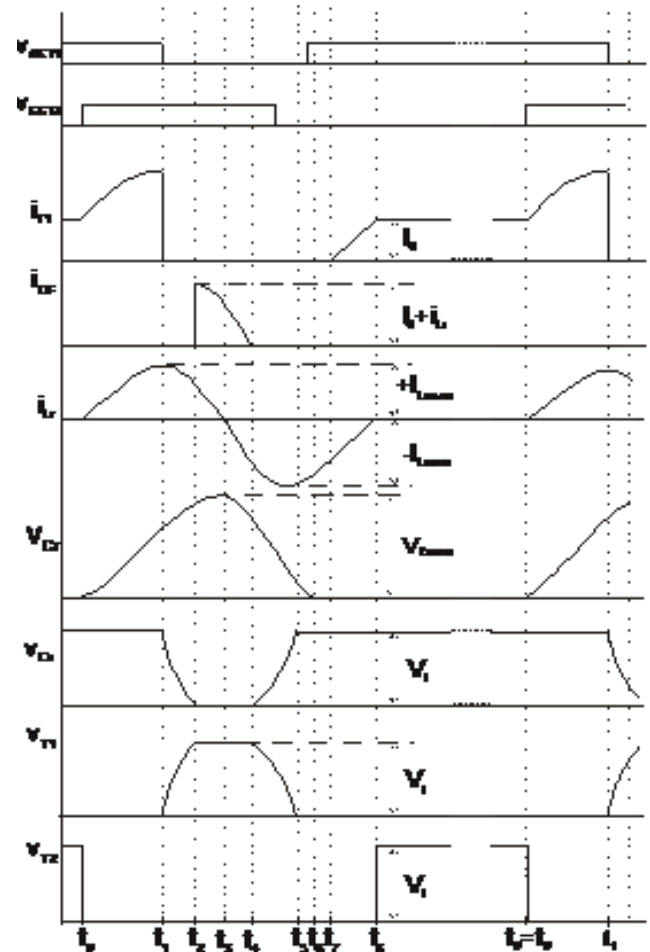


Fig.3 Operating waveforms of the proposed inverter in different intervals of operation.

Interval 4 ($t_3 - t_4$): The diode D_2 is turned on under ZVS. For this interval

$$i_{Lr} = -\frac{V_{Cr3}}{Z_1} \sin(\omega_1(t-t_3)) \quad (13)$$

$$v_{Cr} = V_{Cr3} \cos(\omega_1(t-t_3)) \quad (14)$$

can be written. When the current i_{Lr} of the inductor drops to $-I_0$ and the diode D_F is turned off under ZVS at t_5 , this mode is finished.

Interval 5 ($t_4 - t_5$): At $t=t_5$, as the diode D_F is turned off, a parallel resonance starts via L_r , C_r , C_s , D_2 . For this resonance

$$i_{Lr} = -(1-\frac{C_e}{C_s})I_0 \cos(\omega_2(t-t_4)) - \frac{V_{Cr4}}{Z_2} \sin(\omega_2(t-t_4)) - \frac{C_e}{C_s} I_0 \quad (15)$$

$$v_{Cr} = -\frac{C_e}{C_r} [-V_{Cr4} \cos(\omega_2(t-t_4)) + Z_2(1-\frac{C_e}{C_s})I_0 \sin(\omega_2(t-t_4)) + V_{Cr4}] - \frac{I_0}{C_r + C_s} (t-t_4) + V_{Cr4} \quad (16)$$

$$v_{Cs} = \frac{C_e}{C_s} [-V_{Cr4} \cos(\omega_2(t-t_4)) + Z_2(1-\frac{C_e}{C_s})I_0 \sin(\omega_2(t-t_4)) + V_{Cr4}] - \frac{I_0}{C_r + C_s} (t-t_4) \quad (17)$$

are obtained. When C_s voltage reaches the source voltage V_i at t_5 , the diode D_1 is turned on and this interval stops.

Interval 6 ($t_5 - t_6$): Just after the diode D_1 is turned on at t_6 , a serie resonance starts via L_r , C_r , D_1 , V_i , D_2 . For this stage

$$i_{Lr} = I_{Lr5} \cos(\omega_1(t-t_5)) + \frac{V_i - V_{Cr5}}{Z_1} \sin(\omega_1(t-t_5)) \quad (18)$$

$$v_{Cr} = -(V_i - V_{Cr5}) \cos(\omega_1(t-t_5)) + Z_1 I_{Lr5} \sin(\omega_1(t-t_5)) + V_i \quad (19)$$

are obtained. When the voltage of the capacitor C_r falls to zero and the diode D_3 is turned on under ZVS at t_7 , this interval is finished.

Interval 7 ($t_6 - t_7$): At the beginning of this mode, the diode D_3 is turned on. For this mode

$$i_{Lr} = \frac{V_i}{L_r} (t-t_6) + I_{Lr6} \quad (20)$$

can be written. $i_{Lr} = -I_0$, the diode D_1 is turned off and T_1 is turned on under ZVS, this mode is finished.

Interval 8 ($t_7 - t_8$): At $t = t_7$, T_1 is turned on. For this mode

$$i_{Lr} = \frac{V_i}{L_r} (t-t_7) - I_0 \quad (21)$$

are obtained. When the current i_{Lr} of the inductor drops to zero, the diode D_2 and D_3 are turned off under ZCS, this interval is finished.

Interval 9 ($t_8 - t_9$): During this mode, the load is fed by the dc voltage source via the main transistor T_1 . The duration of this mode is a large part of the switching cycle of the PRDCL circuit. Consequently, one switching cycle is completed and another cycle starts at $t = t_9 = t_0$.

The proposed inverter has the following advantages:

1. All semiconductor devices in the circuit are switched under soft switching. The main switch is turned on and off with ZVS. The auxiliary switch is turned on with ZCS and off with ZVS. The equivalent diode operates under ZVS, and the auxiliary diode is turned on under ZVS and turned off under ZCS.

2. The main switch of this circuit and also all switches of the inverter considered to control are not subjected to any additional voltage stresses. Moreover, the current stresses on the main and auxiliary devices of the circuit are very low.

3. The PRDCL circuit has a more simple structure and more ease of control than most of the similar circuits presented previously. Because the circuit is realized by using only one auxiliary switch, an auxiliary diode, and a resonant inductor and a resonant capacitor.

4. The new PRDCL ensures zero crossing on the DC link voltage at any time and for a time period required for the PWM and SS operation of the inverter, respectively.

5. The circulating energy is quite small and it is slightly dependent on the load current because the fall and the rise of the zero crossing are provided by nearly a quarter resonance.

6. The auxiliary switch and diode devices are subjected to a voltage by nearly twice the input voltage. It can be considered as a drawback of the new circuit.

III. SIMULATION RESULTS

Computer simulation for the ACQPRDCL inverter was conducted with PSPICE. The parameters used in the simulation were $V_i = 250$ V; $L_r = 68\mu\text{H}$; $C_r = 68\text{nF}$; $C_s = 33\text{nF}$. The dc link voltage, resonant inductor current, resonant capacitor voltage and obtained from a PSPICE simulation are presented in Fig.4 (a)-(f). Simulated results were obtained with a load current of about 5 A.



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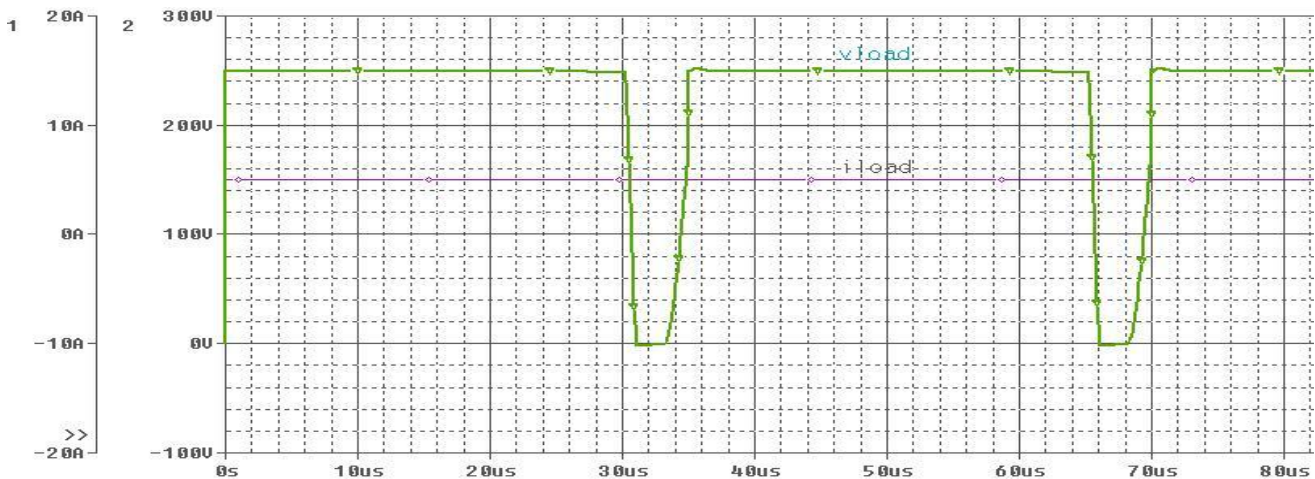
Fig.4(a) shows the dc link voltage input to the inverter can be pulled down to zero and can return to normal dc link voltage quickly as expected. The zero voltage period is short and in the order of the switching times of the inverter. The simulated current in resonant inductor is shown in Fig.4(b). Fig.4(c) shows the resonant capacitor voltage in the quasi-resonant circuit.

Fig.4(d) shows the voltage and current waveforms of the main switch operating at hard switching conditions. From this figure, it can be seen that the main switch is turned on and the main diode is turned off with hard switching simultaneously, and also a short circuit by means of these main devices occurs at the same time. Also, the main switch is turned off with hard switching losses of very high values occur in this hard switching case.

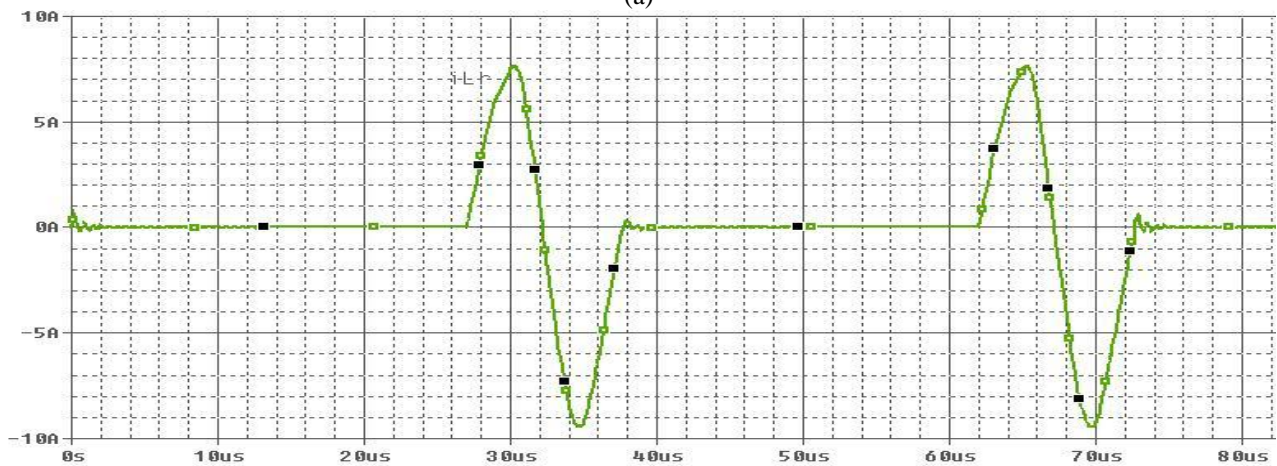
From the voltage and current waveforms of the main switch S_1 given in Fig.4(e) for the soft switching case, it can be seen that S_1 is turned on and off with ZVS through the inductor L_r and the capacitor C_r , and so the switching losses of S_1

are nearly zero. From the voltage and current waveforms of the auxiliary transistor T_2 given in Fig.4(f) for the soft switching, it is clearly seen that T_2 is turned on under ZCS by the inductor L_r and turned off under ZVS by the capacitor C_r , and so the switching losses of T_2 are nearly zero.

Although the peak value of resonant inductor current is greater than the peak load current, the rms value of this current is much lower than that of the load current. The soft switching of the devices in the ACQPRDCL also contributes to low power loss.



(a)



(b)

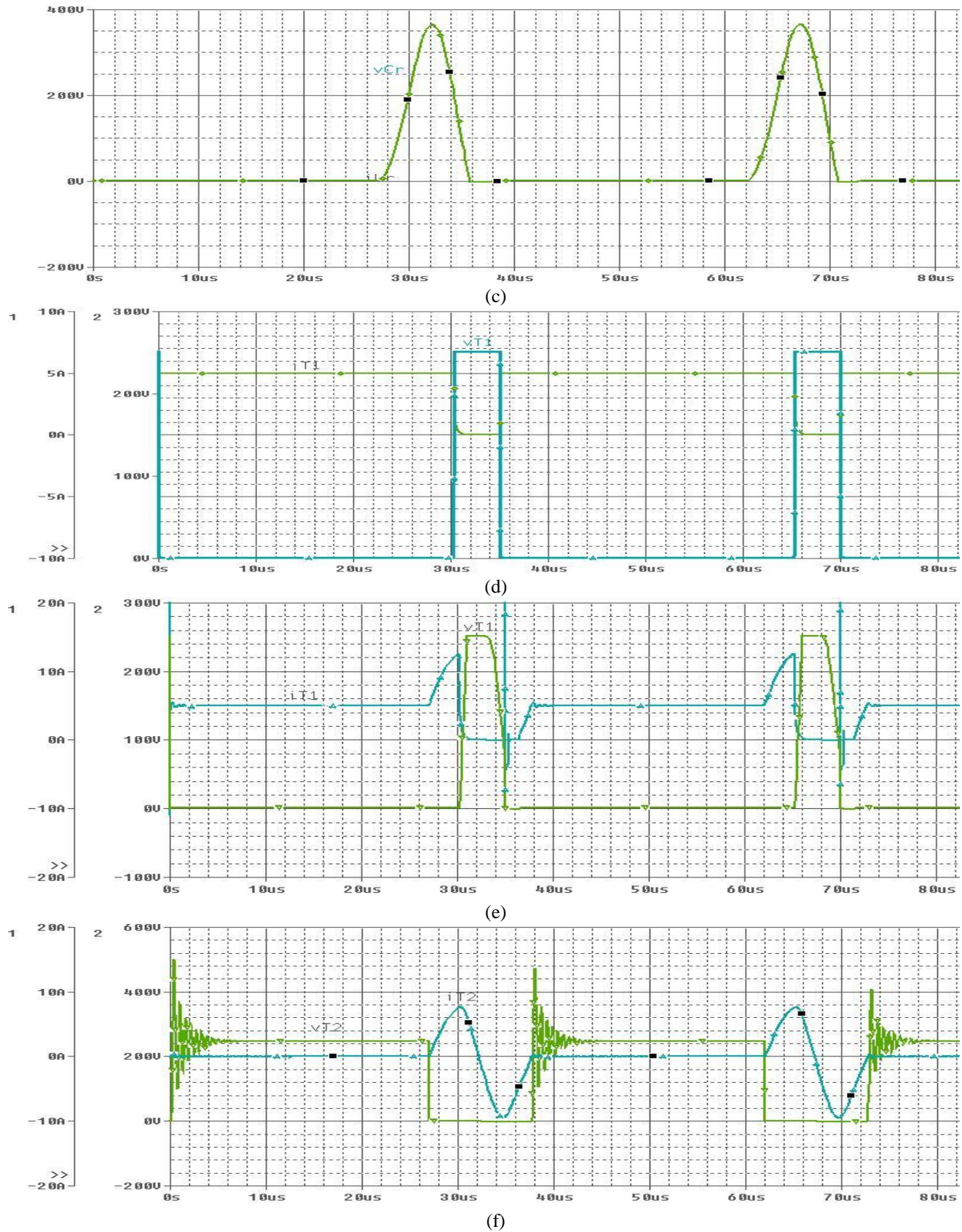


Fig.4 PSPICE simulation of the ACQPRDCL inverter circuit (a) DC link voltage, (b) Current in resonant inductor L_r , (c) Voltage across resonant capacitor C_r , (d) The voltage and current of S1 for hard switching, (e) The voltage and current of S1 for soft switching, (f) The voltage and current of S2 for soft switching

IV. CONCLUSION

In this study, a new ACQPRDCL circuit is presented. This circuit provides zero crossings on the dc link to implement the SS and PWM operation of the inverters. The new circuit combines most desirable features of the circuits presented previously and overcomes most drawbacks of these circuits by using only one auxiliary transistor.

The operating principle of a simple suitable for ZVS inverters has been explained and its operation under different modes analyzed. The proposed ACQPRDCL circuit is simple and has the advantages of minimum voltage stress, snubberless ZVS for inverter switches, and possibility of high frequency operation.

Consequently, new ACQPRDCL circuit was analyzed in detail. It was observed that the theoretical analysis of this circuit was exactly verified by PSPICE simulation of a 1250 W and 50 kHz ACQPRDCL circuit.

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