A Built-in Self-Repair Scheme for Random Access Memories with 2-D Redundancy

K. Bala Souri, K. Hima Bindu, K. V. Ramana Rao

Abstract*— Built-in self-repair (BISR) technique has been widely used to repair embedded random access memories (RAMs). This paper presents a reconfigurable BISR (ReBISR) scheme for repairing RAMs with different sizes and redundancy organizations. An efficient redundancy analysis algorithm is proposed to allocate redundancies of defective RAMs. In the ReBISR, a reconfigurable built-in redundancy analysis (ReBIRA) circuit is designed to perform the redundancy algorithm for various RAMs. Also, an adaptively reconfigurable fusing methodology is proposed to reduce the repair setup time when the RAMs are operated in normal mode. Experimental results show that the ReBISR scheme can achieve high repair rate (i.e., the ratio of the number of repaired RAMs to the number of defective RAMs). The area cost of the ReBISR is very small, which is only about 2.7% for four RAMs (one 4 Kbit RAM, one 16 Kbit RAM, one 128 Kbit RAM, and one 512 Kbit RAM). Moreover, the time overhead of redundancy analysis is very small. Embedded memories are among the most widely used cores in current system-on-chip (SOC) implementations. Memory cores usually occupy a significant portion of the chip area, and dominate the manufacturing yield of the chip. Efficient yield-enhancement techniques for embedded memories thus are important for SOC. In this paper we present a built-in self-repair (BISR) scheme for semiconductor memories with 2-D redundancy structures. The BISR design is composed of a built-in self-test (BIST) module and a built-in redundancy analysis (BIRA) module. Our BIST circuit supports three test modes: the 1) main memory testing, 2) spare memory testing, and 3) repair modes. The BIRA module executes the proposed redundancy analysis (RA) algorithm for RAM with a 2-D redundancy structure, i.e., spare rows and spare columns.

Keywords: Built-in self-test, built-in self-repair, built-in redundancy-analysis, memory testing, semiconductor memory.

I. INTRODUCTION

Memories are key components of a typical system-onchip (SOC). They normally are dense and covers a large portion of the chip area, thus dominate the yield of the chip. Keeping the memory cores at a reasonable yield level is thus vital for SOC products. For such purpose, memory designers usually employ redundancy repair—using, e.g., spare rows and/or spare columns of cells—to improve the yield [1–4]. However, redundancy increases silicon area and thus has a negative impact on yield. To maximize the yield with a reasonable cost, redundancy analysis (RA) is necessary. Conventionally, RA is performed on the host computer of the automatic test equipment (ATE) if it is an on-line process, or on a separate computer if it is an offline process. Either way it is time consuming since RA algorithms are complicated and the memories that implement redundancies are usually large. Moreover, embedded memories are harder to deal with using ATE, and few believe that any known ATE architecture can accurately test tomorrow's system chips for the demanded yield and reliability[5]. The defective cells detected by the BIST circuit are replaced by the cells of the spare SRAM. The built-in selfdiagnosis method presented for repairable SRAMs uses a reduced-instruction-set processor to determine a repair solution. In addition to the complicated processor, it requires a large fault-free RAMblocks to store the fail bitmap. In a BISR scheme for ultra-large capacity memory chips is proposed. The proposed memory architecture has a hierarchical organization that optimizes memory access time and increases the efficiency of test and repair. The authors describe a power-on (soft) BISR design for embedded high density SRAMs with only spare columns. The design can detect defective memory cells and map sparememory cells to functionally replace the defective cells. Because the 1-D redundancy is implemented, the RA algorithm is simple and straightforward. If the RAM has a 2- D redundancy (with spare rows and columns), the optimal redundancy allocation problem becomes NP-complete. A heuristic RA algorithm and its realization are reported and where the RA algorithm provides about 83.3% repair rate (the ratio of the number of repaired memories to the number of defective memories) for a bit RAM with redundancies (i.e., 2 spare rows and 2 spare columns). In Alpha 21264, a redundancy analyzer for a RAM core with redundancies per memory block was implemented. Embeded random access memory (RAM) is one key component in modern complex system-on-chip (SOC) designs. Typically, many RAMs with various sizes are included in an SOC, and they occupy a significant portion of the chip area. Furthermore, RAMs are subject to aggressive design rules, such that they are more prone to manufacturing defects. That is RAMs have more serious problems of yield and reliability than any other embedded cores in an SOC.Keeping theRAMcores at a reasonable yield level is thus vital for SOC products. Built-in self-repair (BISR) technique has been shown to improve the RAM yield efficiently.

However, RAMs in an SOC usually have various sizes, different numbers of redundancies, and even different types of redundancy organizations. If each repairable RAM uses one self-contained BISR circuit, then the area cost of BISR circuits in an SOC becomes high. This results in converse effect in the yield of RAMs.

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K.Bala Souri, M.Tech(ECE), Pydah College of Engineering & Technology, India. e-mail: kbsjob@gmail.com

K.Hima Bindu, M.Tech(ECE), Pydah College of Engineering & Technology, India.

K.V. Ramana Rao, Assoc.Professor & Head, Dept. of ECE, Pydah College of Engineering & Technology, India.

To reduce the area cost, several processor-based BISR schemes have been reported. In these BISR schemes, a BISR circuit can repair multiple RAMs. However, a processor-based BISR scheme uses specific instructions to construct the redundancy analysis algorithm. This results in long redundancy analysis time, since a statement of the redundancy analysis algorithm may need multiple instructions to realize it. Therefore, a time-efficient and area-efficient BISR scheme is needed to improve the yield of RAMs in SOCs economically. After the BISR circuit completes the test/repair process of a defective RAM, an electrically programmable fuse macro enables the on-chip self-reconfiguration process for skipping defective elements of the RAM operated in normal mode. Various implementations of fuse macros have been proposed Typically, multiple RAMs of an SOC share a fuse macro to store the repair signatures of the RAMs. Once the power of the SOC is turned on, the repair signatures are serially shifted to the individual repair register of each RAM. The loading time of the repair signatures is called the repair setup time of the RAMs. The repair setup time determines how long the RAMs in an SOC can be switched to the normal operation mode after the power of the SOC is turned on. Thus, reducing the repair setup time can shorten the boost time of the system.

II. TYPICAL MEMORY BISR ARCHITECTURE

Fig. 1 shows the block diagram of a typical BISR scheme for a RAM, which consists of four major components. 1) *Repairable RAM*. A RAM with redundancies and reconfiguration circuit.

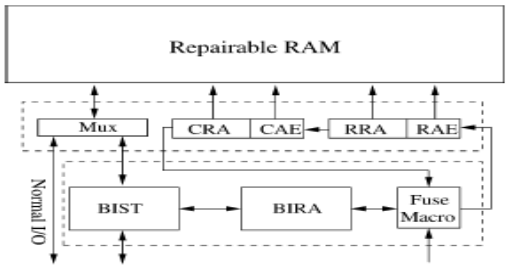

Fig. 1. Typical BISR scheme for embedded RAMs.

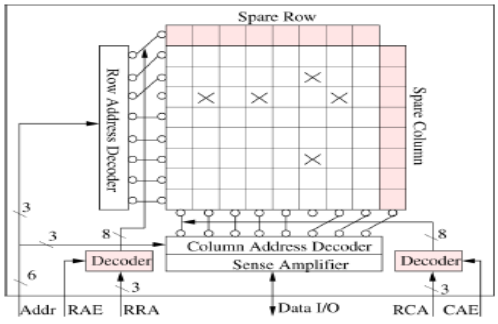

Fig. 2. Conceptual diagram of an 8□8 bit-oriented repairable

RAM with one spare row and one spare column.

Fig. 2 depicts an example of an 8 8 bit-oriented RAM with 1 spare row and 1 spare column. If a spare row is allocated to replace a defective row, then the row address of the defective row is called row repair address (RRA). Then a decoder decodes the RRA into control signals for switching row multiplexers to skip the defective row if the row address enable (RAE) signal is asserted. The reconfiguration of the defective column and the spare column is performed in a similar way, i.e., give a column repair addresses (CRA) and assert the column address enable signal to repair the defective column using the spare column. 2) Built-in Self-Test (BIST) Circuit. It can generate test patterns for RAMs under test. While a fault in a defective RAM is detected by the BIST circuit, the faulty information is sent to the BIRA circuit. 3) BIRA Circuit. It collects the faulty information sent from the BIST circuit and allocates redundancies according to the collected faulty information using the implemented redundancy analysis algorithm. 4) Fuse Macro. It stores repair signatures of RAMs under test. The fuses of the fuse box can be implemented in different technologies, e.g., laserblown fuses, electronic-programmable fuses, etc. The fuse register is the transportation interface between the fuse box and the repair register in the repairable RAM. If a fault is detected, then the fault information is stored in the BIRA circuit. Then, the BIRA circuit allocates redundancies to replace defective elements. As soon as the repair process is completed, the repair signatures are blown in the fuse box. Subsequently, the repair signatures are loaded into the fuse register first and then are shifted to the repair registers (i.e., registers in the wrappers for storing RRA, RAE, CRA, and CAE data) in normal operation mode. Finally, the repairable RAM can be operated correctly.

2.1. BISR Architecture and Procedure

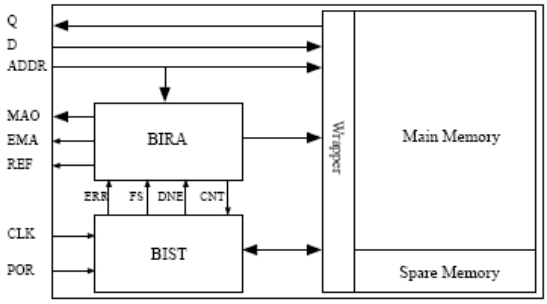

Figure 2. Block diagram of the proposed BISR scheme.

Figure 2 depicts the block diagram of the proposed BISR scheme, including the BIST module, BIRA module, and test wrapper for the memory. The BIST circuit detects the faults in the main memory and spare memory. It is programmable at the March element level [6]. The BIRA circuit performs redundancy allocation using the proposed RA algorithm (to be discussed later). The test wrapper switches the memory between the test/repair mode and normal mode. In the test/repair mode the memory is accessed by the BIST module, while in the normal mode the wrapper selects the data outputs either from the main memory or the spare memory (replacing the faulty memory cells) depending on the control signals from the BIRA module.

The BISR procedure is shown in Fig. 3. Upon turning on the power, the BIST module starts to test the spare memory. Once a fault is detected, it informs the BIRA module to mark the defective spare row or column as faulty through the error (ERR) and fault syndrome (FS) signals. After finishing the spare memory test, it tests the main memory. If a fault is detected (ERR outputs a pulse), the test process pauses and the BIST module exports the FS to the BIRA module, which then performs the RA procedure.

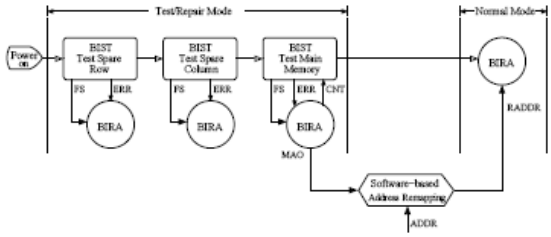

Figure 3. Power-on BISR procedure.

When the procedure is completed and the memory testing is not finished yet, the BIRA module issues a continue signal (CNT) to resume the test process. During the RA procedure, if a spare row is requested but there is no more spare row, the BIRA module exports the faulty row address through the EMA (export mask address) and MAO (mask address output) signals. The memory will then be operated at a down-graded mode (i.e., with a smaller usable capacity) by software-based address remapping. For example, assume that a memory with multiple blocks is used for buffering, and the blocks are chained by pointers. If some block is faulty and should be masked, then the pointers are updated to invalidate the block. The size of the memory is reduced, as one block is removed. The system still works if a smaller buffer is allowed, though the performance may be affected. This approach effectively increases the yield of the products. The number of blocks that can be invalidated normally depends on the performance penalty that can be tolerated. If the down-grade mode is not allowed, the MAO is removed and the EMA indicates whether the memory is repairable.

When the main memory test and RA are finished, the REF (repair end flag) signal goes high and the BIRA module switches to the normal mode. The BIRA module then serves as the address remapper, and the memory can be accessed using the original address (ADDR). When the memory is accessed, ADDR is compared with the fault addresses stored in the BIRA module. If ADDR is the same as any of the fault address, the BIRA module controls the wrapper to remap the access to the spare memory.

III. CONCLUSION

We have proposed a BISR scheme for RAM. The BISR circuit is composed of a BIST module and a BIRA module. The BIST circuit supports three operation modes— main memories testing, spare memory testing, and repair. The BIRA circuit executes a proposed RA algorithm for 2- D redundancy—spare rows and spare columns. The spare columns are grouped and segmented. A software-based address remapping (masking) is performed in the downgraded operation mode, where certain amount of un-repairable faulty rows can be tolerated. The experimental results show that high repair rate can be obtained. Compared with the conventional approach (without grouping and segmentation) using exhaustive search, the proposed scheme outperforms in many instances and can be implemented with low area cost. A BISR design for an industrial 8K_64 SRAM with 4 spare rows and 2 spare column groups has also been implemented. In this case, full repair can be achieved if the number of random faults is no more than 10. Moreover, the area overhead of the BISR design is low—about only 4.6% for the 8K_64 SRAM.

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AUTHORS PROFILE

K. Bala Souri pursuing his M.Tech(ECE) in Pydah College of Engineering & Technology, under the guidence of K.V Ramana Assoc.Professor & Head, Dept.of ECE at Pydah College of Engineering & Technology, Visakhapatnam, A.P., India. My research interest includes VLSI Design and Digital Signal Processing.

K. Hima Bindu pursuing her M.Tech(ECE) in Pydah College of Engineering & Technology, under the guidence of K.V Ramana Assoc.Professor & Head, Dept.of ECE at Pydah College of Engineering & Technology, Visakhapatnam, A.P., India. My research interest includes VLSI Design and Digital Signal Processing and Instrumentaton.

Sri K.V. Ramana Rao working as Assoc. Professor & Head, Department of ECE at Pydah College of Engineering & Technology, Visakhapatnam, A.P., India. His research interest includes Digital Signal Processing and VLSI Design.