Design of Fault Tolerant Reversible Multiplier

H. P. Sinha, Nidhi Syal

Abstract— In the recent years, reversible logic has emerged as a promising technology having its applications in low power CMOS, quantum computing, nanotechnology, and optical computing. The classical set of gates such as AND, OR, and EXOR are not reversible. This paper proposes a novel 4x4 bit reversible fault tolerant multiplier circuit which can multiply two 4-bit numbers. It is faster and has lower hardware complexity compared to the existing designs. In addition, the proposed reversible multiplier is better than the existing counterparts in terms of delay & power. It is based on two concepts. The partial products can be generated in parallel using Fredkin gates and thereafter the addition is done by using reversible parallel adder designed from IG gates. Thus, this paper provides the initial threshold to building of more complex system which can execute more complicated operations using reversible logic.

Index Terms—Reversible logic, Parity, Fredkin gate, IG gate, Constants, Garbage, Delay.

I. INTRODUCTION

Power dissipation is one of the important parameters in the digital circuit design. In VLSI circuit designing where power dissipation plays an important role, there has been an increasing trend of packing more and more logic elements into smaller and smaller volumes and clocking them with higher frequencies. The logic elements are normally irreversible in nature and according to Landauer's principle [1] irreversible logic computation results in energy dissipation due to power loss. This is because; erasure of each bit of information dissipates at least KTln2 Joules of energy where K is Boltzamann's constant and T is the absolute temperature at which the operation is performed. By 2020 this will become a substantial part of energy dissipation, if Moore's law continues to be in effect which states that processing power will double every 18 months. This particular problem of VLSI designing was realized by Feynman and Bennet in 1970s. In 1973 Bennet [2] had shown that energy dissipation problem of VLSI circuits can be circumvented by using reversible logic. This is so because reversible computation does not require erasing any bit of information and consequently it does not dissipate any energy for computation. Reversible computation requires reversible logic circuits and synthesis of reversible logic circuits differs significantly from its irreversible counter part because of different factors [3]. The technological requirement of designing of energy dissipation free VLSI circuits, particular characteristics of synthesis and testing of reversible circuits

and the tremendous advantage of quantum circuits have motivated scientists and engineers from various background (eg. Physics, Electronics, Computer science, Mathematics, Material science, Chemistry) to study various aspects of reversible circuits. But from the construction point of view classical reversible gates are easy to build [4, 5]. A lot of interesting works are already reported in literature in the field of synthesis [6-10], optimization [11], evaluation [12] and testing [13] of reversible circuits. In a short period the reversible computation has emerged as a promising technology having applications in low power CMOS [14], nanotechnology [15], optical computing [16], optical information processing, DNA computing [17], bioinformatics, digital signal processing and quantum computing. It is very clear that reversible circuits will play dominant role in future technologies. These facts motivated many researchers to work in this domain. A reversible logic gate must have the same number of inputs and outputs, and for each input pattern there must be a unique output pattern. Thus, Reversible logic circuits avoid energy loss by uncomputing the computed information by recycling the energy in the system [18]. In the design of reversible circuits two restrictions should be considered [19]; firstly, Fan-out is not permitted and secondly, Feedback from gate outputs to inputs is not permitted. Due to these restrictions, synthesis of reversible circuits can be carried out from the inputs towards the outputs and vice versa [20]. So, there is a one-to-one mapping between input and output vector. In an n-output reversible gate, the output vectors are permutations of the numbers 0 to 2n - 1.

A logic synthesis technique using a reversible gate should have the features like minimum gate count along with less use of constants and garbage generation. Reduction of these parameters is the main design focus. Reversible circuits for different purposes like half adder, full adder [23-26], multiplier [27-29] have been proposed recently. Among these reversible circuits, multiplier circuits are of special importance because of the fact that they are the integral components of every computer system, cellular phone and most digital audio/video devices. It is important for every processor to have a high speed multiplier. Multiplier circuits essentially have two components: partial product generation and parallel full adder. Several 4x4 reversible gates (e.g. TSG [24], MKG [25], HNG [26] and PFAG [30]) have been used in reversible multiplier designing to construct the full adder. Since the design is focused on implementing reversible fault tolerant multiplier so proper selection of gate which must have not only reversible property but also be fault tolerant is necessary.

However, two major constraints in reversible logic are to minimize the number of constant input and garbage output. The extra input that is added to make function reversible is called constant input [21] whereas extra output that is not necessary for further computations is called garbage output [22].

II. BASIC REVERSIBLE LOGIC GATES

A. Reversible Gates

There exist many reversible gates in the literature. Among them 2*2 Feynman gate (FG) [34], depicted in Fig. 1 (a), 3*3 Peres gate (PG) [35], depicted in Fig. 1 (b), 3*3 Toffoli gate (TG) [33], depicted in Fig. 1 (c) and 3*3 Fredkin gate (FRG) [34], depicted in Fig. 1 (d) have been studied extensively. Because of their simplicity and low cost there are design approaches and tools that incorporate them separately or in combination with each other [31], [33].
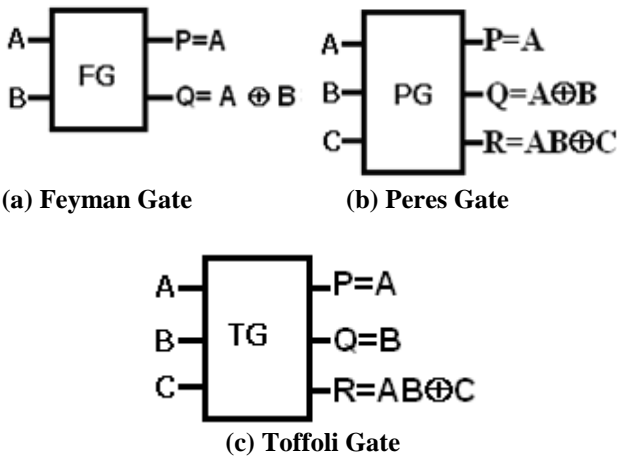

(a) Feyman Gate   **(b) Peres Gate**

(c) Toffoli Gate
Fig. 1 Basic Reversible Gates

B. Parity Preserving fault tolerant Reversible Gates

Fault tolerance is the property that enables a system to continue operating properly in the event of the failure of some its components. If the system itself made of fault tolerant components, then the detection and correction of faults become easier and simple. In communication and many other systems, fault tolerance is achieved by parity. Therefore, parity preserving reversible circuits will be the future design trends to the development of fault tolerant reversible systems in nanotechnology. And a gating network will be parity preserving if its individual gate is parity preserving [32].
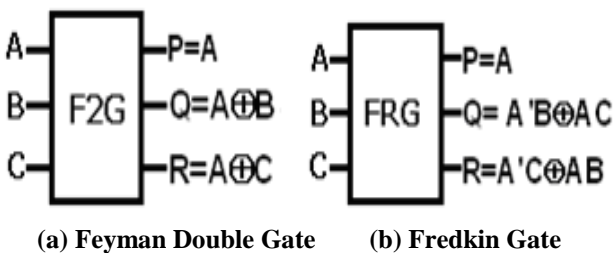
(a) Feyman Double Gate   **(b) Fredkin Gate**
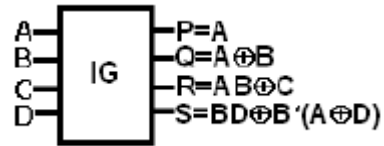
(c) IG Gate
Fig. 2 Basic Parity preserving reversible Gates

A few parity preserving logic gates have been proposed in the literature. Among them 3*3 Feynman Double gate (F2G) [32] depicted in Fig. 2 (a), 3*3 Fredkin gate (FRG) [36] depicted in Fig. 2 (b) and IG gate [37] depicted in Fig. 2 (c) are one-through gates, which means one of the inputs is also output. From Table 1 and 2, it can be seen that the gates F2G, FRG and IG gates are parity preserving since they satisfy $A \oplus B \oplus C = P \oplus Q \oplus R$. And any k*k reversible logic gate where the EX-OR of the inputs matches the EX-OR of the outputs will be parity preserving.

Table1. Truth Table of Parity Preserving Feyman Double Gate (F2G)

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Table2. Truth Table of Parity Preserving Fredkin Gate (FRG)

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Table3. Truth Table of Parity Preserving IG Gate (IG)

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	1	0	1
1	0	0	1	1	1	0	0
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0

1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	0
1	1	1	1	1	0	0	1

III. PROPOSED WORK

The design of the proposed multiplier is based on parallel operation is done using two steps.

Part I: Partial Product Generation (PPG)

Part II: Reversible Fault Tolerant Parallel Adder (RFTPA)

As mentioned before, the purpose of this paper is the design of reversible fault tolerant multiplier circuit with the aim of optimizing its hardware complexity to make it more economical in terms of number of garbage outputs and constant inputs without losing its efficiency. The proposed multiplier is implemented using Fredkin and IG gates. The operation of a 4*4 reversible multiplier is shown in Fig. 3. It consists of 16 Partial product bits of the four bit inputs X and Y to perform 4 * 4 multiplications.

Fig. 3 Working of the 4×4 parallel multiplier

A. Partial Product Generation (PPG)

For product term generation the FRG gate is used. The FRG gate is used to perform AND operation by forcing one constant input as logic 0 whereas it produces required product term along with two garbage outputs. The Fig. 4 shows the implementation of AND operation using FRG.
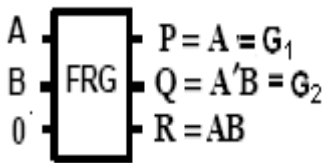

Fig. 4 FRG as AND gate

Multiplier partial products are generated in parallel using 16 Fredkin gates (FRG) as shown in Fig. 5. This uses 16 FRG is a better circuit as it has less hardware complexity compared to other gates and moreover it posses parity preserving logic.

B. Reversible Fault Tolerant Parallel Adder (RFTPA)

The RFTPA circuit needs reversible fault tolerant full adder (FTFA) and half adder (FTHA). Many reversible full adders have been proposed in the past. For example, TSG, MKG and HNG gates can singly perform the full adder operation. Design of multipliers with these gates indicates the different critical parameters for reversible multipliers. Experimental results of different reversible multiplier circuits in terms of speed, number of garbage outputs and constant inputs show that multiplier circuits with adders designed using IG gates have better results than multiplier circuits with MKG or TSG gates.
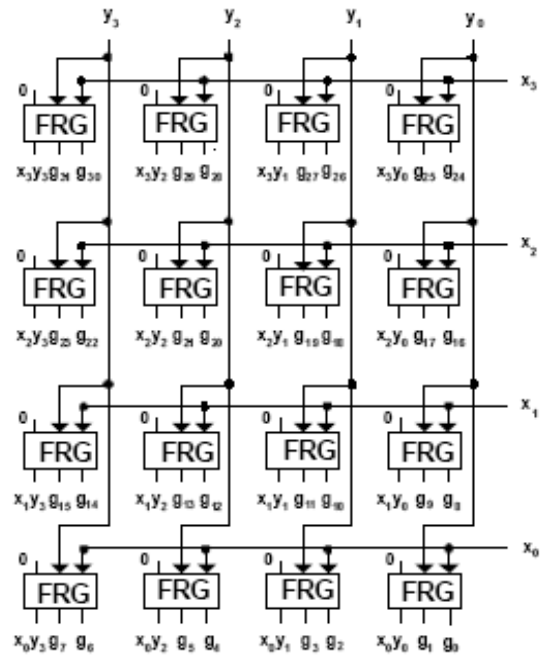

Fig. 5 Partial Product generation circuit using Peres gates

IG gate used as half adder is shown in Fig. 6. It requires two constant inputs of logic 0 and produces the required sum and carry term with two garbage outputs. It can also be further extended to implement full adder circuit which requires two constant inputs of logic 0 and gives three garbage values. The full adder implementation using IG gate is shown in Fig. 7.
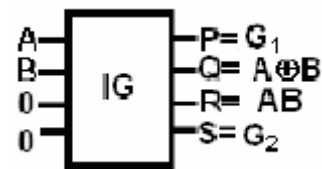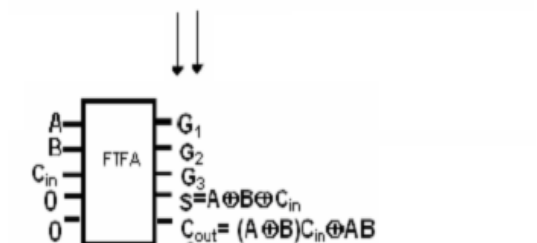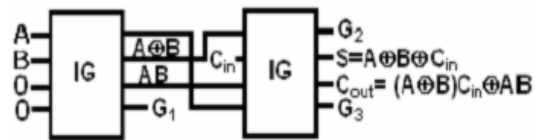

Fig. 6 IG as Half Adder (FTHA)

Fig. 7 IG as Full Tolerant Full Adder (FTFA)

The circuit of proposed RFTPA is shown in Fig. 8. It requires four IG gate as FTHA for half adder and eight FTFA for full adder logic implementation.
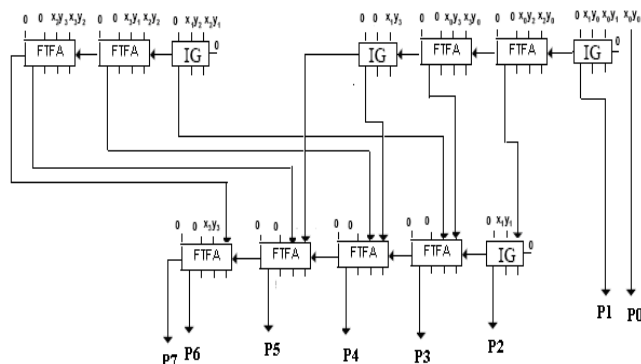

Fig. 8 RFTPA circuit for adding PPG of Proposed Multiplier

IV. RESULT AND DISCUSSION

The entire architecture is modeled using VHSIC hardware description language (VHDL). The coding is done on Xilinx ISE8.2i on Spartan 3E using target device: 3s500efg320-4 at speed grade of -4. For simulation purpose the Modelsim6.2h has been used. The simulation result for proposed multiplier is shown in Fig. 9. The proposed multiplier is efficient in terms of number of reversible gates and delay compared to existing multipliers which are only reversible in nature. The worst case delay is 19.1nS (52.7% logic, 47.3% route).
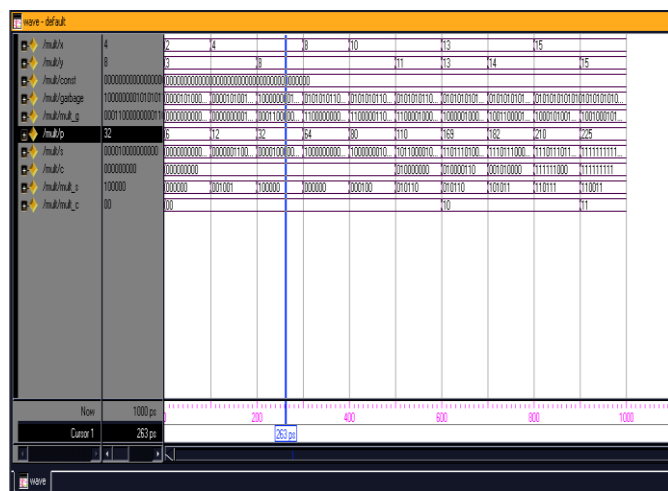

Fig. 9 Simulation result of Proposed Multiplier

Table 1: Comparison Table for 4*4 Multiplier

Performance Parameter Spartan 3E	Reversible Multiplier TSG (2006)	Reversible Multiplier MKG (2008)	Proposed Fault Tolerant Reversible Multiplier
Gate Count	53	52	44
Constant input	58	56	56
Garbage	58	56	56

No. of IO's	132	128	128

V. CONCLUSION

Multiplier is a basic arithmetic cell in computer arithmetic units. The energy consumption in computation turns out to be deeply linked to the reversibility of the computation. The primary objective of this paper was to gain insight into the Reversible Computation and its use for making circuits energy efficient for long life. In the proposed work, we synthesized a parity preserving reversible multiplier circuit with the help of existing fault tolerant Fredkin and IG gate. The comparison between the proposed multiplier and those of the previous multiplier showed that the proposed work is better in few aspects and can be encouraged due to its additional feature of fault detection technique. Thus, our proposed parity-preserving multiplier circuit can be used in designing fault tolerant reversible complex circuits like ALU. Using such circuit can be helpful not in terms of power saving but also acts as high speed multiplier for dedicated hardware. The prospect for further research includes the reversible implementation of more complex arithmetic circuits such as function evaluation and multiplicative division circuits using this multiplier.

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