

Voltage Balancing in SVM Controlled Diode Clamped Multilevel Inverter for Adjustable Drives

P. S. Anish, S. Ramarajan, T. Arun Srinivas, M. Sasikumar

Abstract— The work describes a transformer less medium voltage adjustable-speed induction motor drive consisting of two back-to-back connected five-level diode-clamped converters. Due to the feedback from the load to the dc link nodes, there is a chance of voltage imbalance. In this paper the methods for voltage balancing are discussed and simulated. The usage of switching techniques to employ voltage balancing rather than the external circuitry is being discussed. Proper switching results in the control of average current through the nodes and hence the non symmetrical charging and discharging of the dc split capacitors can be avoided. The first phase of work explains the output using the multicarrier pulse width modulation technique and the second phase deals with the modification done using the Space vector Pulse Width Modulation (SVPWM) technique. Voltage balancing is achieved with lesser harmonic content while using the SVPWM technique.

Index Terms— Medium-voltage drives, multilevel inverters, Space vector modulation, voltage balancing.

I. INTRODUCTION

In a medium voltage drive system for driving an AC motor the method used was to use a step down transformer in the input side. This was the case when power electronic devices were of less power handling capacity. But as the technology advanced to high rated power electronic devices, the use of transformer came in a spot of bother. If the transformer is avoided from the design, losses can be reduced to a large extend. Thus the innovation of new high rated power electronic devices led to the concept of transformer less medium voltage drives. For controlling an AC motor, the method employed is a combination of rectifier and inverter. The converter topology used is a Voltage Source Converter (VSC). In a VSC, even if high rated semiconductor devices are used, the rating may not be sufficient to withstand the high voltage from the input. This can be avoided by using multilevel topology in both the rectifier and the inverter section. The first method was to use the offset voltage injection so that the capacitor voltage can

be balanced [6]. But this method gives a notable delay in making the capacitors balanced. Another method is to use more sophisticated switching methods. This was done by Pulse Width Modulation (PWM) techniques. Multicarrier PWM can give more stability to capacitor voltage [2]. The work includes the use of Space Vector Modulation technique for the proper switching of the semiconductor devices so that voltage balancing can be achieved easily and rapidly. The harmonic levels are compared and the use of this method is justified using MATLAB / SIMULINK results.

II. DESIGN CONCEPT OF THE TRANSFORMERLESS MOTOR DRIVE SYSTEM

A. Five-Level Diode-Clamped PWM Rectifier and Inverter

The prototype of the 11kV industrial application is the main purpose of this paper. For experiment sake the rating is reduced to 230 V from the kV range [4]. The input is directly given to the multilevel rectifier section. The need for the multilevel in the input side is to reduce the input current ripple in the supply. If a normal multi pulse rectifier is used for removing the harmonics, two phase shift transformers have to be used. This again increases the cost and weight already reduced by removing the input transformer. The weight can be reduced to a large extend. The weight of the transformer and the inverter rectifier combination is about 5000 kg and the transformerless system can be designed with 2000 kg in the industrial applications. Hence the proposed method is cost efficient. Again the multilevel inverter section used here is five level. Also the switching control is easy when using the same configuration [6]. Only requirement then will be to make the sum of the firing angles to be complementary.

The circuit explained is an application of multilevel inverters namely back to back connection of multilevel inverters. The advantage is the easiest design of the control signals since the firing pulses are complementary.

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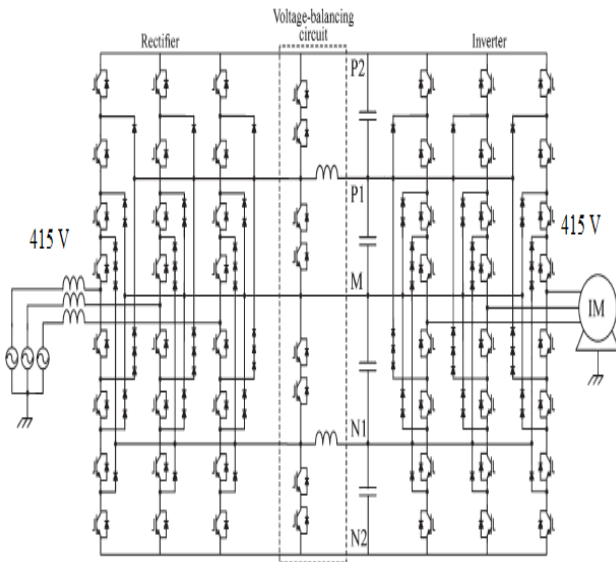


Fig 1.back to back connection of diode clamped converters with voltage balancing circuit

B. Voltage-Balancing Control of the Four Split DC Capacitors

The main draw back in using dc capacitors for multilevel inverter operation is the voltage imbalance in the capacitor voltages. The four series-connected dc capacitors sitting between the rectifier and the inverter has the following five node points in the common dc link: the outer positive point P2, the inner positive point P1, the midpoint M, the inner negative point N1, and the outer negative point N2, as shown in Fig. 1. Whenever the motor is operated either in powering or regenerative mode, an amount of dc current would flow into, or out of, the two inner points P1 and N1. This brings voltage imbalance to the four capacitors unless special care was taken of voltage balancing [5].

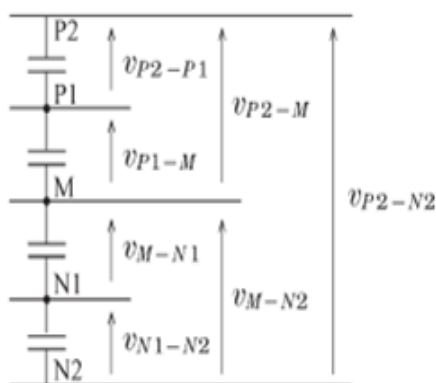


Fig. 2 DC-link voltage and split dc-capacitor voltages.

Existing solutions to the voltage imbalance inherent in the motor drive system can be classified into the following two groups: one is based on sophisticated switching control [2] and the other is based on additional hardware installation

[2]. The former is more preferable in cost than the second one. The authors of [1] have proposed a practical switching-angle control method for staircase modulation or the so-called that is designed, constructed, and tested in this paper. Fig. 2 shows the dc-link voltage and the individual split dc-capacitor voltages.

III. DC LINK VOLTAGE CONTROL

The DC link voltage in the system of discussion is the dc voltage obtained from the rectifier section. This DC voltage is supposed to be aligned itself in such a way that the voltage level across each of the dc capacitors should be the same. When the load used is having no feedback signals this condition is well met. But in the proposed system, the load used is an induction motor [7]. The back emf that is fed back to the system will cause the weak nodes of the dc link to be discharged to zero. Discharge of the dc link capacitor causes the levels of the multilevel inverter to be reduced to three whatever be the design. This can be avoided by using the average current control in the nodes. The voltage in a node is directly related to the average current flowing through the node. The average current of each node is directly related to the $\cos \beta$, $\cos \alpha_1$ and $\cos \alpha_2$.

In the context of the work

$\cos \beta$ – power factor

α_1 – firing angle of the rectifier section

α_2 – firing angle of the inverter section

I_{max} – peak current value

The relation is as follows:

Let the average currents be I_{avg1} and I_{avg2} .

$$I_{avg1} = (I_{max} / \pi) \cos \beta \cos \alpha_2 \tag{1}$$

Similarly the average current of second node

$$I_{avg2} = (I_{max} / \pi) \cos \beta (\cos \alpha_1 - \cos \alpha_2) \tag{2}$$

Thus the average current and hence the dc link voltage can be controlled by controlling the firing angle. The firing angle control can be done by controlling the switching frequency. This can be done by various PWM techniques and the technique used in this work is multicarrier pulse width modulation and Space Vector PWM. SVPWM is more advanced and sophisticated technique to the conventional multicarrier pulse width modulation technique.

IV. CIRCUIT OPERATION

The circuit given in the fig 1 is an ac-dc-ac converter. The first half input is a three phase ac which is being rectified before the capacitor is being fed. The dc split capacitors are used to split the rectified dc to be divided equally among them. This split dc is fed to the inverter section. The similar circuit used in this section acts as an inverter due to the reversal of the firing angle of

the switches. This can be done either by using hardware or by switching techniques. The hardware section can be designed using a bidirectional buck boost converter. This circuit is shown in the circuit diagram. The working is like the buck mode is activated when the particular capacitor voltage exceeds a limit and the boost mode is activated when the capacitor discharges completely. This can ensure perfect voltage balancing across the dc split capacitors. This costs more due to the need of external hardware implementation. This cost can be avoided by using control techniques for the switches. Now we can discuss about the source of voltage imbalance.

In the concerned work the output levels expected is five. The entire circuit acts as an ac-dc-ac converter. The output can be fed either to an ac motor load or to the grid. In either of the cases there is a feedback supply being fed back to the dc link nodes. Due to this supply there is a chance of the inner node capacitors to charge or discharge completely. This normally occurs in the inner node since the outer nodes are more or less stable to the variations in the feedback signals. The feedback from a motor load is due to the back emf created by the ac motor used and in the case of grid it is due to the reactive or active power exchange included for the compensation sake. Now that the voltage unbalance occurs remedy has to be done by proper current control of the nodes. From equations (1) and (2) it is clear that the control can be done by controlling the firing angles of the inverter and rectifier sections.

Now discussing the switching techniques used.

V. MULTICARRIER PULSE WIDTH MODULATION

In ordinary pulse width modulation, the reference signal is compared with the message signal both one in number. The design is such that when the amplitude of the message signal is more a high pulse is generated which is used to trigger the corresponding switch. In the multicarrier pulse width modulation technique, a combination of carrier signals is used with same frequency but different clamped levels. So simultaneous comparison is done and the combined output is obtained.

Since three phase simulation is the purpose of the project, three separate control blocks are required for each phase. Hence the message signal of each control block is delayed by an angle of 120 degrees.

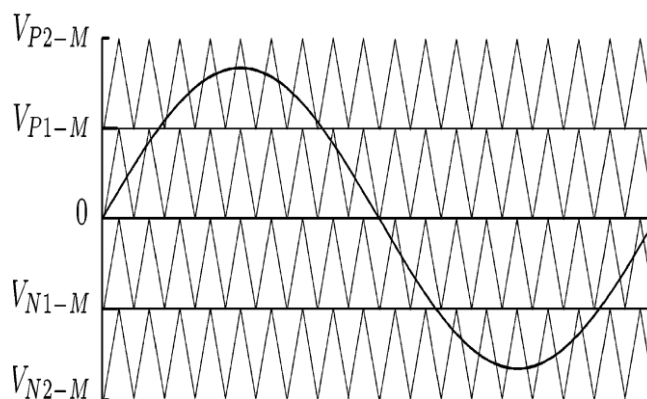


Fig 3. Multicarrier pulse width modulation for a five level inverter

VI. SPACE VECTOR PWM

This project instigates four space vector modulation algorithms – conventional with active vectors placed in the middle of the half-cycle of the carrier and the 30°, 60°, and 120° discontinuous modulation algorithms. Theory tells us to expect the conventional SVM to outperform the discontinuous modulation algorithms with respect to unwanted harmonic content and ripple. One may question the use of discontinuous modulation when faced with this fact. The reason to use discontinuous modulation is to decrease the switching losses through the transistors by periodically clamping one of the three phases to a rail to produce a zero vector. The decrease in switching losses associated with discontinuous modulation allows the system to utilize a higher carrier / switching frequency. However, this analysis only uses one carrier frequency, $f_c = 15$ kHz. The carrier frequency governs the period in which modulation / switching of the inverter gates occurs. We want the amplitude of our stator voltage, V_s , to be $460 \cdot \sqrt{2/3}$ V_{in} on each phase for rated operation. This means by virtue of the inverter circuit and space vector modulation theory that the DC input to the inverter must be

$$V_{in} = V_s \frac{3}{2} \frac{1}{\sin(\pi/3)} \quad (3)$$

VII. RESULTS AND DISCUSSION

The output is simulated and the graphs are recorded. The motor used for the simulation is a 3 hp induction motor which is having a speed of 3000 rpm. The speed was set to be 1500 rpm. The current harmonics are determined up to 7 levels and the values are tabulated. The values were found to be less when space vector modulation was used.

The output of the motor is adjusted by designing the space vector modulation. The harmonic values are as follows.



Order	2 nd	3 rd	4 th	5 th	6 th	7 th
%	0.54	0.16	0.07	0.67	0.11	0.19

Table 1. THD values for SVPWM

The simulated circuit is given below. The load used is a 3hp 200V induction motor. The capacitor voltages were measured and found to be balanced. Each capacitor gives an voltage of 100V each. The output voltage and current were measured. The motor load connected was an induction motor. Since the experiment is to design a prototype, the motor used is of low power rating.

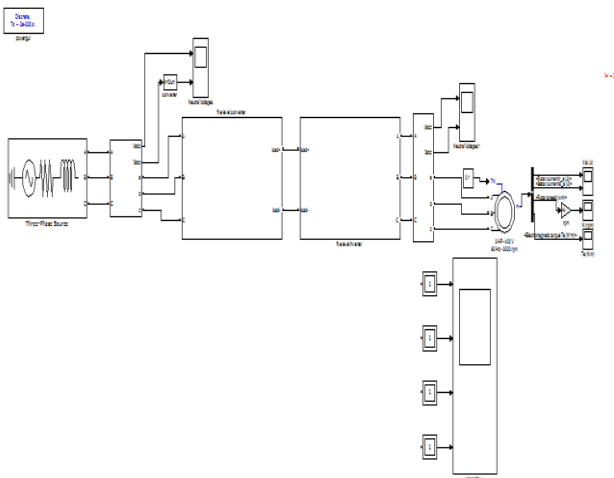


Fig 4. Simulated circuit

The harmonic value was reduced when the space vector modulation was used. The motor current harmonic was 3.9% which is under the acceptable range.

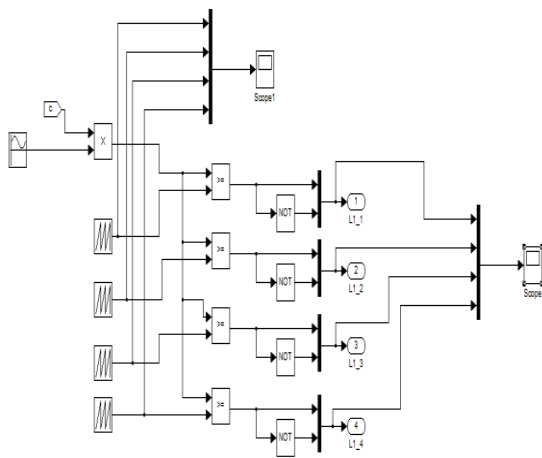


Fig 5. Multicarrier pulse generation circuit

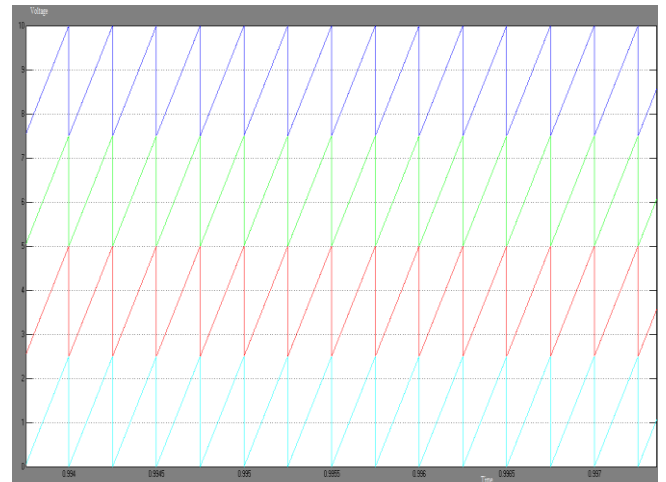


Fig 6. Multicarrier signal

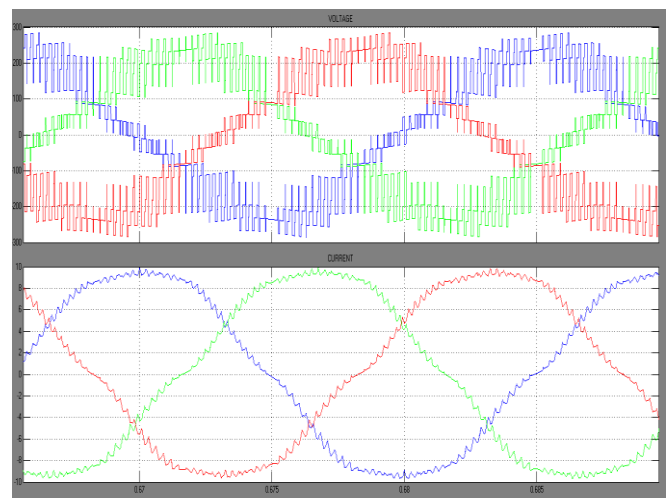


Fig 7. Multicarrier PWM output voltage and current

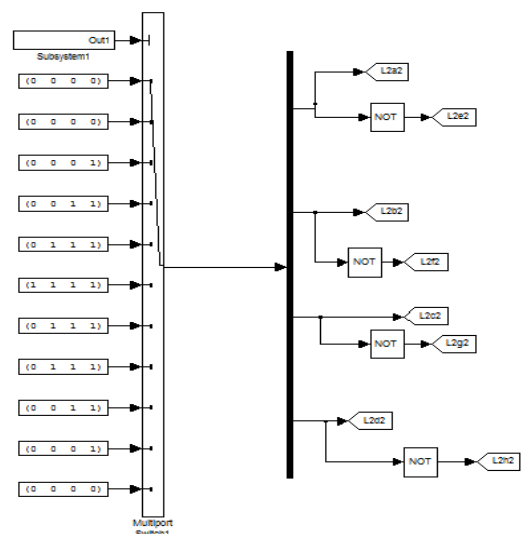


Fig 8. SVPWM Implementation

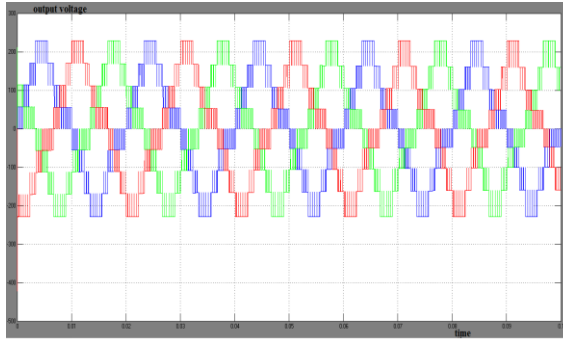


Fig 9. SVPWM output voltage

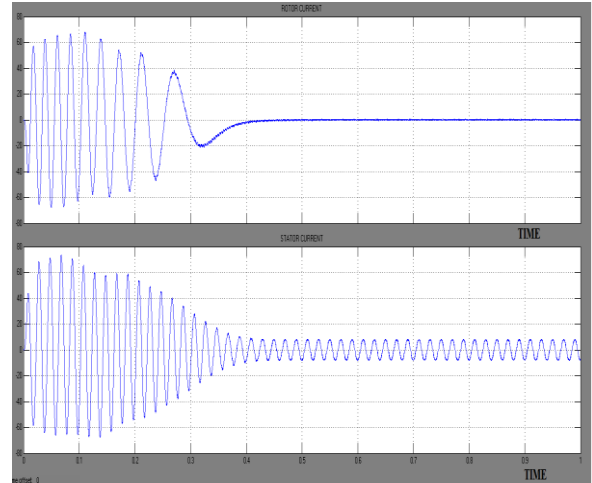


Fig 11. Stator and rotor current

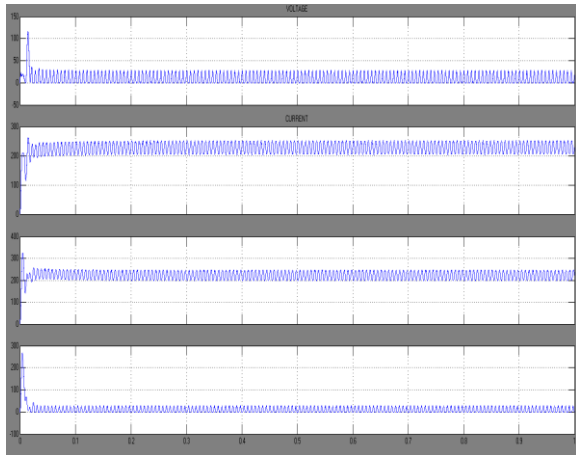


Fig 10. Unbalanced capacitor voltages

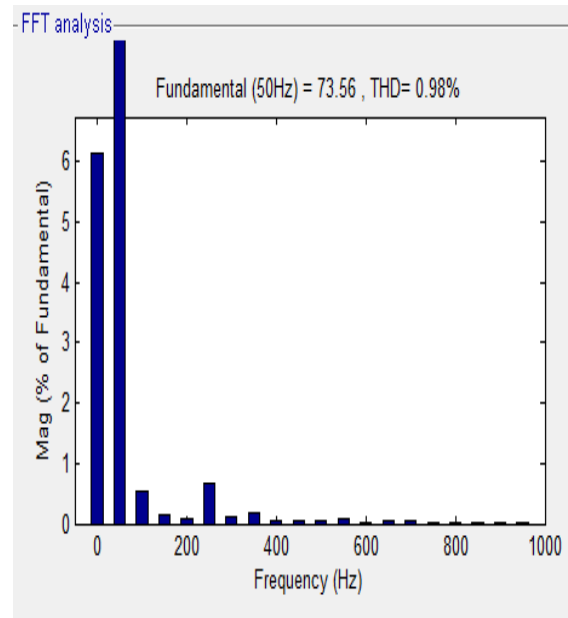


Fig 12. Output THD analysis for SVPWM

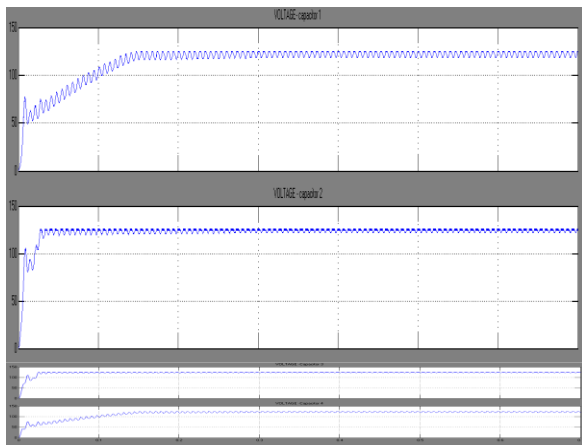


Fig 10. Balanced capacitor voltages

Order	2 nd	3 rd	4 th	5 th	6 th	7 th
%	4.89	6.03	3.11	0.98	0.34	0.79

Table 2. THD values for multicarrier PWM

The THD value obtained from the rotor output is 0.98 % which is well below the accepted level. The listed values are given in table 1. The rotor speed is set at 1500 rpm. This can be varied by varying the switching frequency. By increasing the firing angle, the voltage can be reduced and hence the speed can also be reduced. Thus by this method the motor can be made to work



both in the fixed speed as well as the variable speed.

VIII. CONCLUSION

This paper consists of the work done for controlling an ac motor. This is an extension work of the harmonic reduction using more sophisticated switching techniques. Voltage balancing and harmonic reduction are achieved while using SVPWM ahead of multicarrier pulse width modulation. Three phase simulation is done and the outputs for both switching techniques are shown. The observation is that the output is more accurate and THD reduced while using the SVPWM technique. The THD values reduced from 5% to 0.98 % while the switching technique was changed from multicarrier pulse width modulation to Space vector pulse width modulation.

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