

Design of CNTFET-Based Inverter Inspired BiCMOS Technology

Hossein Etemadi, Morvarid F. Dabiri, Peiman Keshavarzian, Tahere Panahi

Abstract— In this paper we present a new combination of Carbon NanoTube Field Effect Transistors (CNTFETs) and bipolar transistors which named Bi CNTFET and used to design a fast and low power inverter. New inverter proposes and compare to existing Bipolar-CMOS (BiCMOS) design. Propose Bi CNTFET inverter has advantages such as large load drive capabilities, low static power dissipation, fast switching and high input impedance. Extensive simulation using HSPICE to investigate the power consumption and delay of propose inverter. Simulation result shows that the propose inverter using carbon nanotube has better performance in terms of delay and power consumption, in compared to BiCMOS counterpart. Furthermore the new design reduces the chip area because of using carbon nanotubes.

Index Terms—CNTFET, Nanoelectronic, Bi-CNTFET.

I. INTRODUCTION

BiCMOS technologies have been largely used due to combines Bipolar and CMOS transistors onto a single integrated circuit, for example it use for memories and VLSI's design because of their high speed and capacitive load driving, low power consumption and noise protection. [1, 2]. Via this knowledge, a designer can makes best use of a high speed bipolar and high density and low delay in CNTFET for a memory devices and signal processor. Lot of investigators has been working on low voltage BiCMOS technique and also CNTFETs. In this work we use the CNTFET to improve the performance of the appropriate circuit design. Bipolar and combination is a promising alternative to the conventional BiCMOS design because of low delay and the reduction in chip area. However, complexity and scalability of manufacture process are major challenges of BiCMOS circuits. Nanoscaled CNTFETs are promising for high-performance due to near-ballistic transport and low OFF-current properties [3-5]. Furthermore using CNTFET improves the BiCMOS scalability issue. Therefore we use the CNTFET to implement a new inverter design which consumes low power and delay compared to BiCMOS design. HSPICE simulation has performed to

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Comparison the BiCMOS and Bi CNTFET inverter in terms of delay and power consumption. Simulation results are shown that the in Section 5, impact of load variation is given in section 6, finally conclusion is given in section 7.

Bi CNTFET design has a better performance in compared to BiCMOS implementation.

Description of the Nanotube transistor is in part 2, Simulation results are show in section 3, previous design is in part 4, and the performance of propose circuit is shown i

II. NANOTUBE TRANSISTORS

Initial tests showed that the Single Wall Nanotube transistor (SWNT) behavior is similar to a conventional semiconductor transistor, however some differences are important, such as one dimensional Carbon nanotubes, which greatly reduces the scattering probability; thus, CNT may operate in the ballistic regime [6,7]. The nanotube conducts mainly on surface of the nanotube where all chemical bonds are saturated and stabled; therefore, without careful passivation interface between the nanotube channel and the gate dielectric, for example there isn't any equivalent interface silicon dioxide or silicon. Finally Schottky barrier with the metallic nanotubes is the dynamic switching component in inherent nanotube devices [8]. The dimensional characteristics of a CNT transistor are unique.

Fig.1 shows the typical CNTFET device, the distance between two centers of the connecting nanotube channels under the gate of a CNTFET is named a pitch that significantly affects the width of the transistor gate and contacts [9].

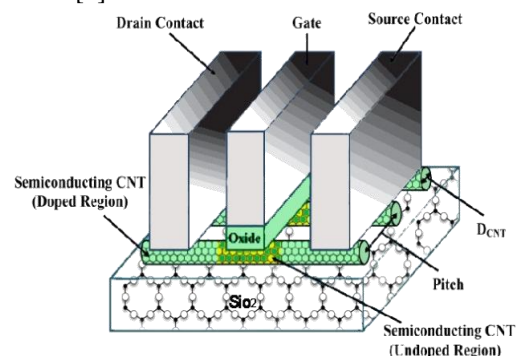


Fig1.schematic diagram of a CNT transistor

The width of gate is presented in the following equation (Eq.1).

$$W_{gate} \approx \text{Min}(W_{min}, N \text{ Pitch}) \quad \text{Equation (1)}$$

W_{min} is the lowest width of the gate and N is the number of nanotubes under the gate.

Properties of I - V CNTFET is shown in Fig.2. The CNTFETs have the same behavior as the MOSFET. CNTFET current at higher voltage saturated along increases length of channel, and also it decrease ON-current because of energy quantization in the axial direction gate length (Fig. 2), [12].

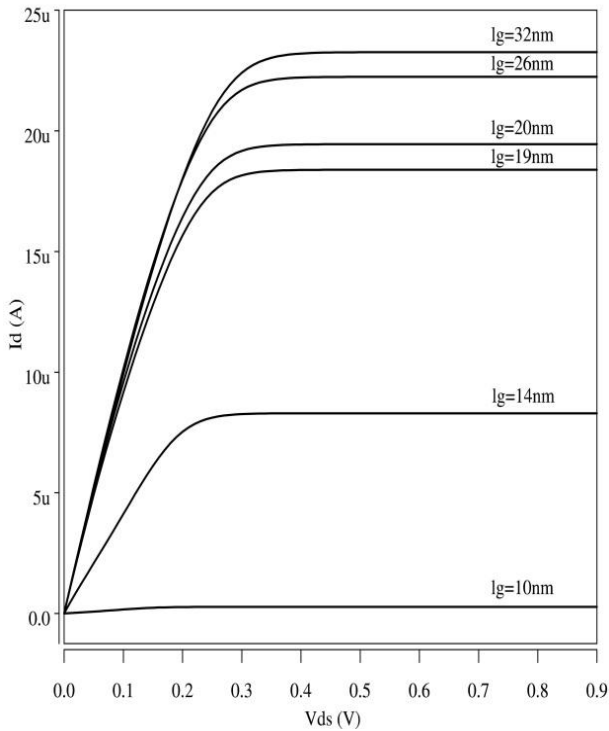


Fig. 2. I-V features of a ballistic CNTFET.

Intrinsic CNT channel voltage can be achieved as the following equation (Eq.2).

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3} aV\pi}{3 eD_{CNT}} \quad \text{Equation (2)}$$

The threshold voltage has been defined as the voltage requirements to turn on the transistor, where $a = 2.49 \text{ \AA}$ is the carbon to carbon atom distance, $V = 3.033\text{eV}$ is the carbon bond energy in the tight bonding model, e is the unit electron charge and the diameter of CNT is D_{CNT} [10-12].

III. SIMULATION RESULTS ANALYSIS AND COMPARISON

In this part, a comprehensive plan assessment in different Compare with other situations in classical and state of the art CMOS and CNTFET-based BiCMOS.

Synopsys HSPICE Simulator simulates the design using with 32nm CMOS technology for CMOS circuits and the SPICE model for circuit based CNTFET, including all nonidealities [10,11], and SPICE models for circuit-based CNTFET.

The standard models for monopoles, MOSFET, such as the CNTFET device is designed, each transistor have one or more CNT.

This model examines the effect of Schottky Barrier, Parasitic, including CNT, Source/Drain, Gate resistors and capacitors, also CNT Charge Screening effects.

CNTFET model parameters and their values, with a brief description, are shown in Table 1. [12]

Table 1. CNTFET Model Parameter

Parameter	Description	Value
L_{ch}	Physical channel length	32e-9
L_{gef}	The mean free path in the intrinsic CNT channel	100e-9
L_{ss}	The length of doped CNT source-side extension region	32e-9
L_{dd}	The length of doped CNT drain-side extension region	32e-9
K_{gate}	The dielectric constant of high-k top gate dielectric material	16
T_{ox}	The thickness of high-k top gate dielectric material	4e-9
C_{sub}	The coupling capacitance between the channel region and the substrate	40e-12

Average power consumption over a long period of time consider as power consumption. All combination of inputs is checked and delay measurements for the maximum delay are reported. Circuit performance can be measured by power delay product (PDP) and the worst case delay. PDP manufacture a trade-off between speed and power consumption [13]. Simulations have been done at room temperature (25°C) at 0.5 V supply voltages and operating frequency is 100 MHz.

IV. CONVENTIONAL BICMOS INVERTER CIRCUIT

Conventional BiCMOS inverter circuit is shown in Fig 3. When V_{in} is equal to zero then M1 transistor is turn ON then both M2 and M3 transistors are OFF. Turn ON the M1 and turn OFF the M3 provide Q1 base Current and turn it ON. In the other side turning OFF the M2, makes no current reaches to Q2 Base, at the same time the M4 can discharge the electron charges in the Q2 base in a very short time.

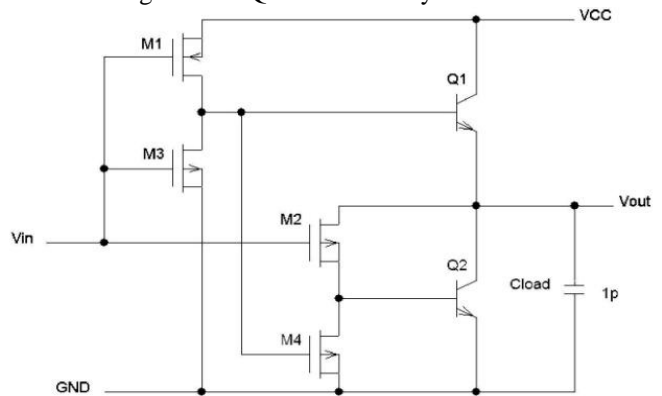


Fig 3. Schematic diagram of conventional BiCMOS inverter



Therefore, great current (I_{EQ1}) completely charge Cloud capacitor. The gate delay propagation from low to high voltage will be low. When V_{in} is equal to V_{cc} , the M is turn OFF then both M2 and M3 are On. Turning ON the M3 makes the voltage Gate of M4 being equal to zero therefore it will be OFF. High voltage of V_{out} and turning ON the M2 then turning OFF the M4 supply the current base of the Q2 and turn it ON. Finally, Cloud capacitor via the Q2 transistor and great current (I_{CQ2}) can be discharged quickly. Figure 4 Shows output voltage per input pulse. The output is not full swing because when the Q1 is ON and capacitor is charging, the output voltage is equal to $V_{CC}-V_{BE}$ and while the Q2 is ON and capacitor is discharging the output is equal to V_{BE} .

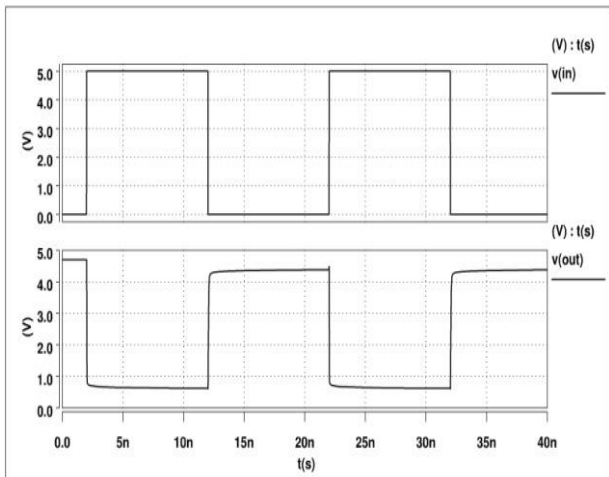


Fig 4. Transient response of BiCMOS inverter

V. PROPOSED BI CNTFET INVERTER

The proposed Bi CNTFET inverter circuit is shown in Fig 5.

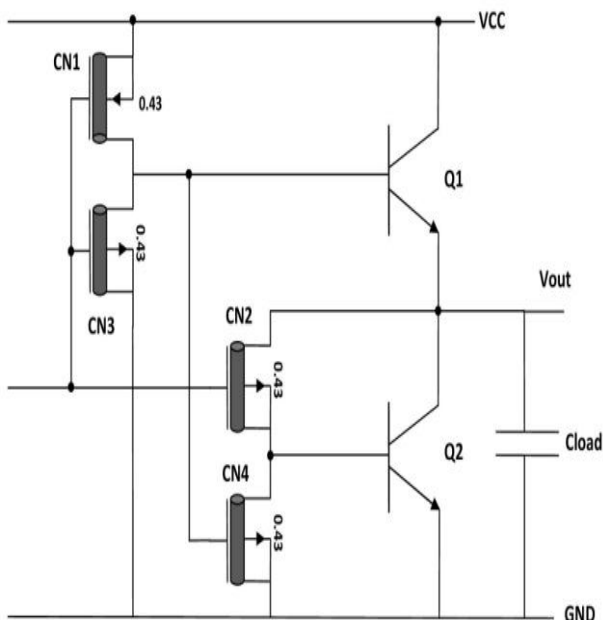


Fig 5. Schematic diagram of proposed Bi CNTFET inverter

This circuit is similar to its counterpart's BiCMOS performance; however in the Bi CNTFET inverter due to using of the CNTFET transistors, switching speed is high and power consumption is less, Moreover, the chip area is reduced

significantly. Figure 6 shows transient input and output of the Bi CNTFET inverter.

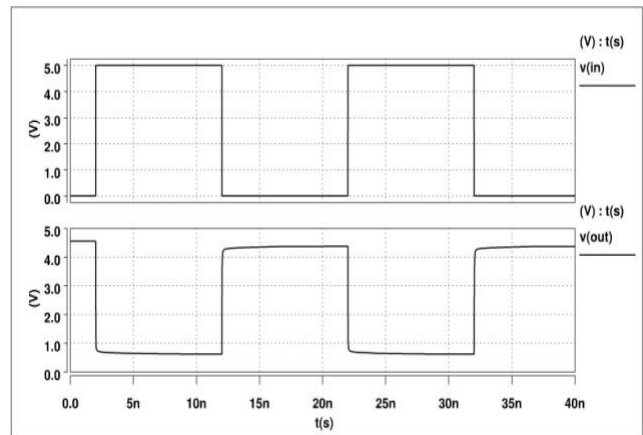


Fig 6. Transient response of Bi CNTFET inverter

Power, delay and Power Delay Product (PDP) of BiCMOS inverter with its counterpart is shown in Table 2.

Table2. Transient result of BiCMOS and Bi CNTFET inverter

Design	Delay	Power	PDP
BiCMOS	36.012E-12	1.1502E-03	4.1422E-14
Bi CNTFET	12.803E-12	9.4891E-04	1.2149E-14

Simulation results are shown that a proposed Bi CNTFET inverter have better performance in terms of power consumption and also delay than the Bi CNTFET inverter.

VI. IMPACT OF LOAD VARIATION

The propagation delay is depending on the charge and discharge of capacitance load. Delay of circuit increases while Cloud increment. Extensive simulation has performed to scrutiny of load variation on inverters delay. The delay for both BiCMOS and Bi CNTFET inverter is shown in figure7.

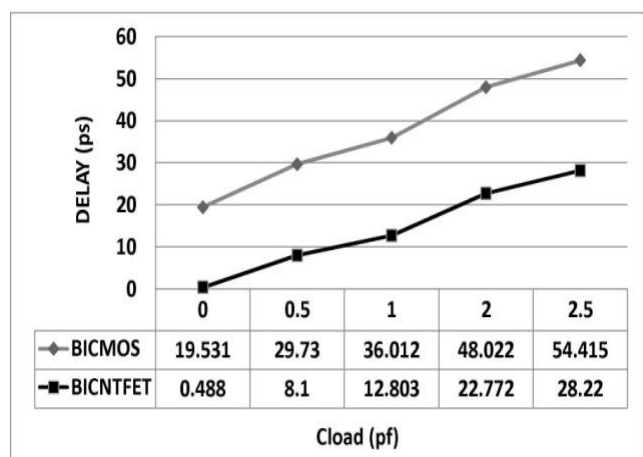


Fig 7. Delay-load curve for both designs

For each C_{load} of the Bi CNTFET design we have lower delay than the BiCMOS design.

VII. CONCLUSION

This work proposes a new design of BiCMOS inverter with Carbon Nanotube Field-Effect Transistor. Simulation results have presented in normal condition that the Bi CNTFET has a significant improvement up to 300% in power and delay. The comparative results have been done by HSPICE. It is quite appropriate for today integration circuit, thus this paper technique warrants minimal structure with high power consumption and speed.

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