Design and Comparison of Multipliers using Different Logic Styles

Aditya Kumar Singh, Bishnu Prasad De, Santanu Maity

Abstract— Low power VLSI circuits have become important criteria for designing the energy efficient electronic designs for high performance and portable devices .The multipliers are the main key structure for designing an energy efficient processor where a multiplier design decides the digital signal processors efficiency. In this paper, 4*4 unsigned Array and Tree multiplier architecture is being designed by using 1-bit full adders and AND2 function following various logic styles. The full adders and AND2 function have been designed using various logic styles following a unique pattern of structure to improve their performance in various means like less transistors, low power, minimal delay, and increased power delay product. The various types of adders used in our paper are complementary MOS (CMOS) logic style, complementary pass-transistor (CPL) logic style and double-pass transistor (DPL) logic style. The main objective of our work is to calculate the average power, delay and power delay product of 4*4 bit multipliers following various logic styles at 5v supply voltage at 25c temperature with 0.15um technology and simulating them with T-spice of Tanner EDA tool. An multiplier architecture is designed using full adder, half adder structure and AND2 function and then the above said various logic style adders and AND2 function are replaced in the multiplier architecture and then their outputs are generated, such that their average power, delay, and power delay product are calculated.

Keywords— Array Multipliers, Tree multiplier, Full adder, CMOS, CPL, DPL, power delay product.

I. INTRODUCTION

In the past, the parameters like high speed, small area and low cost were the major areas of concern, whereas power considerations are now gaining the attention of the scientific community associated with VLSI design [1]. In recent years, the increase of personal computing devices and wireless communication systems has made power dissipation a most critical design parameter. In the absence of low-power design techniques such applications generally suffer from very short battery life, while packaging and cooling them would be very difficult and this is leading to an unavoidable increase in the cost of the product. In multiplication, reliability is strongly affected by power consumption. Usually, high power dissipation implies high temperature operation, which, in turn, has a tendency to induce several failure mechanisms in the system. Power dissipation is the most critical parameter for portability & mobility and it is classified in to dynamic and static power dissipation. Dynamic power dissipation arises when the circuit is operational, while static power dissipation becomes an issue when the circuit is inactive or is in a power-down mode. There are three major sources of power dissipation in digital CMOS circuits, which are summarized in equation (1) [2]:

$$P_{avg} = P_{switching} + P_{short\text{-}circuit} + P_{leakage}$$

$$= \alpha_{0\to1} \times C_L \times V_{dd}^2 \times f_{clk} + I_{sc} \times V_{dd} + I_{leakage} \times V_{dd} \quad (1)$$

The first term represents the switching component of power, where load capacitance is C_L, f_{clk} is the clock frequency and α is the probability that a power consuming transition occurs (the activity factor). In second term direct-path short circuit current, I_{sc} arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current, which can arise from substrate injection and sub-threshold effects, is primarily determined by fabrication technology considerations

The switching power dissipation is a strong function of the power supply voltage in CMOS digital ICs. Therefore, reduction of emerges as a very effective means of limiting the power consumption. However, the saving in power dissipation comes at a significant cost in terms of increased circuit delay. Since the exact analysis of propagation delay is quite complex, a simple first order derivation [3] can be used to show the relation between power supply and delay time

$$T_d = C_L V_{dd} \; / \; K(V_{dd} - V_{th})^{\alpha} \quad (2)$$

K – Transistor's aspect ratio (W /L)

V_{th}- Transistor threshold voltage

α - Velocity saturation index which varies between 1 and 2

Unfortunately, reducing the supply voltage reduces power, but when the supply voltage is near to threshold voltage (from equation 2), the delay increases drastically [4].

Section II gives a short introduction to the most important existing static logic styles and compares them qualitatively. Section III gives the two important multiplier architectures, designed in this paper and output waveform are generated and displayed. Results of quantitative comparisons based on simulations of different multiplier architectures by using different logic design styles are given in Section IV. Some conclusions and references are finally drawn in Section V and VI respectively.

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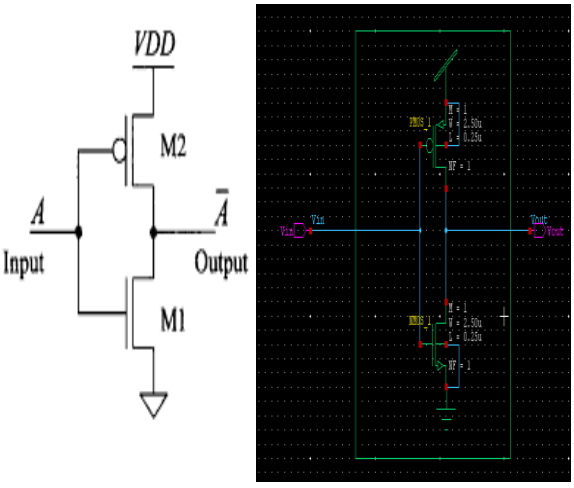
II. LOGIC DESIGN STYLES

The increasing demand for low-power VLSI can be addressed at different steps of VLSI design cycle, such as the architectural, circuit, layout, and the process technology step. At the circuit design step, considerable potential for power savings exists by means of proper choice of a logic style for implementing circuits [5]. This is because all the important parameters governing power dissipation, switching capacitance, transition activity, and short-circuit currents—are strongly influenced by the chosen logic style. Depending on the application, circuit can be implemented in different logic style [6].

A. Conventional Static CMOS Logic-CSL

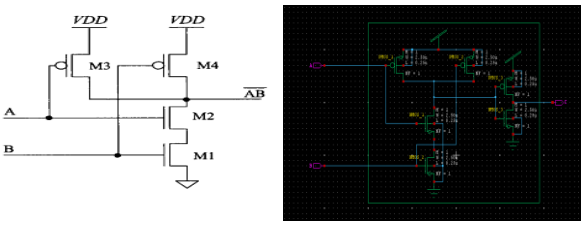
A complementary MOSFET (CMOS) [7] full adder is designed by using pull up and pull down networks .Here the CMOS adder uses 28 transistors where they are highly efficient due to complementary transistor pairs. The voltage scaling and high noise margin design makes them highly advantageous than others thus it makes them to work at low voltages at ratio less transistor sizes. The main drawback of CMOS logic is that it uses more number of PMOS transistors which lead to high power, high delay and area.

Fig.1 (a) and Fig.1 (b) shows symbols of CMOS inverter and their schematic diagram respectively. It requires two transistors. Fig.2 (a) shows the symbol of CMOS NAND2 function .Fig.2 (b) shows the schematic diagram of AND2 function which is designed using CMOS inverter and NAND2 function. It requires six transistors. Half Adder is designed using XOR2 function and AND2 function.Fig.3 (a) and Fig.3 (b) shows the symbol of XOR2 function and schematic diagram of Half Adder respectively.Fig.4 shows the mirror CMOS 1-bit Full Adder and Fig.5 shows the schematic diagram Full Adder.



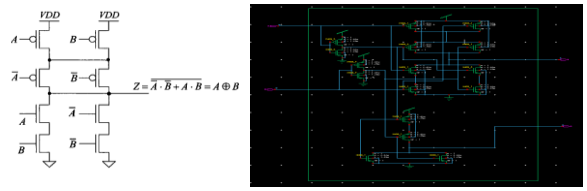
(a) *(b)*

Fig.1 (a) CMOS Inverter (b) Schematic Diagram of CMOS Inverter.



(a) *(b)*

Fig.2 (a) CMOS NAND2 function (b) Schematic Diagram of CMOS AND2 function.



(a) *(b)*

Fig.3 (a) CMOS XOR2 function (b) Schematic Diagram of CMOS Half Adder.

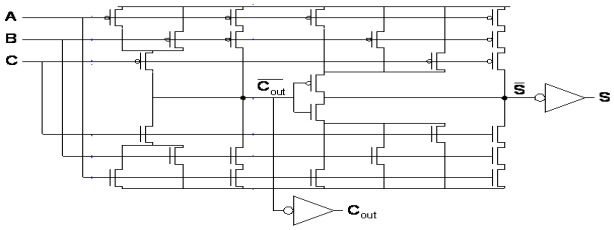


Fig.4 CMOS Full Adder

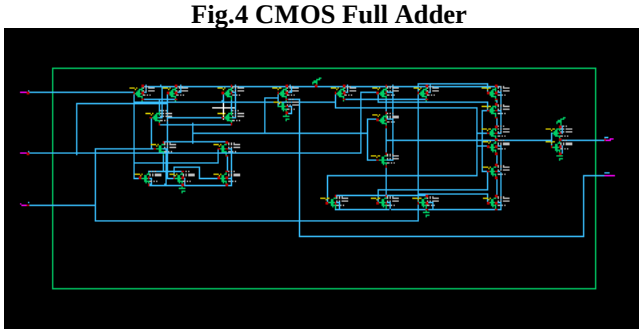
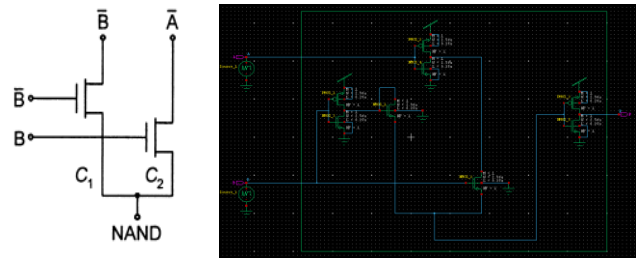


Fig.5 Schematic Diagram of CMOS Full Adder

B. Complementary Pass-transistor Logic-CPL

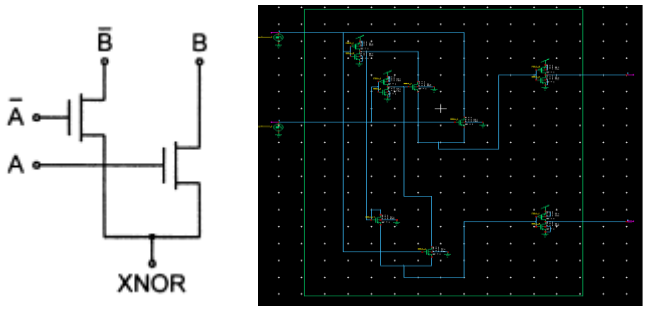
The main concept behind CPL [8] is the use of only an NMOS network for the implementation of logic functions. This results in low input capacitance and high speed operation. Because the high voltage level of the pass-transistor outputs is lower than the supply voltage level by the threshold voltage of the pass transistors, the signals have to be amplified by using CMOS inverters at the outputs [9]. CPL full adder consists of cross coupled NMOS transistors and static PMOS circuits at the output makes the circuit to have good driving capability and full swing operation [10]. The demerit of this CPL adder is that there is large power dissipation in the circuit due to lot of static inverters and internal nodes [11].

Fig.6 (a) shows the symbol of CPL NAND2 function .Fig.6 (b) shows the schematic diagram of AND2 function which is designed using CMOS inverter and CPL NAND2 function. It requires eight transistors. Half Adder is designed using XNOR2 function and AND2 function.Fig.7 (a) and Fig.7 (b) shows the symbol of XNOR2 function and schematic diagram of Half Adder respectively.Fig.8 shows the CPL 1-bit Full Adder and Fig.9 shows the schematic diagram Full Adder. It requires 24 transistors. Here signals noted with '-'are the complementary signals.



(a) *(b)*

Fig.6 (a) CPL NAND2 Function (b) Schematic Diagram of CPL AND2 Function.



(a) *(b)*

Fig.7 (a) CPL XNOR2 function (b)Schematic Diagram of CPL Half Adder.

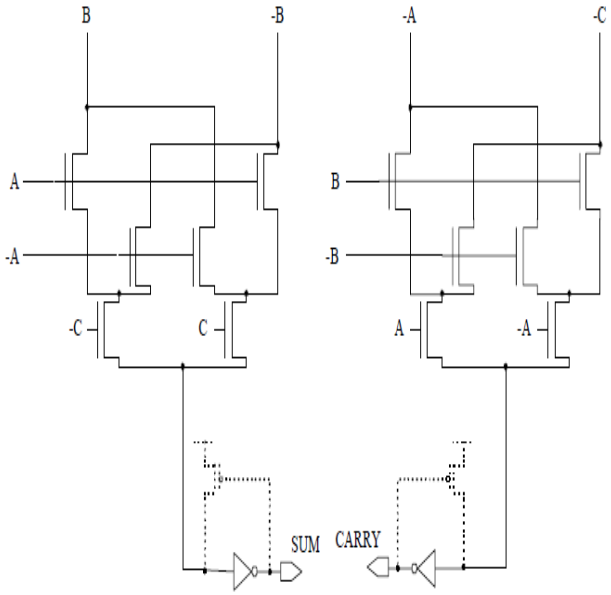


Fig.8 CPL Full Adder

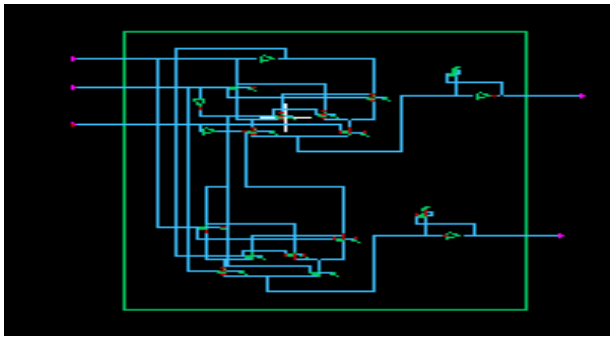
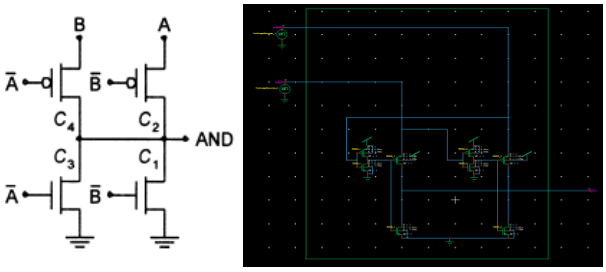


Fig.9 Schematic Diagram of CPL Full Adder

C. Double Pass-transistor Logic-DPL

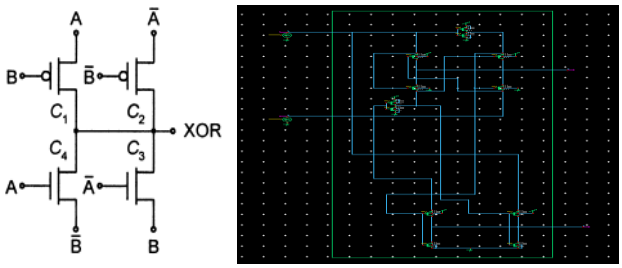
DPL [12] is a modified version of CPL. In DPL, full-swing operation is achieved by simply adding PMOS transistors in parallel with the NMOS transistors. Hence, the problems of noise margin and speed degradation at reduced supply voltages which are caused in CPL circuits due to the reduced high voltage level are avoided. However, the addition of PMOS results in increased input capacitances.

Fig.10 (a) shows the symbol of DPL AND2 function. Fig.10 (b) shows the schematic diagram of AND2 function which is designed in S-Edit. It requires eight transistors. Half Adder is designed using XOR2 function and AND2 function.Fig.11 (a) and Fig.11 (b) shows the symbol of DPL XOR2 function and schematic diagram of Half Adder respectively.Fig.12 shows the symbol of DPL 1-bit Full Adder and Fig.13 shows the schematic diagram Full Adder. It requires 34 transistors. Here signals noted with '-'are the complementary signals.



(a) *(b)*

Fig.10 (a) DPL AND2 function (b)Schematic Diagram of DPL AND2 function.



(a) *(b)*

Fig.11 (a) DPL XOR2 function (b) Schematic Diagram of DPL Half Adder.

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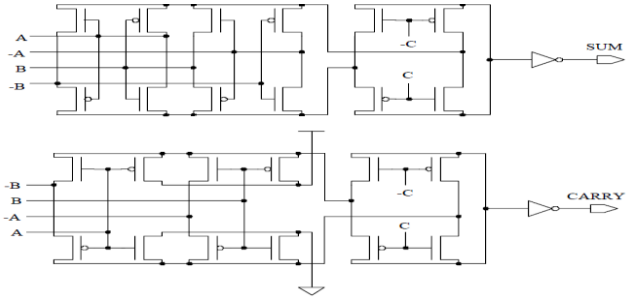

Fig.12 DPL Full Adder

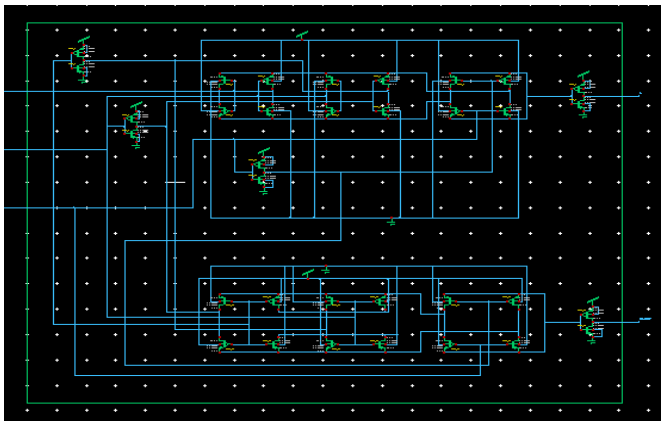

Fig.13 Schematic Diagram of DPL Full Adder

The basic difference of pass-transistor logic compared to the CMOS logic style is that the source side of the logic transistor networks is connected to some input signals instead of the power lines. The advantage is that one pass-transistor either NMOS or PMOS is sufficient to perform the logic operation, which leads to a smaller number of transistors and smaller input loads, particularly when NMOS networks are used. However, the threshold voltage drop (Vout = Vdd - Vth) through the NMOS transistors while passing logic "1" makes swing restoration at the gate outputs which is necessary in order to avoid static currents at the subsequent output inverters or logic gates [13].

III. MULTIPLIER ARCHITECTURE

The multipliers play a major role in arithmetic operations in digital signal processing (DSP) applications. The present development in processor designs aim at design of low power multiplier. So, the need for low power multipliers has increased. Generally the computational performance of DSP processors is affected by its multipliers performance.In this section we design 4 bit unsigned Array and Tree multiplier in different logic style.

A. Array Multiplier

An Array multiplier [14] is very regular in structure. An n bit Array multiplier has n x n array of AND gates to generate partial products, n x (n-2) full adders and n half adders. Each partial product bit is fed into a full adder which sums the partial product bit with the sum from the previous adder and a carry from the less significant previous adder.The number of rows in array multiplier denotes length of the multiplier and width of each row denotes width of multiplicand. The output of each row of adders acts as input to the next row of adders. Each row of full adders or 3:2 compressors adds a partial product to the partial sum, generating a new partial sum and a sequence of carries as shown in Fig.14.

Schematic diagram of unsigned Array Multiplier is shown in Fig.15. In this figure (a3, a2, a1, a0) is multiplicand and (b3, b2, b1, b0) is multiplier. In place of input bit pattern voltage source is applied. P7P6P5P4P3P2P1P0 is the output of multiplier where P0 is LSB and P7 is MSB

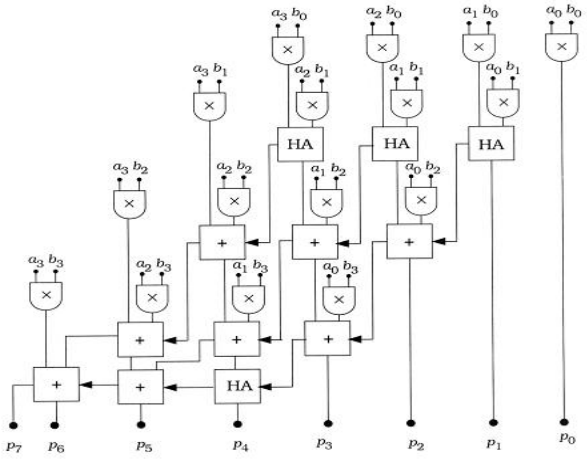

Fig.14.4-bit Unsigned Array Multiplier Architecture

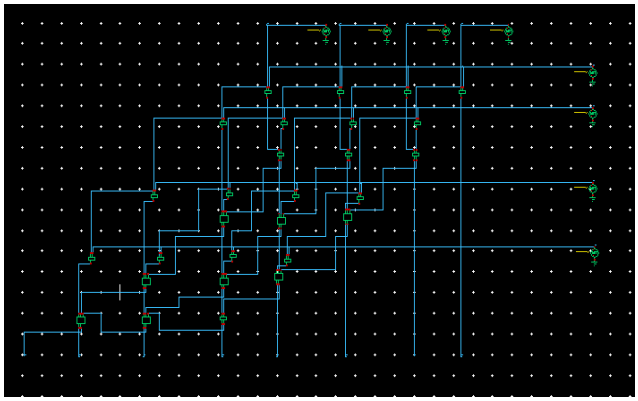

Fig.15 Schematic Diagram of 4-bit Unsigned Array Multiplier

The delay associated with the array multiplier is the time taken by the signals to propagate through the AND gates and adders that form the multiplication array. Delay of an array multiplier depends only upon the depth of the array not on the partial product width. The delay of the array multiplier is given by [15].

T (critical) = [(N-1) + (N-2)] * T (carry) + (N-1) T (Sum) + T (AND) (3)

Where T(carry) is the propagation delay between input and output carry, T(Sum) is the delay between the input carry and sum bit of the full adder, T(AND) is the delay of AND gate, N is the length of multiplier operand.

The advantage of array multiplier is its regular structure. Therefore it is easy to layout and has small size. In VLSI designs, the regular structures can be cemented over one another. This reduces the risk of mistakes and also reduces layout design time. This regular layout is widely used in VLSI math co-processors and DSP chips [16].

B. Tree Multiplier

C. S. Wallace suggested a fast technique to execute multiplication in 1964 [17]. The amount of hardware essential to perform this style of multiplication is large but the delay is near optimal. The delay is proportional to log (N) for column compression multipliers where N is the word length. This architecture is used where speed is the main concern not the layout regularity.

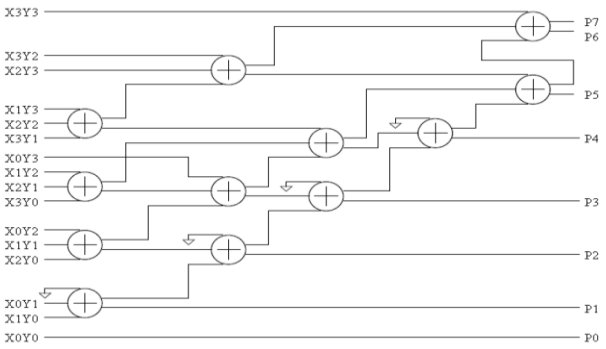

Fig.16 4-bit Unsigned Tree Multiplier Architecture

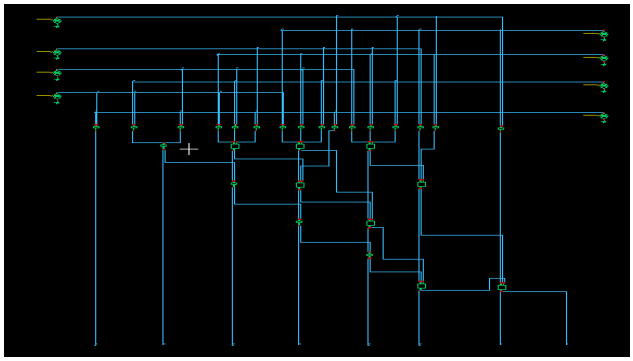

Fig.17 Schematic Diagram of 4-bit Unsigned Tree Multiplier

This class of multipliers is based on reduction tree in which different schemes of compression of partial product bits can be implemented. In tree multiplier partial-sum adders are arranged in a treelike fashion, reducing both the critical path and the number of adders needed as shown in the figure 16. [18]

A collection of AND2 gates generate the partial products or multiples simultaneously. The multiples are added in combinational partial products reduction tree using carry save adders, which reduces them to two operands for the final addition. The results from CSA are in redundant form. Finally, the redundant result is converted into standard binary output at the bottom by the use of CPA [19] as shown in Fig.16.

Schematic diagram of unsigned Tree Multiplier is shown in Fig.17. In this figure (Y3, Y2, Y1, Y0) is multiplicand and (X3, X2, X1, X0) is multiplier. In place of input bit pattern voltage source is applied. P7P6P5P4P3P2P1P0 is the output of multiplier where P0 is LSB and P7 is MSB

IV. SAMPLES AND RESULTS

The functionality of the multipliers are verified and their average power, delay, and power delay product are calculated in transistor level using T-spice at 25c temperature with 0.15um technology and their simulation waveforms are shown in fig18. The attention is not only on delay or power but also usage the full adders replacing in half adder designs thus number of transistors are reduced. We can achieve better performance in higher order circuits.Fig.18.shows the output waveform of multipliers for same input with P0 is at bottom and P7 is at top

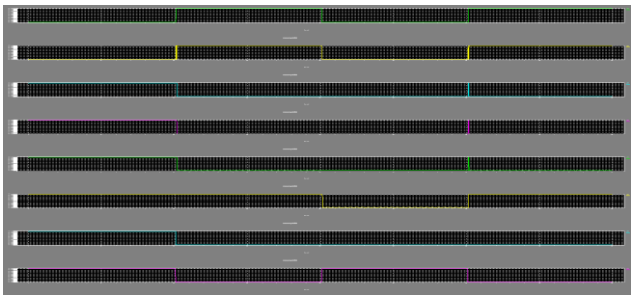

Fig.18 Output Waveform of Multiplier.

V. PERFORMANCE PARAMETER AND SIMULATION SET-UP

The 4-bit multipliers are compared based on the performance parameters like propagation delay, number of transistors and power dissipation. To achieve better performance, the circuits are designed using CMOS process in 150 nm technology. The channel width of the transistors is 450n for the NMOS and 450nm for the PMOS. The output capacitance C_L is 1pF in all cases whereas the operating frequency is 50MHz. All the circuits have been designed using TANNER EDA v13.0 [20] with model file as **dual.md.** To achieve low power and high performance multipliers these are tested at 5v so, that the performance of multipliers can be improved. The power estimation is a difficult task because of its dependency on various parameters and has received a lot of attention [21]. For simulation method [22] T-spice is used in order to analyze the results. The comparative results for two different 4-bit multipliers for different logic design styles are given in Table. I.

Table .I Comparisons of performance parameters for different logic styles

Multiplier Type	Logic style	Delay(ns)	Power(µW)	PDP(fJ)	No. of transistor
Array	CMOS	8.300	10.73	89.06	384
	CPL	4.337	24.70	131.82	368
	DPL	4.667	19.72	92.03	448
Tree	CMOS	4.247	10.68	45.35	384
	CPL	4.105	23.61	125.25	368
	DPL	4.526	19.87	89.93	448

A bar graph is plotted for delay (ns) and power dissipation (µw) of 4-bit unsigned multiplier architectures for the logic used here as shown in Fig.19 and Fig.20 respectively.

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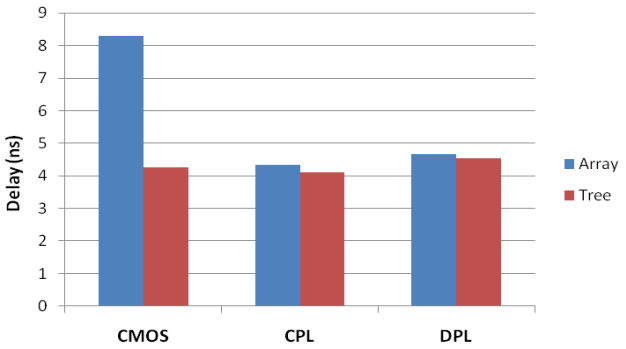

Fig.19 Propogation Delay in Multipliers(Array and Tree) for Various Logic Styles.

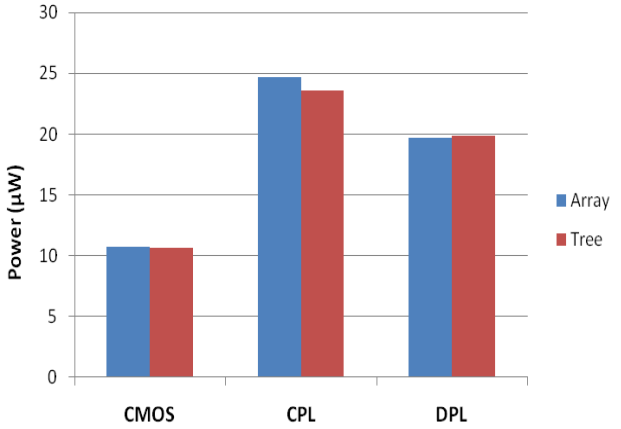

Fig.20 Power Dissipation in Multipliers (Array and Tree) for Various Logic Styles.

VI. DISCUSSION AND CONCLUSION

It has been observed that complementary pass transistor (CPL) logic design style exhibit better characteristics as compared to other design styles. So, CPL logic style can be used where portability and high speed is the prime aim. Where, CMOS consumes the lowest power among the three. But, the CPL logic design style has propagation delay analogous to DPL and CMOS logic design style, so CPL can be considered best logic design style with respect to all parameters of 4-bit multiplier architectures as shown in Table 1.

From the above results, it is observed that array multiplier and tree multiplier exhibits lowest PDP by using CMOS logic design style. Hence CMOS logic is used where lowest DC power dissipation is required.

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