Implementations of DPDE for Delay Locked Loop for High Frequency Clock of 2.5GHz High Speed Applications

J. Meenakshi, G. Rakesh Chowdary, A. L. G. N. Aditya

Abstract:- Variable delay elements are often used to manipulate the rising or falling edges of the clock or any other signal in integrated circuits (ICs). Delay elements are also used in delay locked loops (DLLs). Variable delay elements have many applications in VLSI circuits. They are extensively used in digital delay locked loops phase locked loops (PLLs), digitally controlled oscillators (DCOs), and microprocessor and memory circuits. In all these circuits, the variable delay element is one of the key building blocks. Its precision directly affects the overall performance of the circuit. In this a new proposed digitally controlled delay element is implemented in 130nm technology for DLL Delay locked loop for higher clock rates greater than 2.5GHz. This is implemented in Micro wind tool.

Index Terms:- DLL, PLL, Delay element, Microprocessor, Clock frequency.

I. INTRODUCTION

As technology is shrinking day by day, supporting the highest bandwidth data rates between devices requires advanced clock management technology with correct clock timing necessary for proper operation of high performance digital and mixed-signal circuits. As the size decreases and operating frequency of VLSI systems increase, designing of clock distribution system poses numerous challenges. In general, the quality of clock pulses is determined by several constraints such as frequency, phase, duty-cycle, jitter, and clock skew. 'Delay elements' constitute to be one among the basic building blocks of such clock distribution network in VLSI circuits and systems.

They are intended to define a time reference for the movement of data within those systems**.** Since they play an important role in designing accurate clocks, they are highly crucial from the aspect of design and implementation. Although a few delay elements are existing[2][3], they do not offer large delay ranges and are insensitive to small changes in the control input. This makes them unsuitable for many practical applications. Hence a better delay element is necessary, which has large delay ranges and can be precisely controlled by a control vector. To develop an improved Digitally Programmable Delay Element (DPDE) architecture in 130nmm technology using Microwind simulation tool.
The new DPDE should have larger delay ranges than the existing delay elements and moderate power consumption.

Manuscript received on April 26, 2012.

J.Meenakshi, M.tech VLSI, KL University, Vijayawada, India, Mobile No 8374030842, (e-mail:jandhayala.meenakshi@gamil.com).
G. Rakesh Chowdary, ECE, KL University Vijayawada, India, Mobile No 9000800891, (e-mail:rakeshchowdary23@yahoo.com).
A.L.G.N.Aditya, M.tech VLSI, KL University, Vijayawada, India, Mobile No 9014936978, (e-mail:adityasind@gamil.com).

Variable delay element is a new gate design in VLSI that can produce different delays at the output for a given input according to a variable control signal.

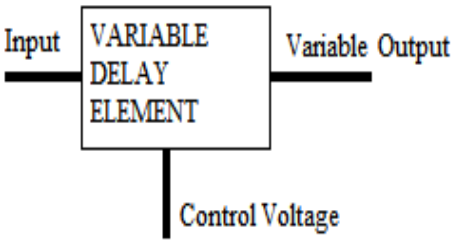


Fig 1 Variable Delay Element

These are inverter–based circuits used for fine, precise, and accurate pulse delay control in high-speed digital integrated circuits. In order to achieve wide phase shift variable delay elements are realized as a chain of inverters. The chain of inverters is called delay line. In a delay line, each of the delay stage provides a delay path for passing the input signal with predetermined delay time and generates possible delays according to the voltage control applied to various stages. The number of cascaded delay elements determines the maximum delay of the delay line. Thus the use of variable input delay gates drastically reduces the required number of delay buffers. These elements find applications in complex VLSI ICs, delay lines are constituents of DLLs (Delay Locked Loops), TDCs (Time-to-Digital Converters), VCOs (Voltage Controlled Oscillators), Pulse-Width Control Loops (PWCLs) etc.

II. DLL (DELAY LOCKED LOOP)

Delay-Locked Loop (DLL) circuits provide zero propagation delay and low clock skew between output clock signals distributed throughout the device allowing for very precise synchronization of external and internal clocks.DLL in its simplest form consists of a variable delay line and control logic. The delay line produces a delayed version of the input clock CLKIN. The clock distribution network routes the clock to all internal registers and to the clock feedback CLKFB pin. The control logic must sample the input clock as well as the feedback clock in order to adjust the delay line. Delay lines can be built using a voltage controlled delay or a series of discrete delay elements.

DLL works by inserting delay between the input clock and the feedback clock until the two rising edges align, putting the two clocks 360 degrees out of phase (meaning they are in phase). After the edges from the

input clock line up with the edges from the feedback clock, the DLL "locks." As long as the circuit is not evaluated until after the DLL locks, the two clocks have no discernible difference. Thus, the DLL output clock compensates for the delay in the clock distribution network, effectively removing the delay between the source clock and its loads.

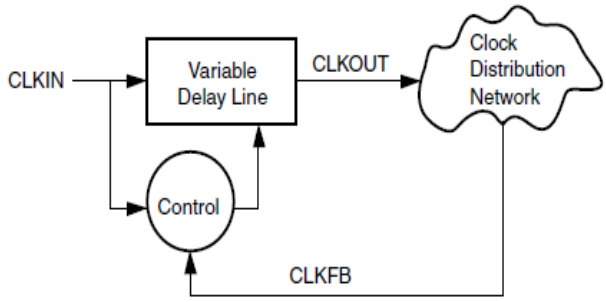


Fig 2 Delay-Locked Loop Block Diagram

A.Existing Delay Element Design

The design of delay elements has various techniques, but the major constraints are the high frequency clock rates and area that determine the design issues of the delay element.

A. Shunt Capacitor Delay Element

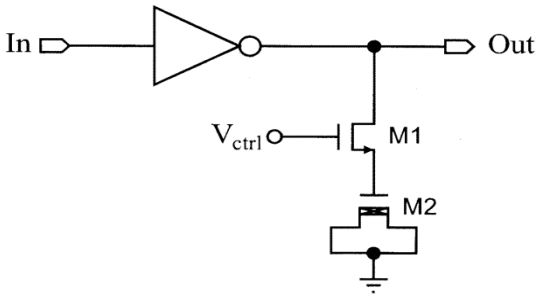
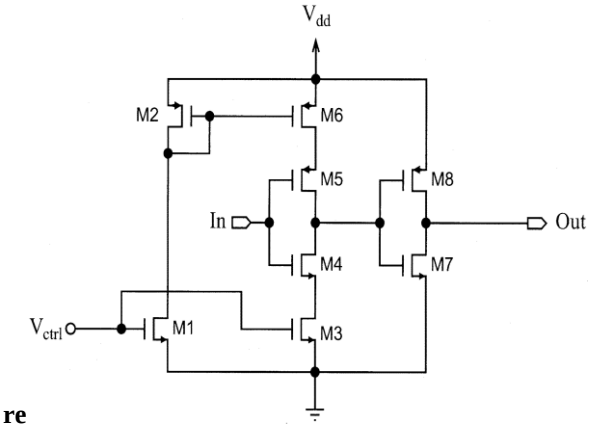


Fig 3 shunt capacitor delay element

Fig 3 shows the basic circuit of using a shunt capacitor. In this circuit, M2 acts as a capacitor. Transistor M1 controls the charging and discharging current to the M2 from the NOR gate. The M1 gate voltage controls the discharge current. As a consequence, the NOR gate delay can be controlled. Shunt capacitor delay element is capacitive loaded inverter. In this case, the transistor (M1) acts as a linear resistor and defines the charging/discharging current of a load capacitor (transistor M2). Indirectly it changes the delay of output pulses. This type of delay element has the following disadvantages: a) the output capacitor occupies large silicon area; b) the amount of a delay and the active range of voltage regulation are small. This choice allows for a robust implementation of the circuitry controlling the delay generation, while the maximum speed attainable by the line is high compared to the maximum speed achieved by other delay line architectures. These are used in applications when maximum speed and power of consumption are of concern.

B.B.Current Mirror Delay Element



re

Fig 4 Current Mirror Delay element

The basic building block of a Current Mirror Delay element is illustrated in the above figure. There are two inverters between input and output of this circuit. The charging and discharging currents of the output capacitance of the first inverter, composed of M4 and M5, are controlled by two MOS transistors, M3 and M6. Charging and discharging currents depend on the gate voltage of M6 and M3 transistors, respectively. M2 and M6 constitute a current mirror for controlling the current of M6 using the control voltage. In this delay element, both the rising and falling edges of the input signal can be controlled. If in a given application only the control of rising (falling) edge is required, and then Vctrl may directly be applied to M3 (M6). The second stage inverter (composed of M7 and M8) is for improving the rise and fall times of the circuit. Sometimes, multiple cascaded inverters are used for this purpose.

C.Current Starved Delay Element

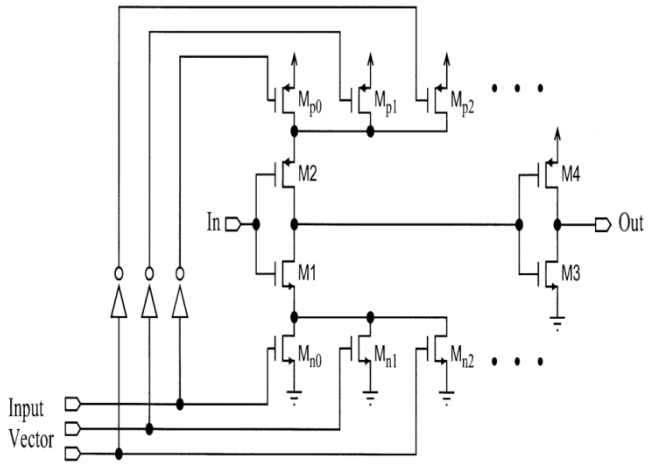


Fig. 5 Current starved delay element

In both of the above techniques, a continuous voltage is used to control the delay. In some applications, we need a delay which can be controlled digitally. The current mirror circuit can be modified for this purpose. Fig. 3 shows a current starved DCDE. As can be seen, by applying a specific binary vector to the controlling transistors (Mn0,Mn1,…Mp0, Mp1,…), a combination of transistors are turned on at the sources of the M1 and M2 transistors. Such an arrangement, controls the rise and fall times (and hence, the delay) of the output voltage of the first inverter. The ratios of the controlling transistors are usually chosen in a binary

fashion so as to achieve binary, incremental delay. Unfortunately, as it will become apparent in the following sections, neither the binary, nor any other way of weighing can make a linear, monotonic relationship between the input vector and the output delay.

D.Delay Element using variable Resistor

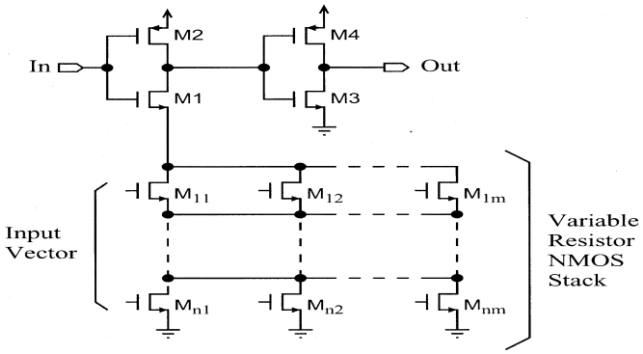


Fig 6 Delay element using variable resistor

In this circuit, a variable resistor is used to control the delay. A stack of n rows by m columns of NMOS transistors is used to make a variable resistor. This resistor subsequently controls the delay of M1. In the circuit, only the rising edge of the output can be changed with the input vector. Another stack of PMOS transistors can be used at the source of the PMOS transistor, M2, to have control over the falling edge delay. The input vector is an n x m matrix with elements logic "1" or "0".The matrix is taken such that it contains at least one charging and discharging path. In this kind of circuit, at any time, at least one transistor should be ON in each of the rows. Hence, with six transistors in two rows, there are at most nine different resistance combinations. The delay prediction in this structure for a given input vector is even more complicated than the current starved DCDEs. Besides changing the equivalent resistance, a change in input vector causes a change in the effective capacitance seen at the source of M1 and other intermediate nodes in the NMOS stack.

All these design techniques have pro and cons, one such disadvantage is with existing DCDE architecture is the non monotonic delay behavior with ascending binary input pattern. One usually expects to have a longer circuit delay for a smaller W/L ratio of controlling transistor(s). The resistance of the controlling transistor: by increasing/ decreasing the effective ON resistance of the controlling transistor(s) at the source of M1, the circuit delay can be increased/decreased. And the capacitance of the controlling transistor: as the effective capacitance at the source of M1 increases the charge sharing effect causes the output capacitance to be discharged faster and the overall delay of the circuit decreases. The problem of finding the W/L ratios of the transistors in both of the above mentioned methods is difficult. The result of any change in W/L parameter cannot be estimated and the circuit should be simulated for every change in the W/L. To overcome this problem we propose a new configuration for a DCDE in the following section. In this circuit, finding the W/L ratios of the transistors is straightforward and determining the input vector for a specific delay is simpler than the methods mentioned above.

III. PROPOSED DELAY ELEMENT

It can be seen in this figure, a current starved buffer, M7–M11, is the main element. The controlling current through this buffer is controlled by a current mirror circuit composed of transistors M6–M7. An appropriate current through M7 can be adjusted by turning-on transistors M1–M4, while transistor M5 is always on. At the instance when M8 turns on, the capacitor at its output node starts to discharge. The discharging current is controlled by transistor M7 acting as a current source. The passing current through this transistor is determined by the gate voltage of M6. The gate voltage of M6, in turn, is determined by the current passing through its drain. PMOS transistors M1–M5 control the current flowing through M6 NMOS transistor. Therefore, the overall delay of this circuit is digitally controlled by M1 to M4. The W/L ratio of transistors M5 can be designed for maximum delay of the circuit. The input vector for a specific delay is applied to the gates of M1 to M4 (a,b,c,d). In this circuit, depending on the input vector, one may realize 16 different delay settings.

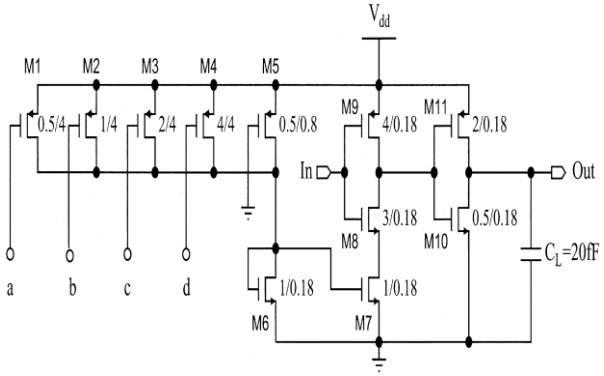


Fig 7 Developed Digitally Programmable Delay element

In order to find a relationship between V_g (the gate voltage of transistor M7 and/ or M6), and the delay of the circuit (t_d), we should calculate the current passing through transistor M7. Once this current is known, one can find the output voltage. Transistor M7 is a relatively small transistor with a channel length of 0.18 m. It shows a velocity saturated behavior for gate voltages more than about 0.65 V. Hence, we can consider the following for the drain current of this transistor.

$$i_d = \frac{k_n W_7}{2L_7}(V_g - V_{T7})(1 + \lambda V_{DS7}) \text{--- (1)}$$

Where represents the overall capacitance at node V_{01} and

$$K_1 = \frac{k_n W_7}{2L_7}(V_g - V_{T7}) \text{ ----- (2)}$$

Solving the above differential equations with initial condition of $V_{01}=V_{dd}$ at **t=0** results to the following

$$V_{01} = (V_{dd} + 1/\lambda_7)e^{-t/\tau_1} - 1/\lambda_7 \text{ --- (3) and}$$

$$\tau_1 = C_{L1}/(K_1\lambda_7)$$

$$t_{d1} = \tau_1 L_n \frac{1+\lambda_7 V_{dd}}{1+\lambda_7 V_{dd}/2} \text{ ---- (4)}$$

To compute the circuit delay of this delay element, we should V_{02} find as a function of time. At the instance when the input voltage (V_{in}) goes high, V_{01} starts to fall and M10 starts to turn off. When V_{01} becomes less than V_{dd}-V_{T11}, transistor M11 starts to conduct

while transistor M10 starts to turn off. Hence, for a period of time, both M10 and M11 transistors are on. Owing to the current starved nature of the first inverter, the fall time of V_{01} is not very small. Therefore, the direct current passing through transistors M10 and M11 is not negligible. It is necessary to consider the current in both of these two transistors in order to find V_{02}. However, this complicates the equations and defeats the purpose of a simple analytical model. We assume that the direct path current is negligible and can be ignored in these calculations. Moreover, ignoring the channel length modulation effect of M11, we can write

$$i_{d11}=\frac{k_p W_{L11}}{2L_{11}}(V_{gs11}-V_{T11})^2 \text{ --- (5)} \quad \text{And}$$

$$i_{d11}=C_L\frac{dV_{02}}{dt}$$

The initial condition for the above differential equation is V_{02} =0 at t=0. We can substitute V_{gs11} in the above equation by V_{dd} - V_{01} ($t+t_p$) where t_p is the time when V_{01} reaches V_{dd}-$|V_{T11}|$ that is

$$t_p=\tau_1 L_n\frac{1+\lambda_7 V_{dd}}{1+\lambda_7(V_{dd}-|V_{T11}|)} \text{ --- (6)}$$

$$V_{02}=K_3K_2^2\tau_1\left(\frac{t}{\tau_1}+2e^{-t/\tau_1}-\frac{1}{2}e^{-2t/\tau_1}-1.5\right))$$

$$K_2=V_{dd}+\frac{1}{\lambda_7}-|V_{T11}|$$

$$K_3=\frac{k_p W_{L11}}{2L_{11}C_L} \text{ -- (7)}$$

In spite of ignoring the direct path current in M10/M11, and channel length modulation effect in transistor M11, (9) is too complicated to be used as a means for delay element circuit design.

$$t_d=\frac{A_1}{(V_g-V_1)} \text{ ---- (8)}$$

Where A_1 and V_1 are constants. This equation illustrates the relationship between V_g and td of the delay element. TheV_g, in turn, is a function of the current passing through M6. The drain current of M6 is the sum of the drain currents of all the PMOS transistors (M1 through M5). Since, M6 is working in saturation, V_g can be found from the following

$$V_g=V_2+A_2\sqrt{I}$$

Where A_2 and V_2 are constants and depend on M6. V_2 is actually the threshold voltage of M6 and A_2 is the inverse of the root of its transconductance M6. In (11), the current ***I*** can be calculated from

$$I=I_0+I_1\bar{a}+I_2\bar{b}+I_3\bar{c}+I_4\bar{d}$$

The coefficientsI_0, I_1,I_2,I_3 and I_4 depend on W/L ratio of the pMOS transistors. All the parameters in the above formulas can be found by simulating the circuit for five different input vectors (***abcd***=1111, 0111, 1011, 1101, 1110).

IV. DESIGN STEPS OF THE PROPOSED DELAY ELEMENT

a). The size of transistors M8 to M11 is basically determined by the load capacitance. Transistor M7 should be much smaller than M8 such that the discharging current is controlled by M7. M6 can be the same size as M7.

b) The number of pMOS controlling transistors (N) can be obtained from the number of different delays (m) one may want to get from the delay element such that **m=** 2^N Moreover, the circuit must contain one more pMOS transistor (M5) which is always on.

c) Place M5 and size it to get the maximum delay

d) After sizing M5, place one PMOS transistor (e.g., M0) in parallel to M5 and size it to obtain the minimum required delay.

e) Now M0 should be broken into N transistors, (M_{p0} toM_{pN}), in a binary fashion. That is

$$\left(\frac{W}{L}\right)_{M_{pi}}=\frac{2^{i-1}}{2^{N-1}}\left(\frac{W}{L}\right)_{M_0}$$

1. Implementation and Results

The basic Delay element circuit layout's are drawn in Microwind and for a given clock frequency the delay between the input clock frequency and the clock output, for various values of control input Vcntrl are tabulated

E. Shunt Capacitor Delay Element

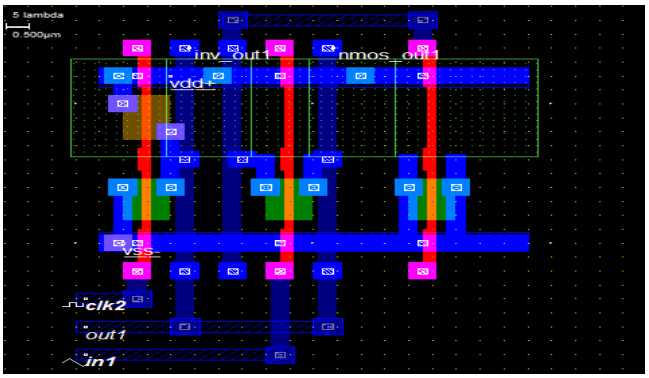


Fig .8 Shunt capacitor Delay Element

F. Current Mirror Delay Element

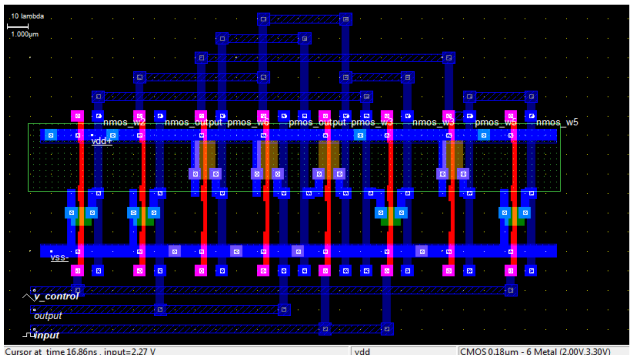


Fig 9 current mirror delay element layout

In the Current Mirror delay element circuit the M1, M2 transistors give out a constant current, thus making the delay directly dependent on the control input.

G. Current Starved Delay Element

This delay element has 3 bit digital inputs to control the delay of the output. So the output is simulated for the 8 (=2^3) possible combinations of the digital control inputs and the

delay is observed for the various combinations. These are plotted against the control input to study the characteristics of the delay element. Figure 6 -7 shows the layout of current starved delay element.

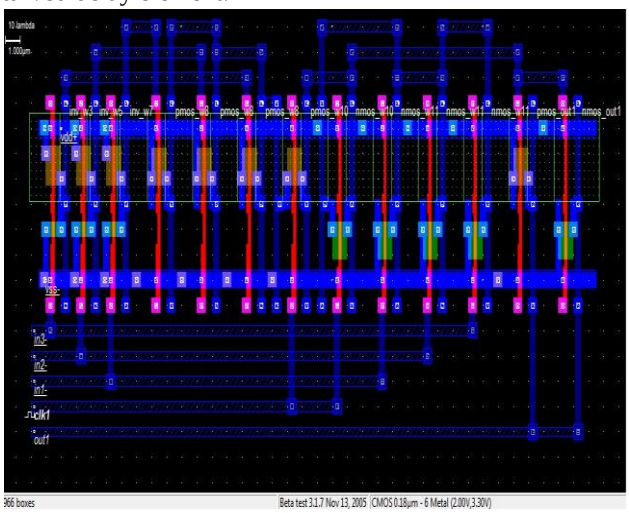


Fig 10. Current starved delay element

H. 3 Bit Proposed DPDE

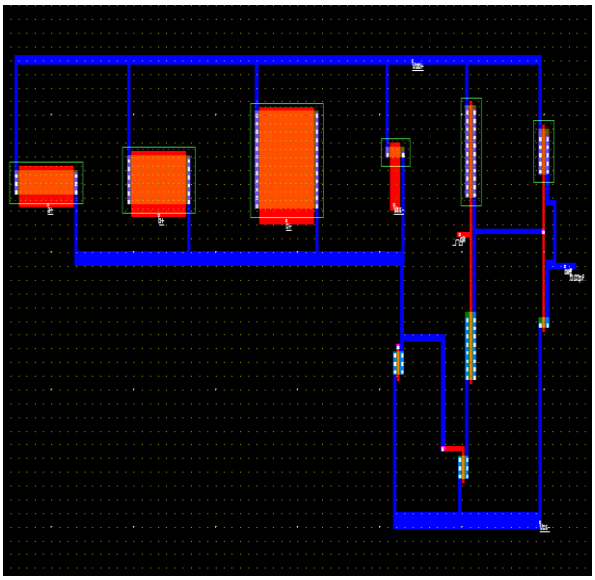


Fig 11 3 Bit DPDE layout

When compared to all the design this proposed architecture produces the greater delay and this can be easily programmable using a digital input. When current starved and the shunt capacitor produce 25ps and 120ps, the proposed architecture produces 712ps.

Table.1 3 bit DPDE Delay and control voltage

CONTROL VOLTAGE	DELAY IN PS
000	712
001	596
010	491
011	423
100	372
101	330
110	313
111	270

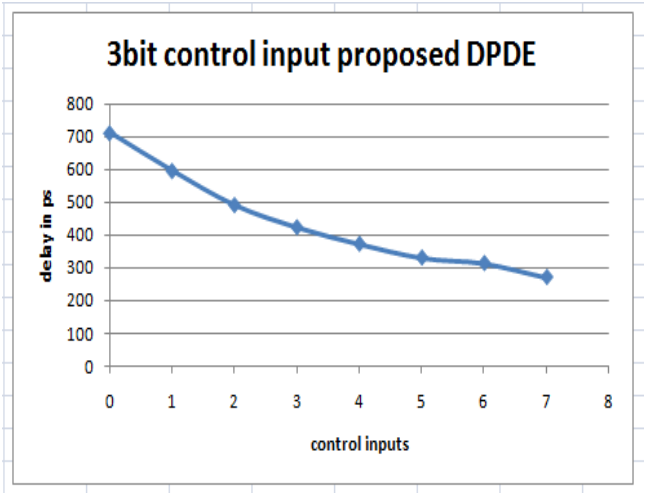


Fig 12 graphical representation of 3 bit DPDE delays

I. 4 Bit DPDE Delay Element

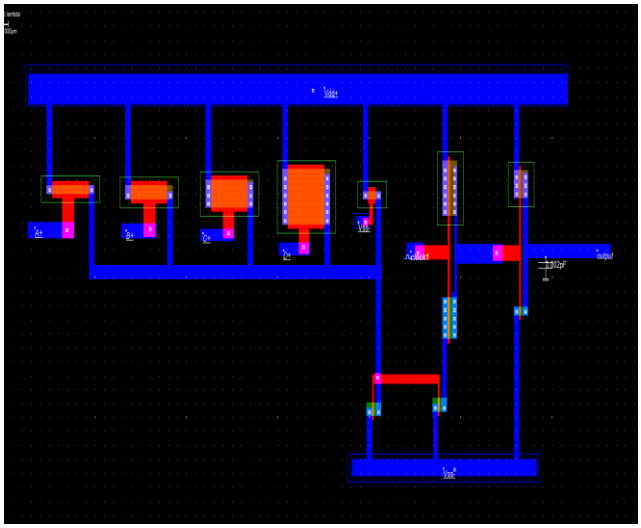


Fig 13 4 bit DPDE layout

the developed DPDE gives the best performance among all the existing circuits. The maximum delay is 725ps and the minimum delay is 250ps. Thus the delay range is approximately 375ps. The delay decreases monotonically with increasing control input level. For each control input Vctrl there is a unique delay possible and the delay can be varied exactly by varying the control inputs. The power dissipation is also comparable with the current starved delay element, nearly 67µW.

The static power consumption of the circuit can be optimized independent of its delay behavior. This can be achieved by scaling down the W/L ratios of transistors M1 to M6. The key issue in such an exercise is to keep V_g constant. In order to examine the effectiveness of this method, we scaled down the W/L ratio of M1–M6 transistors by half. The resulting circuit was simulated and found to be consuming 51µW of power while its maximum delay remained unchanged, resulting in overall decrease in the delay range. However, it should be mentioned that as the current is reduced, it becomes more susceptible to interference.

Therefore, there is a tradeoff between power consumption and noise immunity of the circuit

Table.2 4 bit DPDE delay vs Control voltage in ps.

CONTROL VOLTAGE	DELAY IN PS
0	775
1	661
10	604
11	537
100	500
101	456
110	431
111	399
1000	380
1001	357
1010	343
1011	324
1100	313
1101	298
1110	289
1111	277

V. CONCLUSION

In this project a new architecture for a digitally programmable delay element is developed. The developed circuit is compared with three other architectures. Moreover, simple empirical equations for finding the delay of the circuit are investigated. These equations can determine the delay of the circuit with an error of less than 6%. The main advantage of the proposed delay element is that finding the input vector for a specific delay is straightforward compared to the two other DCDEs. Furthermore, the delay behavior is monotonic. The delay range if found to be the highest among all the existing circuits. The simulations are repeated for various transistor sizes in order to find the most optimum design parameters. The results are simulated at 2.5GHz frequency, but are found to be satisfactory up to 5GHz. The delay of the developed is changes quickly with change in the control vector. This characteristic may be exploited in high-precision applications and in this paper it is designed for DLL(Delay Looked Loop).

REFERENCES

1. M. Saint-Laurent and M. Swaminathan, "A digitally adjustable resistor for path delay characterization in high frequency microprocessors," in Proc. Southwest Symp. Mixed-Signal Design, 2001, pp. 61-64.
2. M. G. Johnson, E. L. Hudson, and H. Kopka, "A variable delay line PLL for CPU-Coprocessor synchronization," IEEE J. Solid-State Circuits,vol. 23, pp. 1218–1223, Oct. 1988.
3. Current Starved Delay Element with symmetric load by G.S.Jovanovic, M.K.Stojcev. Published in International Journal of Electronics, Volume 93, Issue 3 March 2006, pages 167-175
4. Rothermel and F. Dell'ova, "Analog phase measuring circuit for digital CMOS ICs," IEEE J. Solid-State Circuits, vol. 28, no. 7, pp. 853–856, Jul. 1993.
5. M. Saint-Laurent and G. P. Muyshondt, "A digitally controlled oscillator constructed using adjustable resistors," in Proc. Southwest Symp. Mixed-Signal Design, 2001, pp. 80–82.
6. "Digital Integrated Circuits –A Design Perspective" by JAN M. RABAEY, ANANTHA CHANDRAKASAN and BORIVOJE NIKOLIC.

AUTHORS PROFILE

J. Meenakshi was born in Tenali, Guntur (Dist.), AP, India. He received B.Tech. in Electronics & Instrumentation Engineering from SV University AP, India ,M.Tech from KL University , Vijayawada, AP, India.

G. Rakesh Chowdary working as Asst.Prof in ECE Dept from KL university. He has deep interest in analog design and low power design. He has 3 Publishments

A. L. G. N. Aditya was born in vizag,(dist),AP, India. He received B.Tech. in Electronics & Communication Engineering from TPIST,AP. India ,M.Tech from KL University , Vijayawada, AP, India. He has undergone 8 international conferences and 1 publishment in IEEE