

FPGA Implementation of Optimized 4 Bit BCD and Carry Skip Adders using Reversible Gates

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Abstract: The project proposes design of BCD adder and implementation of Carry Skip adder using the new concept of Reversible logic gate to improve the design in terms of garbage's and area on chip. Furthermore, in the recent years, reversible logic has emerged as a promising technology having its applications in low power CMOS, quantum computing, nanotechnology and optical computing because of its zero power dissipation under ideal conditions. It is not possible to realize quantum computing without reversible logic gates. Thus, the project will provide the reversible logic implementation of the conventional BCD adder using NG and NTG gate and Carry skip adder using TSG. The proposed reversible logic implementation of the 4-bit BCD adder is optimized to obtain minimum number of reversible logic gates and minimum number of garbage outputs. This project work on the reversible BCD circuits designed and proposed here form the basis of the decimal ALU of a primitive quantum CPU.

The designed and optimized 4-bit reversible BCD adder and existing Carry skip adder are implemented in VHDL Using Xilinx ISE 10.1 tool and simulated using ModelSim SE 6.3f. Implemented on FPGA Spartan-II.

Index Terms: Reversible logic, Feynman gate, NOT Gate, Fredkin Gate, TSG Gate, New Toffoli Gate, New Toffoli Gate, TS-3 Gate, NTG, BCD etc.

I. INTRODUCTION

Due to the information loss in irreversible hardware computation, it results in energy dissipation. Loss of information is an important consideration in digital design. Part of the energy dissipation is due to the non-identity of switches. Because of higher level of integration and use of new fabrication process have dramatically reduced the heat loss over last decades [5]. Other part of the energy dissipation is according to Landauer's research, the amount of energy dissipated for every irreversible bit operation is at least $KT \ln 2$ joules, where $K=1.3806505 \times 10^{-23} \text{ m}^2 \text{ kgs}^{-2} \text{ k}^{-1}$ (joules/Kelvin) is the Boltzmann's constant and T is the temperature at which operation is performed.

In 1973, Bennett showed that $KT \ln 2$ energy would not be dissipated from a system as long as the system allows the reproduction of the inputs from which does not result in information called reversible.

Reversible are circuit (gates) in which number of inputs and outputs are equal i.e. one to one mapping between inputs and outputs. Reversible logic supports the process of running the systems both forward and backward [2]. It means that reversible computation can generate inputs from outputs and can stop and go back to any point in computation history. The amount of energy dissipation in a system increases in direct proportion to the number of bits that are erased during computation. Bennett showed that $KT \ln 2$ energy dissipation would not occur, if a computation is performed in a reversible

way. Reversible computation in a system can be performed if the system is composed of reversible gates. Thus Reversibility may play important role in future circuit design.

The current irreversible technologies will dissipate a lot of heat and can reduce the life of the circuit. The reversible logic operations do not erase (lose) information and dissipate very less heat. Thus, reversible logic is likely to be in demand in high speed power aware circuits.

The most prominent application of reversible logic lies in quantum computers. A quantum computer will be viewed as a quantum network (or a family of quantum networks) composed of quantum logic gates.

The main objective of this project is to design and optimize 4-bit BCD adder and implement Carry skip adder such that,

- Minimum number of gates is used for implementation
- Restrict the number of garbage outputs as fewer as possible
- Design should cater all the good features of reversible logic synthesis

This project focuses on the design and optimization of 4-bit BCD adder and implement Carry skip adder using reversible gates.

II. NEED OF REVERSIBLE CIRCUITS

Following are the need of reversible circuits:

- The amount of heat dissipation due to information loss in irreversible circuit is avoided by reversible logic gates
- Reversible logic circuits are in demand for high speed power aware circuits
- Reversible logic gates are needed to recover the state of inputs from outputs
- Reversible computing will lead to improvement in energy efficiency
- Energy efficiency will fundamentally affect the speed of circuits such as nano circuits and therefore the speed of most computing applications
- To increase the portability of devices again reversible computing is required.
- High performance chips are releasing large amounts of heat, to reduce the heat reversible logic gates are used.

III. LIMITATIONS OF REVERSIBLE GATES

Following are the limitations of reversible gates:

- Fan-out is not permitted
- Loops are not allowed

Fan-out and feedback can be achieved using copying gate

-Feynman and Double Feynman gates [12][13].

IV. PROPERTIES OF REVERSIBLE LOGIC GATE

Following are the properties of logic gate:

- Minimum input constants
- Minimum number of gates
- Minimum number of garbage outputs

Garbage outputs are those outputs which are not used further for any computation

V. SYNTHESIS OF REVERSIBLE GATES

Synthesis of reversible logic is different from conventional logic [20]. Synthesis can be carried out from the input towards the outputs or from the output towards the inputs. In reversible logic there is one more factor, which is more important than the number of gates used i.e. the number of garbage outputs. The Unutilized outputs from a reversible gate/circuit are called “garbage”. Though every synthesis method engages them producing less number of garbage outputs, but sometimes garbage outputs are unavoidable [5].

VI. REVERSIBLE GATES USED FOR DESIGNING

Garbage is defined as number of unwanted outputs. A heavy price is paid for every garbage outputs.

A. New Gate

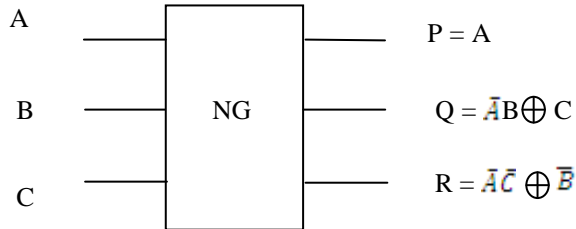


Fig.1 New Gate

B. New Toffoli Gate

It can be defined as $I_v = (A, B, C)$ and $O_v = (P=A, Q=A⊕B, R=AB⊕C)$ Where I_v and O_v are the input and output vector respectively [21].

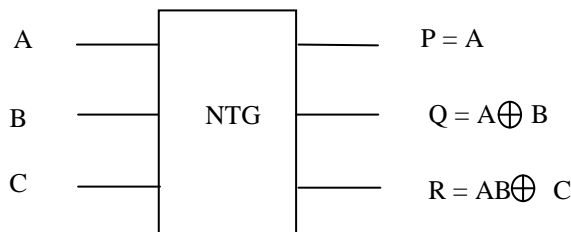


Fig.2 New Toffoli gate

C. TSG Gate

The TSG gate can implement all Boolean functions. One of the main functionality of the TSG gate is that it can work single as a reversible full adder.

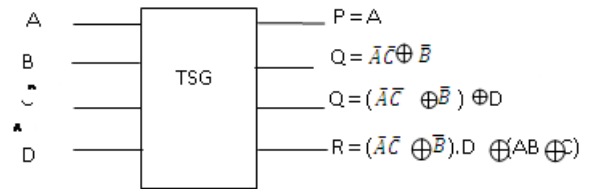


Fig.3 TSG Gate

VII. SYNTHESIS OF REVERSIBLE CIRCUITS

The main difference of synthesizing a circuit with reversible gates as compared to the standard conventional circuits is the following [21][22][23][24].

- The number of outputs of a logic gate is equal to the number of inputs
- Every gate output which is not used as input for a next gate or not used as a primary output is called as Garbage. If the output is left unattended or if the mirror circuit and spy gates are added.
- In reversible logic, outputs from one gate can be used as inputs to the next gate without fan-out of more than one.
- Feynman gates can be used as “copying circuits”, “spy circuits” to increase the fan-out.

VIII. APPLICATIONS OF REVERSIBLE CIRCUITS

The most prominent application of reversible logic lies in,

- Quantum computers
- Low power CMOS design
- Optical computing
- Nanotechnology

IX. DESIGN OF ADDERS

A. Design of a 4 bit BCD Adder

The designed 4-bit BCD adder Block diagram is shown in figure 4. In the circuit, 1-bit reversible full adder circuit is designed to construct a 4-bit parallel adder. Each of the full adder circuit produces two garbage outputs and therefore the total garbage output generated from the 4-bit parallel adder is 8.

In the circuit combinational logic circuit generates 3 garbage’s. Feynman gates which were used for copying bits in the existing circuit are not used in this circuit.

Combinational logic circuit itself generates the (S1, S2, S3) for the next processing. Therefore in this circuit 3 Feynman gates are reduced and hence the area on the chip is reduced. As a result, the total number of garbage outputs required to construct a reversible BCD adder is $2*8+3= 19$.

In this circuit, four reversible full adder circuits are used to construct a reversible 4-bit parallel adder. Total 8 reversible gates are required to construct a 4 bit reversible adder. 3 new gates are used in combinational logic of reversible BCD adder circuit. One Feynman gate is used for copying the result of combinational logic.



Total number of gates required to construct a reversible BCD adder is $2*8 + 3 + 1 = 20$.

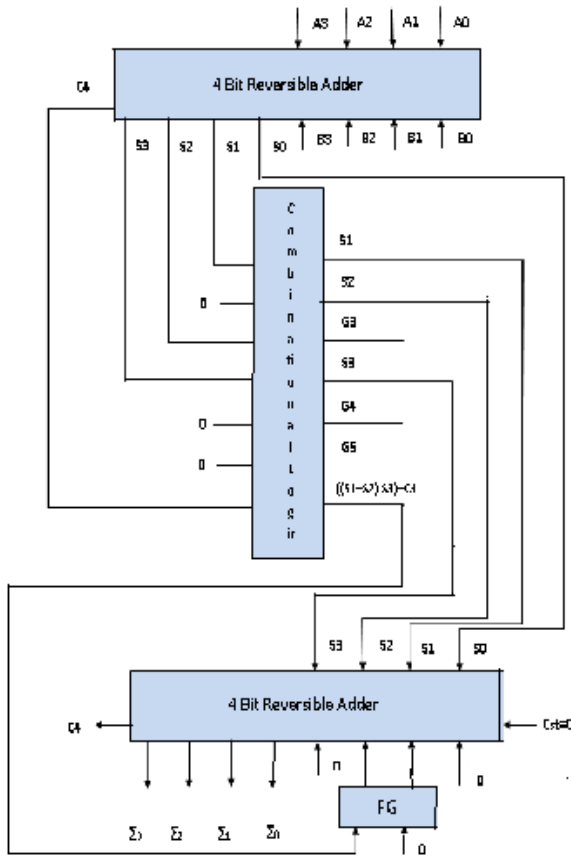


Fig.4 4-Bit BCD Adder

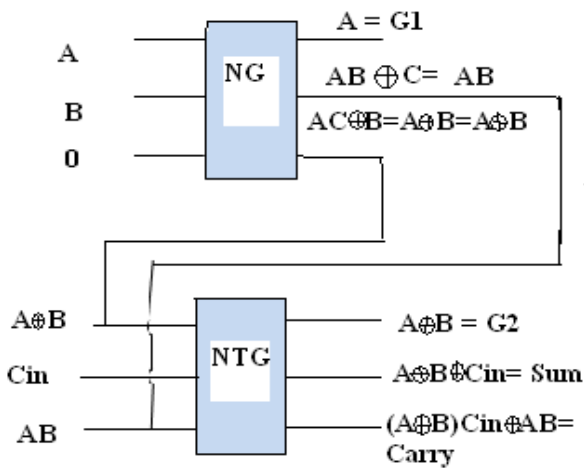


Fig.5 1-Bit Full Adder

For designing 1-bit full adder one new gate and one new Toffoli gate is used. Only Two reversible gates are used for designing 1 bit full adder. Design of full adder using these reversible gates produces only two garbage outputs.

B. Design of a 4 bit Parallel Adder

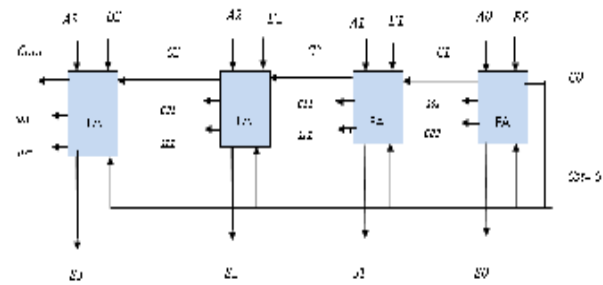


Fig.6 4-Bit Parallel Adder

A 1-Bit reversible full adder is cascaded to form 4-bit reversible parallel adder. Totally it uses 8 reversible gates and generates 8 garbage outputs.

C. Combinational Logic

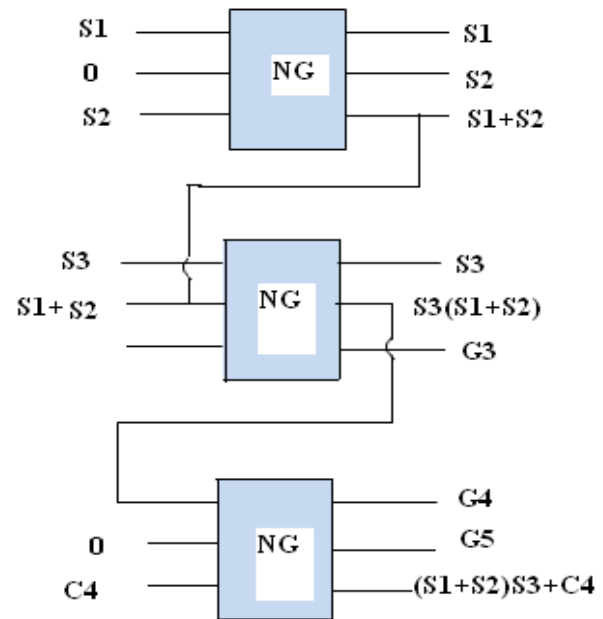


Fig.7 Combinational Logic

Combinational circuits are used in the design of BCD adder for the purpose of error correction. If the addition of the two numbers overflows. In the combinational logic, S3, S2, S1 and C4 should be checked for error correcting purpose. The equation will be directly control the error-correcting module $X = C4 + (S1+S2) S3$.

If x is 1, 0110(decimal 6) should be added with the previous addition result (S3, S2, S1, S0) to calculate the final result. If the carry is generated that directs the overflow of the addition. If X is 0, no modification will occur in the previous addition.

X. CARRY SKIP ADDER

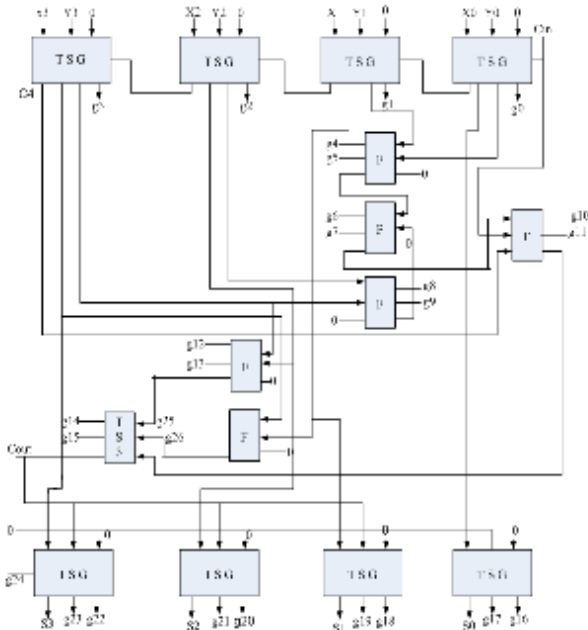


Fig.8 Carry Skip Adder

Figure 8 shows the block diagram of the carry skip BCD adder which constructed using the TSG gates and Fredkin gates (F).

The 3 Fredkin gates in the middle used to perform the AND4 operation. This will generate the block propagate signal 'P'.

The single FG in the right side perform the AND-OR gate combination to create carry skip logic.

In this circuit, the FG propagates the block's carry input Cin to the next block if the block propagate the signal 'P' is one otherwise the most significant full adder carry C4 is propagated to the next block.

The novel proposed TS-3 gate helps in the realization of the 3 inputs XOR gate, with minimum of one reversible gate.

It can also helps in avoiding the problem of fan out, as two of the inputs are directly passed as outputs. The proposed reversible carry skip BCD adder is still better compared to the reversible implementation of the conventional BCD adder in terms of the gates used for the designing.

The time saving in the proposed carry skip adder is significant compared to the conventional BCD adder. This is due to the skipping and this feature is not available for the conventional BCD adder.

XI. RESULT AND ANALYSIS

A. Top level (4-bit BCD Adder) (Refer to Figure 9)

- A 4-Bit BCD adder is a special type adder that adds two BCD numbers and converts the result into its equivalent BCD number.
- Give 4 bit inputs to a and b.
- Example: Give the input data, a = 0101(5 in decimal) and b = 0101(5 in decimal) as shown the simulation results.
- The addition of a and b is 1010 (10 in decimal), as it is a BCD adder this 1010 is converted in to 0001 0000 by BCD adder.
- Therefore the output, sum is 0000 and carry (Cout) is

0001 which is shown in the simulation result Figure 9 for top level BCD adder.

B. 4-Bit Carry Skip BCD adder (Figure 10)

- The carry skip adder constructed with first full adder block consisting of 4 full adders can generate the output carry Cout instantaneously depending on the input signal Cin without waiting for the carry to propagate.
- In the single bit full adder operation, if either of the input is a logical one, the cell will propagate the carry input to its output. When the p is one, it will make the carry input 'Cin' to propagate as the carry output 'Cout' of the BCD adder, without waiting for the actual propagation of the delay.
- If Cout is 1 then binary 0110 is added to the binary sum. Then final Sum and Carry is obtained.
- Example: a = 0001(1 in decimal) b = 1001(9 in decimal).The result obtained is sum = 1010 (10 in decimal).As sum exceeds 9 so 0110(6 in decimal) is added Hence the sum = 0 and Cout = 1 is shown in the simulation result.

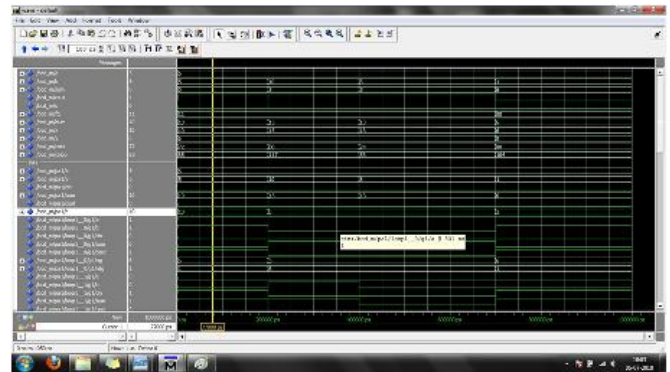


Fig.9 Simulation of 4-Bit BCD Adder



Fig.10 Simulation of Carry Skip Adder

The project entitled “FPGA implementation of optimized 4-bit BCD adder and Carry Skip Adder using reversible logic” has been undertaken to optimize the existing circuit using reversible gates in terms gates and garbage outputs. The design of the 4 Bit BCD adder is done in such way that it uses the less number of gates and produces the less number of garbage outputs. Since less number of gates are used in the design, area used on the chip is reduced and subsequently delay is also reduced. The optimized 4-bit BCD adder and existing 4-bit Carry skip adder is implemented on FPGA



Table 1.1 Comparative Analysis of the Reversible BCD Adders

	No of reversible gate used	No of garbage output produced
Proposed reversible conventional BCD adder	20	19
Existing reversible conventional BCD adder	23	22

XII. CONCLUSION AND FUTURE WORK

The designed 4-bit BCD and implemented carry skip adder circuit is one of the contributions of reversible logic. These circuits can further be used in a large reversible system as a module of reversible logic. In future, there is a plan to construct large reversible system that executes more than one reversible operation concurrently.

The designed circuit can be used for designing large reversible systems which is the necessary requirement of quantum computers, since quantum computers must be built from reversible components. Thus the project provides the initial threshold to build more complex systems which can execute more complicated operations.

This project work on the reversible BCD circuits designed and proposed form the basis of the decimal ALU of the primitive quantum CPU

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