

Command Mode Decoding Logic for Bus Management Unit

Nidhi Singh, Devendra Singh, Minakshi Sanadhya

Abstract: Command Processing Logic is command execution in spacecraft. The commands and the clock extracted from incoming signal are sent to the command processing logic. The commands are transmitted with redundancy and with encoding. Each command is transmitted four times. To detect error in commands encoding is used. The command processing logic should take care of redundancy and also should extract the correct command bit from the incoming bit stream. Once correct command is detected the command processing logic produce an authentic pulse. With the rising edge of the authentic pulse, the commands are stored in an auxiliary register. The command processing logic also contains the logic to produce pulse commands. Command Decoding Logic the command decoder extracts the command information, the message bits and stores it in auxiliary register which can be read using CPU. The command decoder then checks for the command bits and produce the pulse commands.

Keywords : VHDL, auxiliary register, command decoder, pulse commands, authentic pulse, BMU, command processing logic, Command Decoding Logic

I. INTRODUCTION

Main objective of Project is to do VHDL coding of command mode decoding Logic for BMU , As the Project was aimed to implement on ASIC/FPGA, since the system is realized using VHDL, miniaturization is achieved along with good performance, improved reliability and flexibility in terms of future improvements. The design can be targeted on to any family of ASIC/FPGA.

The study of Command Processing Logic for Space Application was successfully carried out as the first step. Study of VHDL coding and design tools was next step, successfully coded, simulated and synthesized design.

The scope for the future developments is, since the design is implemented using VHDL code, it is easy to add new features and design is target independent.

The command bits are sent in a definite format from the ground station. The commands are sends as messages. Each message contains four commands, which contain same command information. Each command is send four times for redundancy purpose. There is a gap of 500 ms between the messages and 100 ms between frames where no information is send. Each frame contains 32 data bits and 6 parity bits, By comparing the parity bits generated from the frame with received parity, We will be able to decide whether the command bit are received properly or not. If the command

bits are not received properly, then that frame is discarded and checks for next frame. With the first frame which received correctly we generate an authentic pulse signal to indicate that the command is received correctly.

Once the authentic pulse is generated the command bits are stored in an auxiliary register. This can be read from an output port. The command bits can be taken into processor and can be used for telemetry purpose.

II. FUNCTIONAL REQUIREMENT AND PROCEDURAL DESIGN

2.1- Command Decoding Logic

The 54 bits is transferred using burst clock (40 KHz), data and Latch pulse. This module receives command frame from Link #1 and Link #2. Both command frames decoded independently and both decode output Ored finally to get final output. The complete block diagram of command mode decoding logic is shown in fig2.1

2.1.1Qualifier

This block checks for I/P signal pulse width for 3 and 1/2 clock width. If the signal satisfies this condition, this block will generate output otherwise blocks the input signal. The qualifier block diagram is shown in fig 2.1.1.1

State diagram shown below shows five states for functionality of qualifier block states are change on falling edge of clk. Fig 2.1.1.2

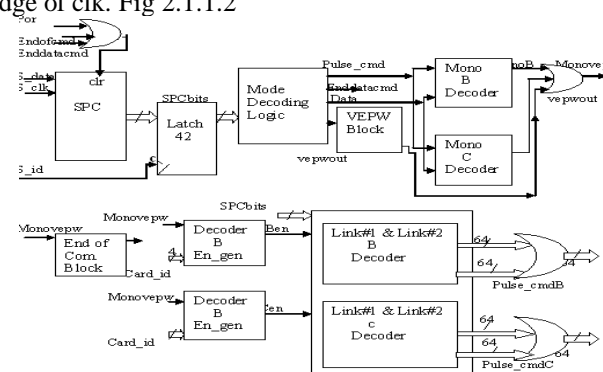


Figure2.1

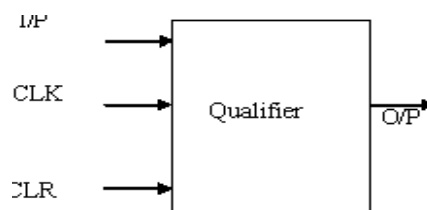


Figure2.1.1.1

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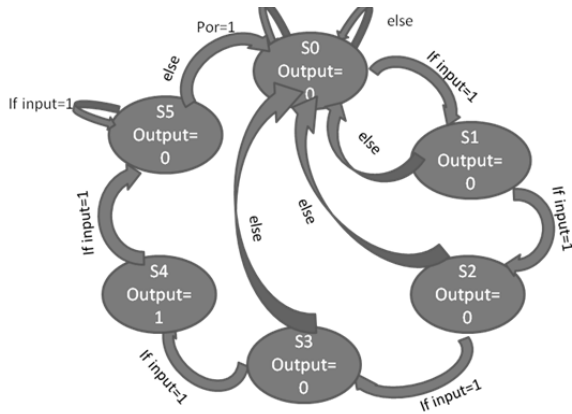


Figure 2.1.1.2

2.1.2- 42 bit-SPC

This block converts serial data stream into parallel data stream. The parallel data stream is latched into 42-bit latch with rising edge of strobe signal fig 2.1.2.1

2.1.3-Delay Pulse

This block generates pulse of 2 clock width. The delay pulse block details are shown in following fig.2.1.3.1 and state diagram in fig 2.1.3.2

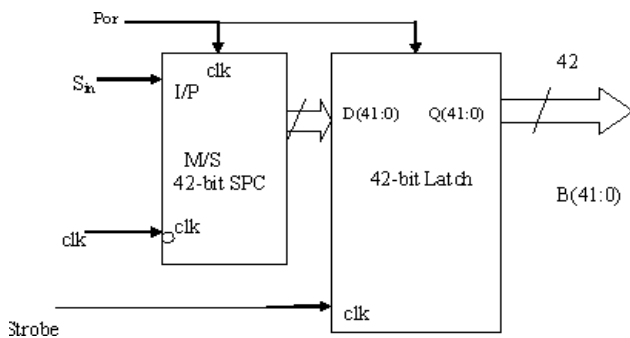


Figure2.1.2.1

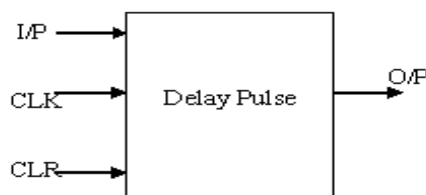


Figure 2.1.3.1

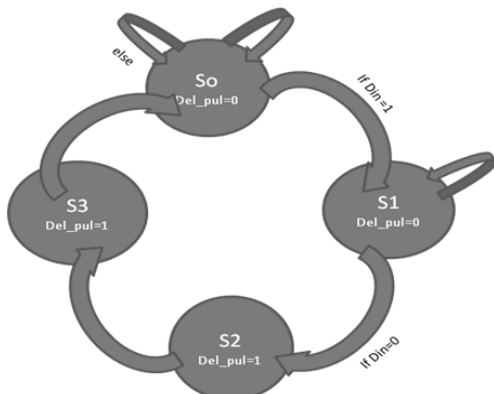


Figure2.1.2.2

2.1.4 Pulse command mode generation

The block checks for pulse command mode and card-id bits are specified independently for B & C decoder. Once these bits match, generates separate enable signal for mono of B & C decoder. In addition to this it will generate Bcard & Ccard flag whenever card-id bit matches with command card-id bits. The pulse command mode generation details are shown in fig 2.1.4.1 below.

2.1.5 Mono Generation Block

The mono block generates pulse of different pulse width depending upon selection bits. The mono generation block diagram shown in fig.2.1.5.1

Fig 2.1.5.2 shows state diagram for functionality of mono generation block. It contains four states and state is change on rising edge of CLK 1ms. For implementation of mono generation block contains one counter also. Counter starts counting on falling edge of clock 1 ms, load signal used as enable for counting and Por signal used to clear the counter.

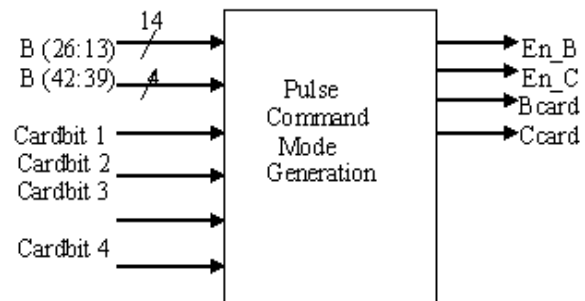


Figure 2.1.4.1

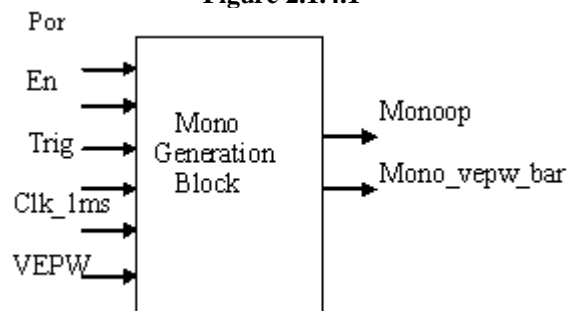


Figure2.1.5.1

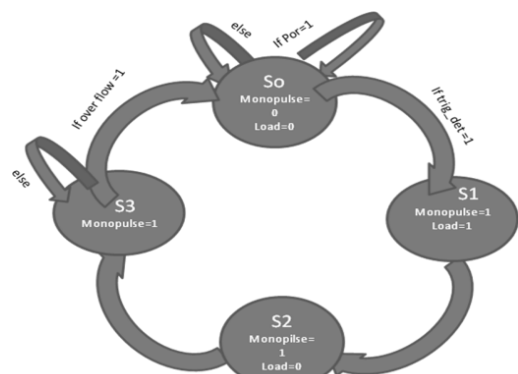


Figure2.1.5.2

2.1.6 Decoder Enable Generation

This block generates enable signal for decoder whenever system-id of BMU matches

with command sys-id bits. The decoder enable generation details are shown in following fig2.1.6.1

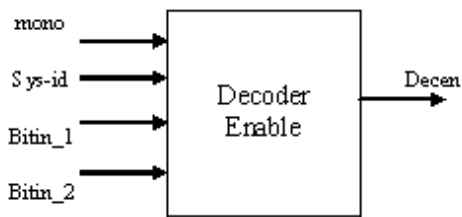


Figure3.1.6.1

2.1.7 End of Data Command Generation Block Introduction

This block decodes data command mode. Whenever, encounters this mode, enable 40 ms timer. At the end of timer flag, generates 3 clock width reset signal to clear 42-bit command register. The details of end of data command block are shown in fig (2.1.7.1,2.1.7.2,2.1.7.3)

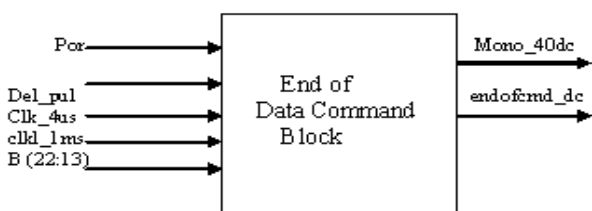


Figure2.1.7.1

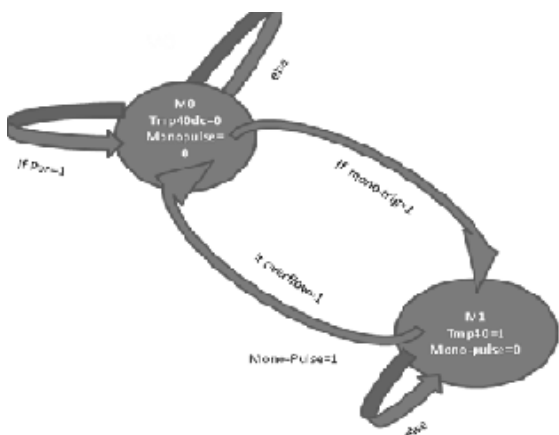


Figure2.1.7.2

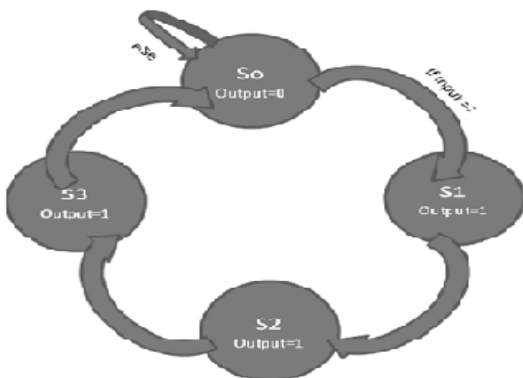


Figure2.1.7.3

2.1.8 Safe Mode Staggering Block Introduction

This block generates 15-staggered command whenever safe mode decodes these commands are pulse commands of 64ms

pulse width. The gap between two successive commands also 64ms. The first 8 SMP staggered commands can be enable or disable through commands. The details of safe mode staggering block are shown in fig 2.1.8.1.

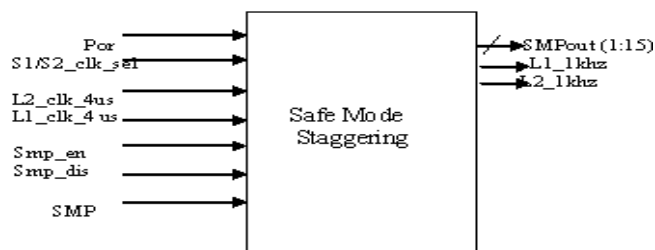


Figure2.1.8.1

2.1.9 Variable Executive Pulse width (VEPW) Block

The VEPW mode gives flexibility for having variable pulse width of commands. The VEPW pulse width is approximately-

$$\text{VEPW Command pulse width} \approx (n-1) 23 \text{ ms} + 49 \text{ ms}$$

Where 'n' is number of commands

The VEPW block contain 49 ms timer. The first VEPW commands enables VEPW timer. Whenever it encounters next VEPW command before completing set time, VEPW timer gets retrigger. This way variable pulse width is achieved. The details of VEPW block is shown in following fig2.1.9.1 The VEPW block contain two State diagrams fig-(2.1.9.2, 2.1.9.3)

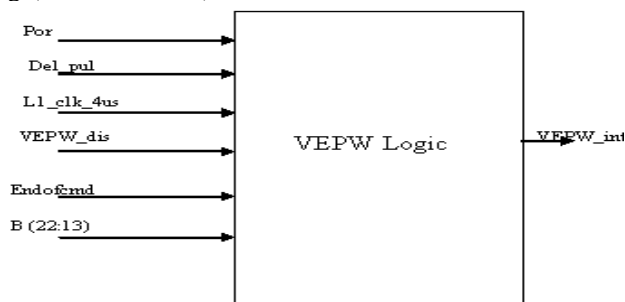


Figure2.1.9.1

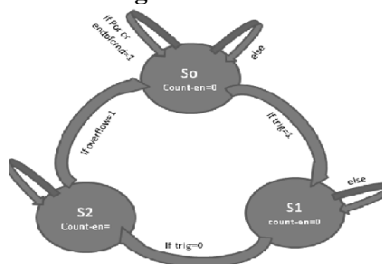


Figure2.1.9.2

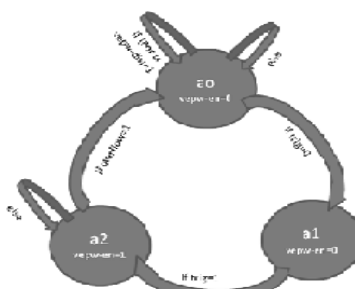


Figure2.1.9.3

2.1.10 Main Decoder

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The decoding is done in two levels. It is shown in following figure2.1.10.1

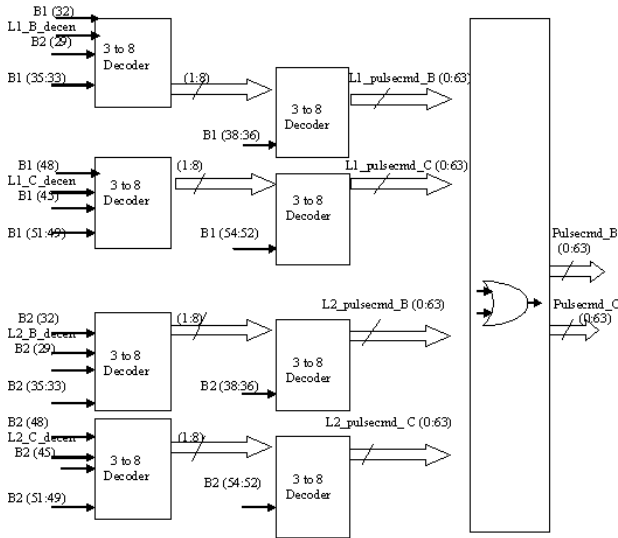


Figure2.1.10.1

2.1.11 End of Command Block Introduction

At the end of pulse, generates 3 clock width reset signal to clear 42 bit command register. The details of end of command block are shown in following fig3.1.11.1. in fig 3.1.11.2 FSM shows states of end of command block it contains four states and states are change on rising edge of clock 4 us.

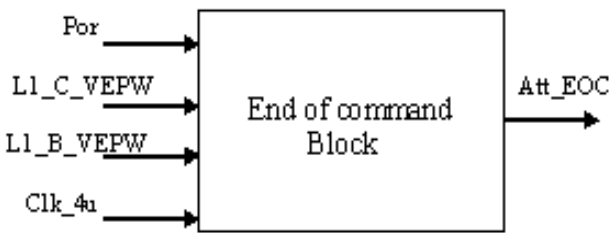


Figure2.1.11.1

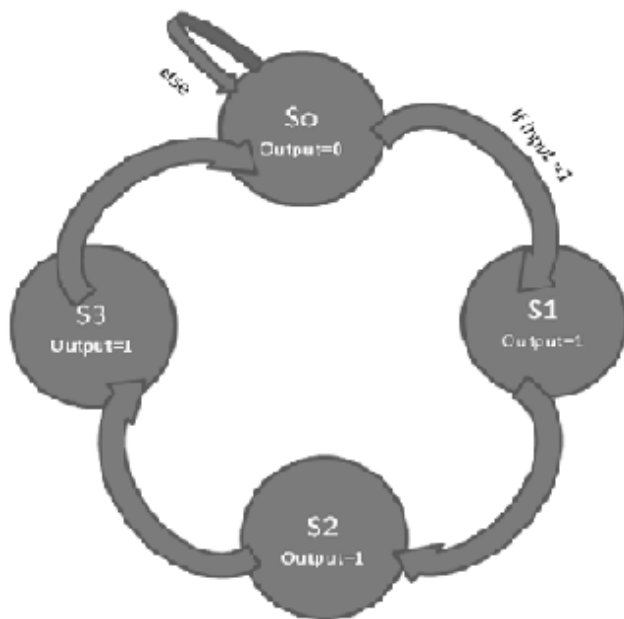


Figure2.1.11.2

3-Results

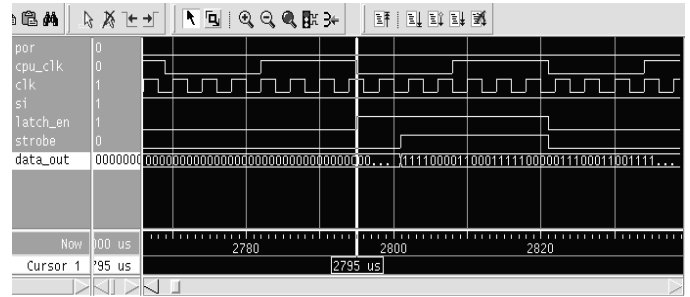


Fig3.1- 42-bit SPC block wave form



Fig3.2- Variable Executive Pulse Width (VEPW) block wave form

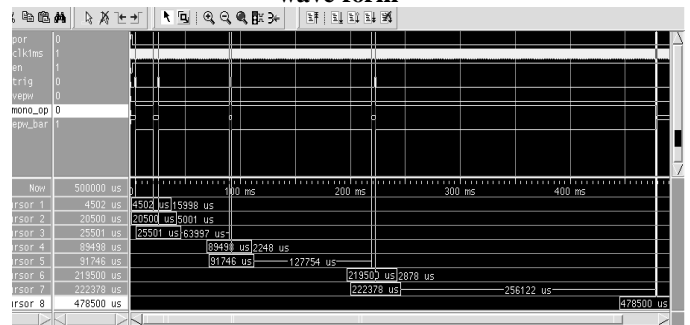


Fig 3.3 -Mono Pulse Generation block Waveform

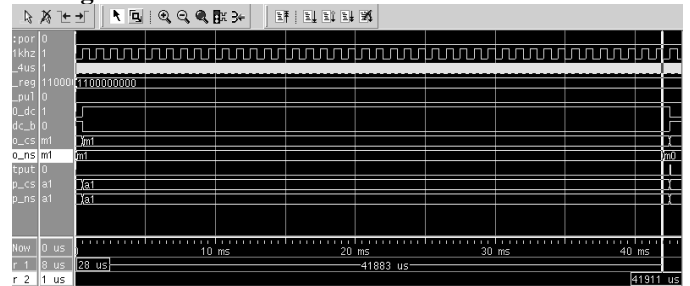


Fig 3.4- End of data command generation block signal

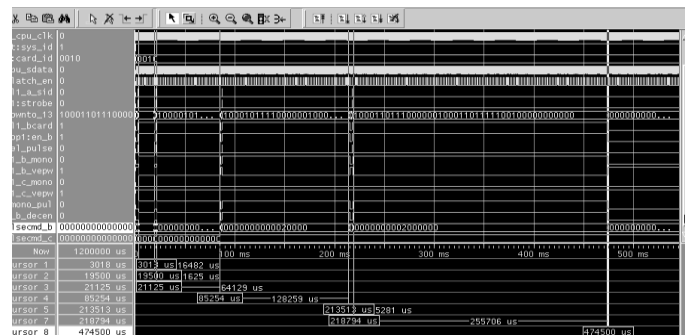


Fig 3.5- Pulse commands when Mono B decoder block is active (First test case)



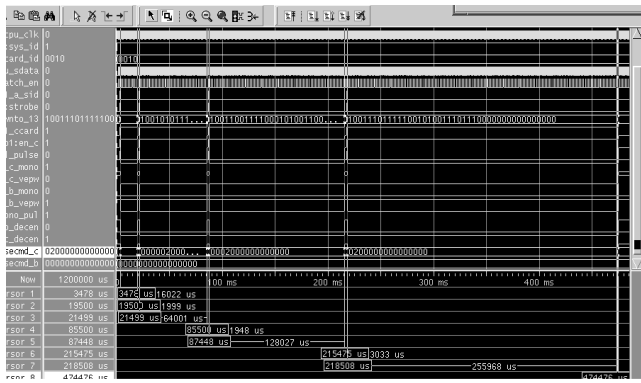


Fig 3.6- Pulse commands when Mono C decoder block is active(Second test case)

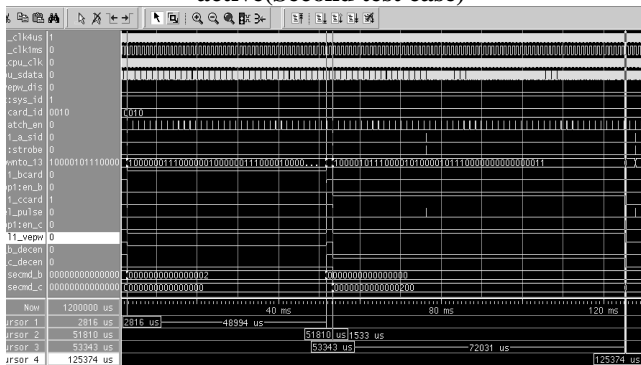


Fig 3.7- Pulse commands when VEPW block is active (Third test case)

III. CONCLUSION

Main objective of Project is to do VHDL coding of command mode decoding Logic for BMU , As the Project was aimed to implement on ASIC/FPGA, since the system is realized using VHDL, miniaturization is achieved along with good performance, improved reliability and flexibility in terms of future improvements. The design can be targeted on to any family of ASIC/FPGA.

The study of Command Processing Logic for Space Application was successfully carried out as the first step. Study of VHDL coding and design tools was next step, successfully coded, simulated and synthesized design.

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