

NoC Based Approach to Enhance the Existing Network Architecture

Saurabh Yadav, Ajay Kumar Singh

Abstract— Now a day's performance is really one of the greatest issue. We want to send the packet from source to destination with a highest throughput, even though there is any fault in the intermediate node or router we don't want to compromise with the packet loss as it leads to wastage of bandwidth. In this paper we have tried to improve the architecture of existing system. That yield better performance, in order to improve the performance we have taken the approach of shortest path.

Index Terms—Dijkstra Algorithm, NoC, Packet Switching, Pyramid Network, Topology.

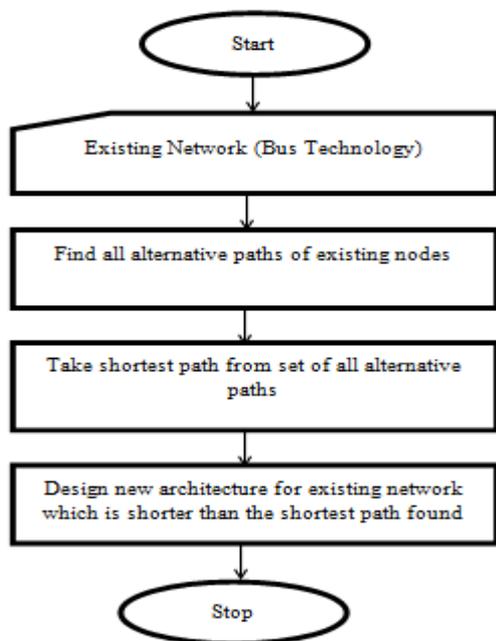


Fig. 1 Shows the Flow Chart of Whole System

I. INTRODUCTION

Speed is one of the greatest factor for measuring the performance of the system. How to process two or more jobs parallelly, if we have pretty good number of processor interlinked with each other. Many parallel algorithms are existing now a day's so one can choose any of them. Modules of traditional systems are connected by common bus [1]. This is very old technology and it has some serious disadvantages like performance of circuit delays between the system modules. In common bus technology only two modules can communicate.

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Saurabh Yadav, Computer Science Engineering, Meerut Institute of Engineering and Technology, Meerut, India

Dr. Ajay Kumar Singh, Computer Science Engineering, Meerut Institute of Engineering and Technology, Meerut, India

Network on chip (NoC) [2] is the solution of above problem. In this, modules can communicate each other's by packet transfer. Different modules are arranged as different type of network topologies like 2-D Mesh, Tree, Pyramid, Cube-Connected Cycles Network (CCC) etc. In NoC fashion system, performance is good as compared to traditional bus systems. The entire process is shown in figure1.

II. MESH TOPOLOGY

In mesh network the modules are arranged into q-dimensional (D) lattice.

So, for a 2-D mesh network:-

$$\begin{aligned} \text{Diameter} &= q*(k-1) \\ &= 2*3 \text{ since } (q=2, k=4) \\ &= 6 \end{aligned}$$

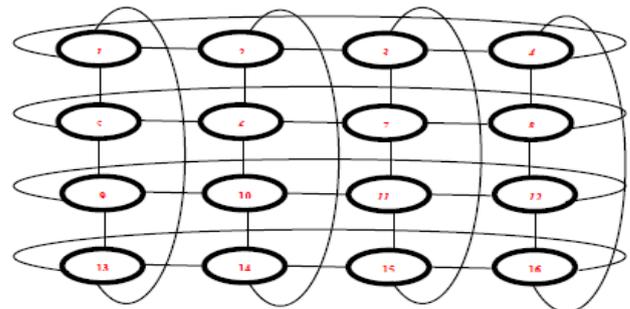


Fig. 2 2-D Mesh with 4 Modules Each Dimension

Direct Communication in mesh network [3] is allowed only between neighbouring modules so any internal node can communicate directly with maximum 2q other modules. In 2-D mesh, where dimension q=2, a module can communicate with 4 other modules with network size k^q where k is number of modules along each dimension and q is the dimension. The diameter of 2-D mesh is six according to formula q*(k-1). When there is wrap – around connections between modules it becomes 2-D TORUS which decreases the diameter of mesh network.

As shown below in figure 2 and its corresponding graph in figure 3.

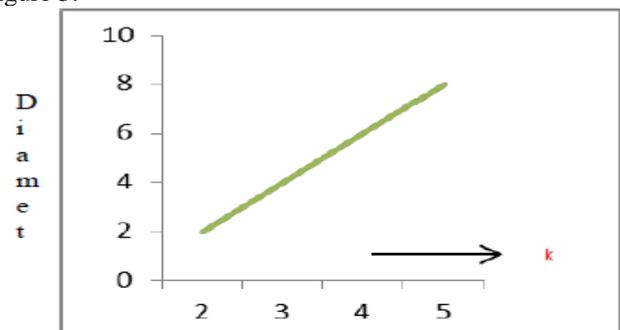


Fig. 3 Graph for Diameter of Mesh when q=2

III. TREE TOPOLOGY

In a tree model, there is only one path between any pair of modules as shown in figure 4. A completely balanced binary tree of depth $k-1$ has 2^k-1 modules. Any interior module can communicate directly only with maximum three other modules i.e one parent module and two child module [4]. Tree has only one root with one left sub tree and right sub tree.

$$\begin{aligned} \text{Diameter} &= 2*(k-1) \\ &= 2*(4-1) \text{ since } (k=4) \\ &= 6. \end{aligned}$$

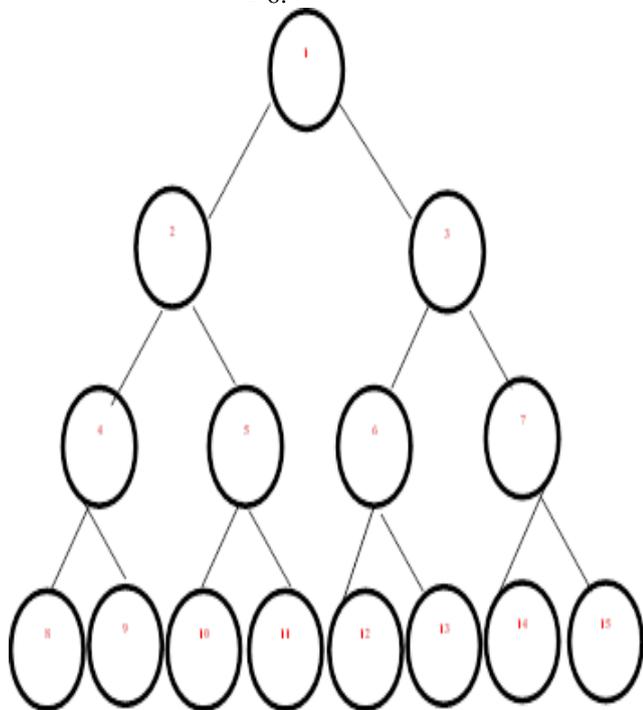


Fig. 4 Complete Binary Tree with k=4

IV. PYRAMID TOPOLOGY

Pyramid network [5] is combination of mesh and tree networks so it has the advantages of both types of networks. A pyramid network of size k^2 has its base 2-D mesh which contains k^2 modules. A pyramid of k^2 modules is a complete 4-ary rooted tree with height $\log_2 k$. It is augmented with extra inter-modules links so that modules in every tree level form a 2-D mesh.

It is shown in figure 5 and its corresponding graph between Diameter and k is given in figure 6.

Base of pyramid has level 0 and level increased in upward direction so single module at Apex (top) of pyramid has level $\log_2 k$ with diameter $2*\log_2 k$. A module can communicate directly with maximum nine other modules. One is its parent, four mesh neighbors and four children. So, for pyramid size $k^2=16$

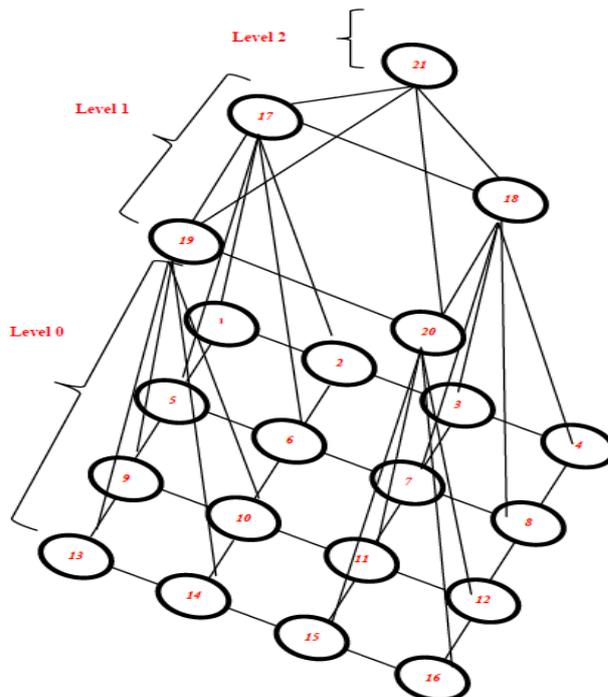


Fig. 5 Pyramid Network with k=4

$$\begin{aligned} \text{Diameter} &= 2*\log_2 k \\ &= 2*2 \text{ since } k=4 \\ &= 4. \end{aligned}$$

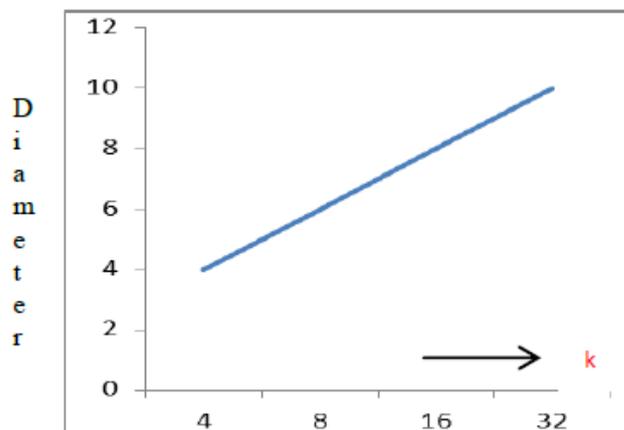


Fig. 6 Graph for diameter of pyramid network

V. COST EVALUATION

The earlier research was done in NoC field is based on mesh type networks. In which modules are placed at the intersection point of links of network so that many modules can communicate at same time. If a 2-D mesh is converted to 2-D TORUS then diameter is decreased by warp around connection of links. For example, in figure below, module no.13 needs to communicate with module number 8, then there is too many choice to route the packet [6] but best route is 13-19-21-18-8 with cost 4 instead of other routes which have cost more then 4 it is illustrated in figure 7.

Assuming each path has same weight i.e. 1. In the Same way, if module no.1 needs to communicate with module no. 14 then by using warp around connection it can reach to destination with cost 2 only.

VI. PROPOSED SOLUTION

When a pyramid network is used instead of a mesh network then a good advantage is get over 2-D mesh that is reduced the diameter of network by which more speed and performance is achieved in systems.

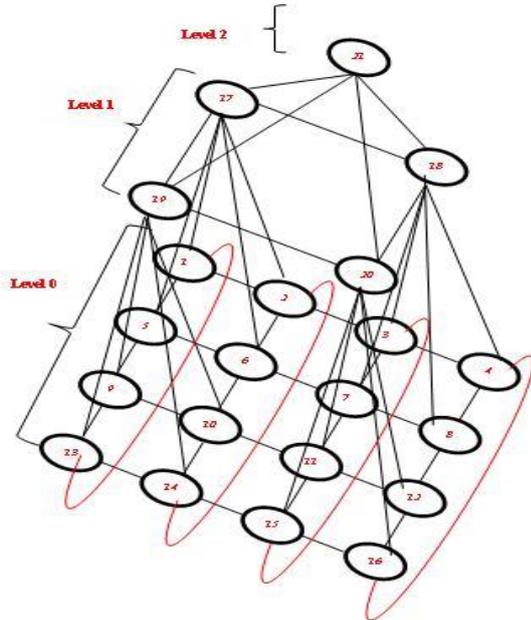


Fig. 7 Pyramid Network with Each Level Mesh is 2-D TOURS

Because when in a mesh network a module sent a message to other module which is on the side of the module like -communicating modules are opposite diagonal modules. In mesh network message have to traverse $q*(k-1)$ links. But when same thing is done by pyramid network then a packet can go by moving upward direction and then taking down to reach the destination by traversing fewer links a clear picture is shown in figure 7. So by using pyramid network with warp around connections of its mesh a greater speed is achieved. Architecture [7] of entire system can be improved by putting wire in wraparound fashion. Red line shows wraparound connections of mesh in figure 7.

VII. GENERALIZED PACKET FORMAT

Communication between modules takes place by sending and receiving the packets across the network. The packet format is given below in figure 8, which is used in this framework.

Destination address (m bits)	Source address (m bits)	Data bits (k)
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Fig. 8 Packet Format

Destination address is followed by source address then the Data bits. The basic components in generalized packet format [8]. The size of module address depends upon the number of modules in system plus level bits. So the size of packet will be $2m+k$ bits.

VIII. INTERCONNECTION

A set of three wires is used to connection of modules. Three wires corresponds to request (REQ), acknowledgement (ACK) and data (D). The figure 9 below depicts the interconnection between modules.

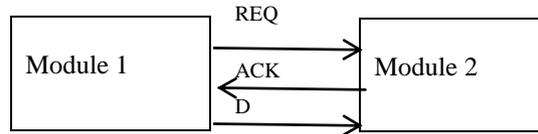


Fig. 9 Data Transfer Process

IX. MODULE DESIGN

A module or node is a part of whole system which is has a certain functionality to complete the full system task. A module is designed in such a way that it can communicate with all of its neighbors at same time so it have equal interfaces to its neighbors. Module may be a router to communicate with others and pass the packets [9].

In this approach a module can have maximum nine interfaces i.e. pyramid network [10] property and as shown in figure 10. A module/router may use any no. of interfaces at any time from nine interfaces. A module can plug in on NoC [11].

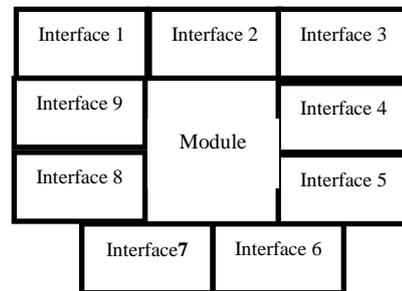


Fig. 10 Interface of Module

X. INTERFACE DESIGN

In each interface two circular buffers is used for sending and receiving packets. It store and forward the packets, as soon as packet reach to interface [12], it have two temporary registers, one is busy bit and other is counter register. Interface is used for taking the decision about packets. What to do with this packet? A packet which is sent to interface is stored in temporary register s and checked in the routing logic, and then it is forwarded to next interface along its destination. Over all interfaces is checked by control logic, busy bit etc.

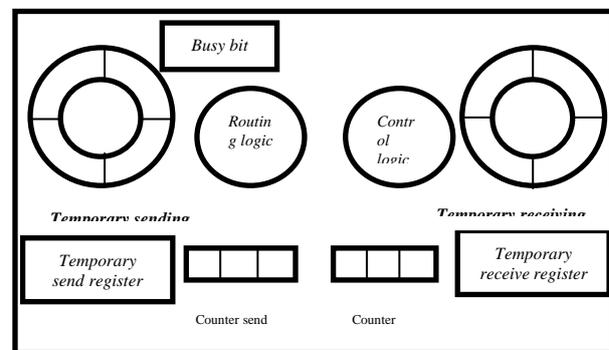


Fig. 11 Interface

XI. WORKING

The basic work of network on chip [13] is to send packet across the topology to the destination. After receiving the packet, destination processed it. When a module wants to send a packet to adjacent module, then it first sends a request signal to receiving module and waits for its reply. The signal receiving module then checks for busy bit and receiving buffer. If busy bit is not set and receiving buffer is not full then it first set the busy bit and sends an acknowledgement to request signal sending module. After getting acknowledgement, the sending module sends the data packet and receiving module store it in its temporary register and forwards it to destination.

XII. CONTROL LOGIC

Control logic does the checking of busy bit and status of buffer. By this it is decided to whether the interface can receive packet or not.

XIII. ROUTING LOGIC

Each packet have two address one source address and other destination address as shown in figure 8. So for routing [14] Dijkstra's algorithm is used for finding the shortest path between two modules. When a module forwards a packet to another module, at that time that module first checks the best path according to dijkstra's algorithm. Dijkstra's algorithm provide shortest path when in network edge or link wait or cost is given.

XIV. BUFFER

Circular queues is used to implement the sending and receiving buffers the following pseudo code is used to insert the data from temporary register in to queue-

```

if (rear==max-1)
    rear ← 0;
else
    begin
        rear ← rear+1;
        if (rear == front)
            rear ← rear-1;
    end
    q[rear] ← TempReg;

```

XV. STATUS BITS

Packet is stored in to the receiving buffer, status bit is incremented and decremented whenever deleted for the forwarding it to the next interface. Same logic is also used in the send buffer.

XVI. CONCLUSION

We have shown how we can improve the performance of the system if we put the entire system on the chip. The problem that may be faced is collision of packets among each other, which leads to rise in temperature of IC. Packets may be transmitted using radio signal wirelessly among different components of IC. Since wire or PCB is not involved, it increases the throughput of the entire system.

Performance is directly proportional to rise of temperature. This can further be used in parallel computing.

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Saurabh Yadav: Born in 1989 in Bulandshahr, Uttar Pradesh, India. He has completed his B.Tech with Information Technology (2010) from Radha Govind Engineering College Meerut, Uttar Pradesh. He is currently pursuing M.Tech with Computer Science Engineering from Meerut Institute of Engineering And Technology (MIET), Meerut, Uttar Pradesh, India. He has published 2 papers in international Journals. He is IBM DB2 certified DBA.



Dr. Ajay Kumar Singh: Born in 1974 at Dhanbad (Jharkhand). He had done B.E (Computer Science & Engg.) from Kumaon Engineering College, M. Tech (I.T) Allahabad, Ph. D (Computer Science & Engg.) Jaypee University of Information Technology. Work Experience: He had been in different institution / university like Radha Govind Engineering College, Meerut, (U.P), Sir Padampat Singhania University, Bhatnagar, Udaipur, Rajasthan, Jaypee University of Information Technology, Wagnaghat, Solan (H.P), Mody College of Engineering and Technology, Lakshmangarh, Sikar, Rajasthan, Regional Engineering College (Now N.I.T.) Kurukshetra (Haryana), Software Solution Integrated Ltd. (Delhi), Computer Centre CMC. Now he is working with MIET, Meerut, U. P. He has published 8 papers in international Journals like PIER, Asia Magazine EFY Elsevier, JSIP, 8 papers in international Conference out of which 4 of them in IEEE, Published 4 papers in National Conferences, 1 in EFY and presented his papers at Bangalore, Pune, IT B.H.U, USA (Washington DC).

