Effect of Thickness and Material on Electronic Properties of GAA-MuGFETs

Himani Malik, Amarjeet Kaur, Asha Lather, V.K.Lamba, Bhupesh Kharb

Abstract— ***We present a CMOS compatible n-type gate-all-around (GAA) silicon nanowire (NW) MOSFETs with excellent electrostatic scaling. This paper investigates the sensitivity of gate-all-around (GAA) nanowire (NW) to process variations in silicon film thickness and material i.e. Si and Ge with multigate devices using analytical solutions of Poisson's equation verified with device simulation Our study indicates that the GAA nanowire (NW) has the smallest threshold voltage (Vth) dispersion caused by process variations in silicon film thickness. Specifically, the GAA NW shows better immunity to channel thickness variation than multigate devices because of its inherently superior surrounding gate structure. To explore the optimum design space for (GAA) silicon nanowire (NW) MOSFETs were performed with three variable device parameters: channel width, material, and silicon film thickness. The efficiency of the GAA gate structures is shown to be dependent of these parameters.***

Index Terms— ***GAA gate FETs, MOS devices***

I. INTRODUCTION

Until recently, many performance metrics (i.e. speed, total harmonic distortion, etc.) of the conventional MOSFET have generally improved with each scaling. But as channel lengths approach and fall below 100 nm, new characteristics are observed; many of them are undesirable. During the last few decades, an extraordinary effort has been made to improve semiconductor-device features while reducing their dimensions. However, the miniaturization of traditional bulk CMOS transistors is reaching fundamental limits that, eventually, could slow down this trend. In order to follow the predictions of the International Technology Roadmap for Semiconductors [1], new materials and architectures have been proposed.

FULLY-depleted (FD) SOI MOSFETs are very attractive for sub-100 nm CMOS applications because of their steep sub-threshold slope and a low body effect coefficient. SOI microprocessors with a 22% speed improvement over bulk have been reported recently [1]. FDSOI MOSFETs with a gate length of 50 nm and a switching speed less than a picosecond [2] have been reported.

Manuscript received September 02, 2012.

Er. Himani Malik, Electronics& Communication Engg., HCTM, Kaithal, India.

Er. Amarjeet Kaur, Electronics& Communication Engg., ACME, Faridabad, India

Er. Asha Lather, Electronics& Communication Engg., HCTM, Kaithal, India.

Dr. V.K. Lamba, Electronics& Communication Engg., HCTM, Kaithal, India.

Er. Bhupesh Kharb, Electronics& Communication Engg., GITM, Gurgaon, India.

To minimize short channel effects and to maintain full depletion if the doping concentration in the channel region is increased, the silicon film thickness must be scaled down with gate length. While devices made in films thicker than 20 nm have excellent mobility and current drive characteristics, significant mobility degradation is observed in devices made using a silicon film thickness less than 10 nm [3]. If a metal gate is used instead of N poly-silicon the doping concentration in the film can be reduced, while allows for fully depleted operation in thicker silicon films. This decrease of doping concentration, however, degrades the short channel characteristics. A possible solution is multiple-gate structure devices have been reported. Such multiple-gate devices include, double gate, triple-gate and quadruple-gate structures (i.e. GAA- gate) When the silicon body is completely surrounded by the gate contact, the resulting structure is known as GAA [9]. It is well known that the double-gate (top and bottom gate) silicon-on-insulator (SOI) MOSFET and the gate-all-around device are the most suitable device structures for suppressing short-channel effects and subthreshold slope degradation [4], [5], [6].

II. THEORY

In the present simulation, the silicon island is assumed to have a rectangular cross section and the gate oxide has a uniform thickness in all devices (It is assumed that there is no gate oxide thinning at the edges of the silicon island.) In thin-film quadruple-gate devices(GAA gate) operating in the sub-threshold region most carriers flow through the middle of the film due to the volume inversion. Fig. 5.17 shows that the threshold voltage of GAA-gate devices increases when the channel width is increased. Even though the use of thin silicon film increases the source and drain resistance, a small silicon film thickness is required to improve the SCE immunity and sub-threshold slope. If the silicon film is ultra thin, energy quantization effects start to appear, which influence the threshold voltage and the I-V characteristics of SOI MOS devices Fig. 5.19 shows the threshold voltage as a function of film thickness of GAA gate structure. This graph shows the threshold voltage is almost constant for the GAA-gate MOSFET

III. DEVICE SIMULATION

Device electrical characteristics were simulated using the Omen Nanowire software from nanohub. In thin-film quadruple-gate devices(GAA gate) operating in the sub-threshold region most carriers flow through the middle

Published By:
Blue Eyes Intelligence Engineering
& Sciences Publication

of the film due to the volume inversion.. In order to explore the design space for GAA gate structures, simulations were performed with variables of four device parameters such as channel width, material, and silicon film thickness. Simulations were performed for channel widths of 10nm, 20 nm, 30 nm, and 40 nm. The thickness of the silicon film, varies from 10 nm to 40 nm. Even though the use of thin silicon film increases the source and drain resistance, a small silicon film thickness is required to improve the SCE immunity and sub-threshold slope. If the silicon film is ultra thin, energy quantization effects start to appear, which influence the threshold voltage and the I-V characteristics of SOI MOS devicesThe simulated structures have a uniform doping concentration in the channel and source/drain region. Abrupt source and drain junctions are used to fix the effective gate length of the devices. The simulations were done using a single carrier, drift-diffusion model without impact ionization to focus on the electrostatic behavior. From the simulation results, the trans-conductance and drive current quadruple-gate (GAA gate) devices is approximately four times that of a single-gate device, as could be expected. Encroachment of electric field from drain on the channel region can be seen in the triple-gate device, but not in the GAA-gate devices. Therefore, it is expected that GAA-gate device can suppress effectively short channel effects and thus could be a promising candidate for future nanometer MOSFETs.

IV. RESULTS & DISCUSSION

A. Channel Width

In the present simulation, the silicon island is assumed to have a rectangular cross section and the gate oxide has a uniform thickness in all devices (It is assumed that there is no gate oxide thinning at the edges of the silicon island.) In thin-film quadruple-gate devices (GAA gate) operating in the sub-threshold region most carriers flow through the middle of the film due to the volume inversion. Fig. 1.1 shows that the threshold voltage of GAA-gate devices increases when the channel width is increased.

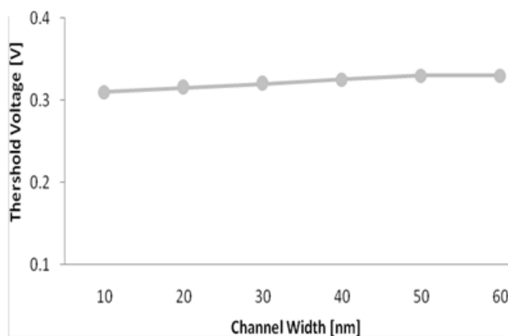


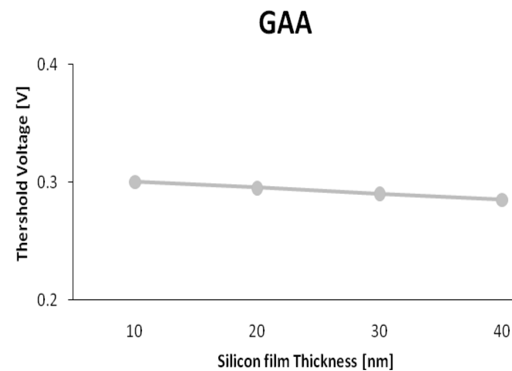
Figure 1.1: Threshold voltage in fully depleted GAA gate MOSFET with channel widths W=T_{Si} = 25 nm, $N_A = 1 \times 10^{18}$ cm^{-3}.

B. Silicon Film Thickness

Even though the use of thin silicon film increases the source and drain resistance, a small silicon film thickness is required to improve the SCE immunity and sub-threshold slope. If the silicon film is ultra thin, energy quantization effects start to appear, which influence the threshold voltage and the I-V characteristics of SOI MOS devices Fig. 1.2 shows the threshold voltage as a function of film thickness of GAA gate structure L and W are both equal to = 25 nm, and channel doping concentration, $N_A = 1 \times 10^{18}$ cm^{-3}. Similarly, it can be observed that the threshold voltage roll-off is minimized by the use of the quadruple-gate structure. This graph shows the threshold voltage is almost constant for the GAA-gate MOSFET.

Figure 1.2: Threshold voltage as a function of film thickness of GAA gate structure L and W are both equal to = 25 nm, and channel doping concentration, $N_A = 1 \times 10^{18}$ cm^{-3}*Film Thickness And Material*

In this, the current of GAA gate MOSFET is linearly varying with threshold voltage for 0.5nm thickness. But for 1nm and 2nm thickness the graph shows abrupt changes in current value, whenever the thickness of the film is greater than the twice the length of mean free path of electrons the charge transport takes place because of tunneling and hence we have sudden increase in current value for both Si and Ge material GAA gate MOSFETs.



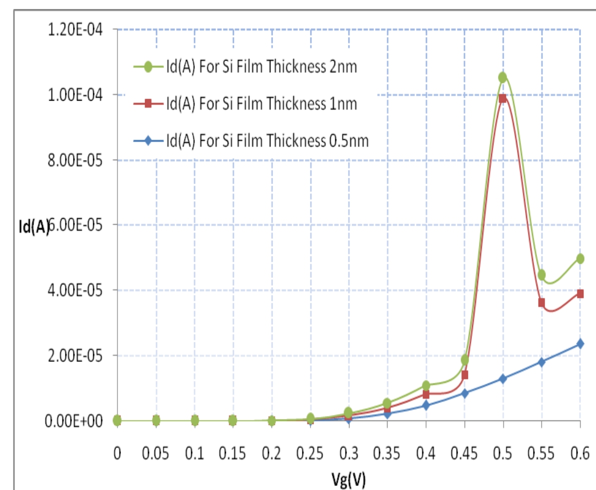


Figure 1.3: Current-Voltage Characteristics of Si Film for different thickness

Published By:
Blue Eyes Intelligence Engineering
& Sciences Publication

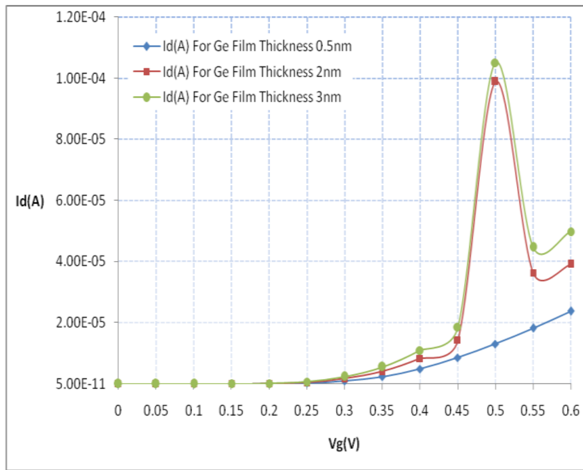


Figure 1.4: Current-Voltage Characteristics of Ge Film for different thickness

V. CONCLUSION

In summary, we have demonstrated Si/Ge n-type GAA-gate MOSFETs devices based on omen nanowire GAA with 10nm channel lengths shows excellent sub-threshold voltage and film thickness of 2nm shows good drain current. A very thin silicon film thickness of Si/Ge material of GAA-gate MOSFETs are expected to further enhance device ON current. This work projects GAA-gate MOSFETs as a promising successor of MOSFETs and for future energy efficient green electronics.

REFERENCES

1. S. B. Park, Y. W. Kim, Y. G. Ko, K. I. Kim, I. K. Kim, H. S. Kang, J. O. Yu, and K. P. Suh, “A 0.25-_m, 600 MHz, 1.5-V, fully depleted SOI CMOS 64-bit microprocessor,” IEEE J. Solid-State Circuits, vol. 34, pp. 1436–1445, 1999.
2. R. Chau, J. Kavalieros, B. Roberds, A. Murthy, B. Doyle, D. Barlage, M. Doczy, and R. Arghavani, “A 50 nm depleted-substrate CMOS transistor (DTS),” in IEDM Tech. Dig., 2001, pp. 621–623.
3. T. Ernst, D. Muteanu, S. Cristoloveanu, T. Ouisse, N. Hefyene, S. Horiguchi, Y. Ono, Y. Takahashi, and K. Murase, “Ultimately thin SOI MOSFETs: Special characteristics and mechanisms,” in Proc. IEEE Inte. SOI Conf., pp. 92–93, 2008.
4. J. P. Colinge, M. H. Gao, A. Romano-Rodriguez, H. Maes, and C. Claeys, “Silicon-on-insulator gate-all-around device,” in IEDM Tech. Dig., 1990, pp. 595–598.
5. H.-S. P. Wong, K. K. Chan, and Y. Taur, “Self-align (top and bottom) double-gate MOSFET with a 25 nm thick silicon channel,” in IEDM Tech. Dig., 1997, pp. 427–430.
6. J. P. Denton and G. W. Neudeck, “Fully depleted dual-gated thin-film SOI P-MOSFET’s fabricated in SOI islands with an isolated buried poly-silicon back gate,” IEEE Electron Device Lett., vol. 17, pp.509–511, Nov. 1996.
7. (Basic Book/Monograph Online Sources) J. K. Author. (year, month, day). Title (edition) [Type of medium]. Volume(issue). Available: http://www.(URL)
8. J. Jones. (1991, May 10). Networks (2nd ed.) [Online]. Available: http://www.atm.com
9. (Journal Online Sources style) K. Author. (year, month). Title. Journal [Type of medium]. Volume(issue), paging if given. Available: http://www.(URL)
10. R. J. Vidmar. (1992, August). On the use of atmospheric plasmas as electromagnetic reflectors. IEEE Trans. Plasma Sci. [Online]. 21(3). pp. 876—880. Available: http://www.halcyon.com/pub/journals/21ps03-vidmar

AUTHORS PROFILE

Er. Himani Malik, M.Tech in Electronics & Communication Engineering. She performed research work on Effect of Thickness and material on electronic properties of GAA-MuGFETs

Er. Amarjeet Kaur, M.Tech in Electronics & Communication Engineering. She performed research work on Electromagnetic Interaction Between Human Body & Hand-held RF devices like Mobile phones etc.

Er. Asha Lather, M.Tech in Electronics & Communication Engineering. She performed research work on Nano Technology.

Dr. V.K. Lamba, PHD in Nano Technology. He has done M.Tech in VLSI. He has been handling various Government projects based on Nano Technology. He has done deep research in Nano Technology.

Er. Bhupesh Kharb, M.Tech in Optical Engineering. He did research on Mobile & Home Appliances Control in secure Mode.