Transient and DC Analysis Microcontroller 8051 at 0.5 micro Technology for High Speed Applications

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Abstract— This paper presents the different types of analysis such as Transient and DC. The Schematic Design of 8051 microcontroller is based upon 0.5µm CMOS Technology using Tanner Tools and focused mainly on four components (SRAM, Interrupt Controller, ALU, CPU). An efficient and practical 8051 microcontroller has been proposed for solving the problem like to minimize the time delay during the operation and minimize the noise margin using different module level, by reducing the number of transistor in 8051 microcontroller its functioning speed goes rises, size & cost reduce.

Keywords: Microcontroller, Schematic, layout, CMOS,VLSI circuit.

I. INTRODUCTION

This paper is to introduce an 8-bit microcontroller called as 8051µC. The CPU can work on only 8 bit of data at a time. Data larger than 8 bit has to be broken into 8 bit pieces to be processed by the CPU. We are focusing mainly four part of 8051 microcontroller SRAM using 4 transistor, Interrupt Controller, ALU and CPU and also finding the AC and DC Analysis. 8051 Microcontroller has 128bytes of RAM, 4K bytes of on-chip ROM, two timers, one serial port, and four ports(each 8-bits wide) all on a single chip. At the time it was also referred to as a " System on a chip". It is noted that although there are different flavours of the 8051 in terms of speed and amount of on-chip ROM, they are all compatible with the original 8051 as far as the instructions are concerned. This means that if you write any program for one, it will run on any of them regardless of the manufacturer.

II. MODULES

i) Four Transistor Sram

The second driving force for SRAM technology is low power applications. In this case, SRAMs are used in most portable equipment because the DRAM refresh current is several orders of magnitude more than the low-power SRAM standby current[1]. For low-power SRAMs, access time is comparable to a standard DRAM[2]. Random Access Memory (RAM) is called volatile memory since turned off the power to the IC will result in the loss of the data. Sometimes RAM is also referred to as RAWM (read and write memory), in contrast to ROM, which cannot be written to data. There are three types of RAM as follows:

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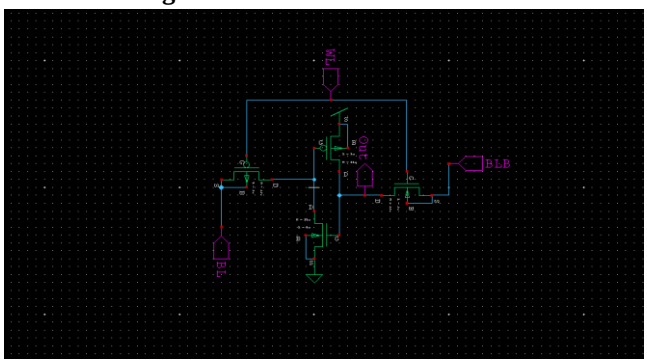
a) Static RAM(SRAM)
b) NV-RAM(nonvolatile RAM)
c) Dynamic RAM(DRAM)

Storage cells in SRAM memory are made of flip-flop and therefore do not require refreshing in order to keep their data. The use of 4-transistor cells plus the use of CMOS technology has given birth to a high-capacity SRAM.

Design Specification

1) Power Supply= 3.3V
2) Technology 0.5 Sub Micron
3) Logic Block= Array Specification.

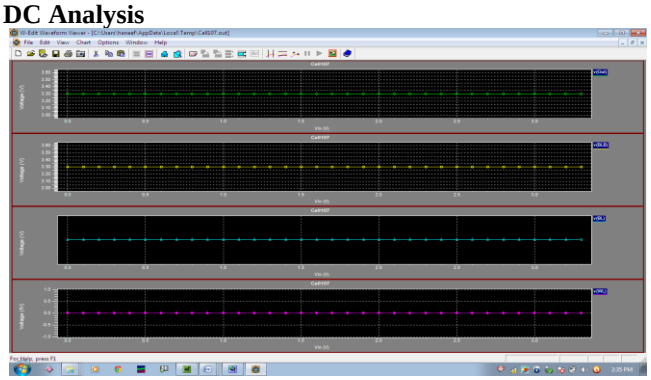
Schematic Diagram



Module

Model NMOS NMOS kp=4.5u vto=1v gamma=0.4
lambda=0.02 phi=0.6v
Model PMOS PMOS kp=3.6u vto=-1v gamma=0.4
lambda=0.02 phi=0.6v
Vdd Vdd Gnd 3.3v
Vin In Gnd Pulse(0 3.3v 0 1n 1n 10n 20n)
*.tran 1n 100n
.dc VIn 0 3.3v .1v
.Power Vdd 1n 100n
.print V(WL) V(BL) V(BLB) V(out).

DC Analysis



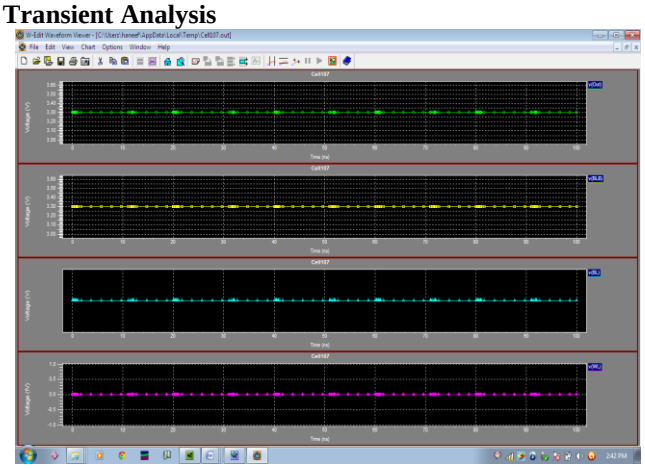
SPICE export from S-Edit 12.50 Mon Aug 13 19:48:50 2012

* Design: sram.sdb
* Cell: Cell107
* View: view0
* Export as: Top-level Cell
Root path: C:\Users\haneef\Desktop\4T-SRAM\sram.sdb

Simulation Settings - Parameters and SPICE Options

MMOSFET_N_1 N_1 Out Gnd Gnd NMOS L=0.5u W=0.5u AD=0.6p PD=3.5u AS=0.6p PS=3.5u
MMOSFET_N_2 Out WL BLB BLB NMOS L=0.5u W=0.5u AD=0.6p PD=3.5u AS=0.6p PS=3.5u
MMOSFET_P_1 BL WL N_1 BL PMOS L=0.5u W=1.5u AD=1.8p PD=5.5u AS=1.8p PS=5.5u
MMOSFET_P_2 Vdd N_1 Out Vdd PMOS L=0.5u W=1.5u AD=1.8p PD=5.5u AS=1.8p PS=5.5u

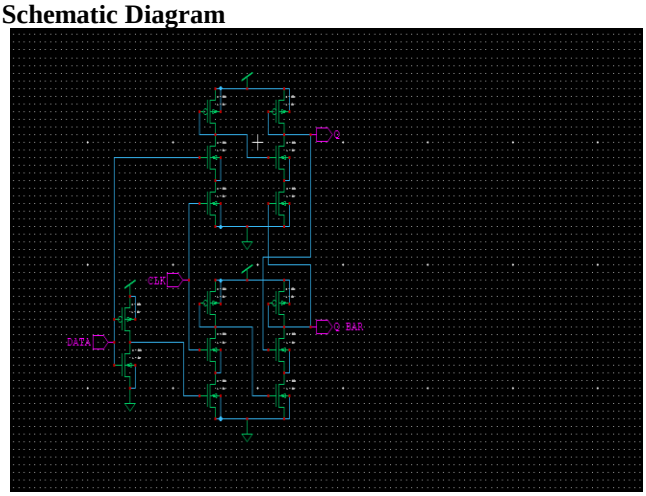
Transient Analysis



ii) INTERRUPT CONTROLLER

Whenever any device needs its service, the device notifies the microcontroller by sending it an interrupt signal. Upon receiving an interrupt signal, the microcontroller interrupts whatever it is doing and serves the device[4]. The program which is associated with the interrupt is called the interrupt service routine (ISR) or interrupt handler. D flip-flop store the current outputs between clock pulses.

Schematic Diagram

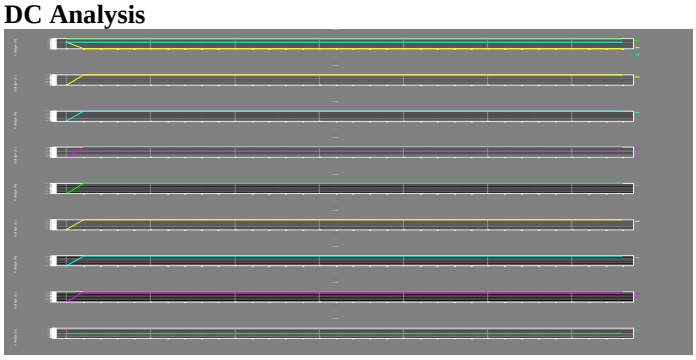


Module

.Model NMOS NMOS kp=4.5u vto=1v gamma=0.4 lambda=0.02 phi=0.6v

.Model PMOS PMOS kp=3.6u vto=-1v gamma=0.4 lambda=0.02 phi=0.6v
Vdd Vdd Gnd 3.3v
Vin In Gnd Pulse(0 3.3v 0 1n 1n 10n 20n)
*.tran 1n 100n
.dc VIn 0 3.3v .1v
.Power Vdd 1n 100n
.print V(DATA) V(CLK) V(Out).

DC Analysis

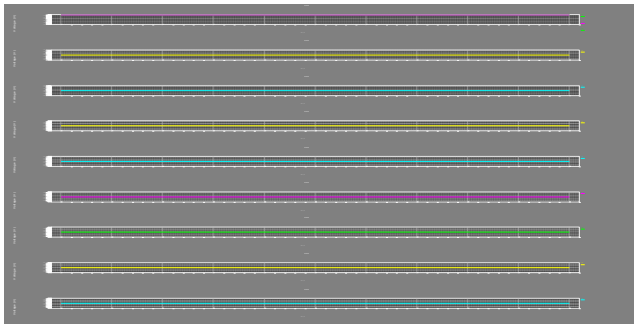


SPICE export from S-Edit 12.50 Mon Aug 13 19:42:16 2012
* Design: int.sdb
* Cell: 161
* View: view0
* Export as: Top-level Cell
Root path: C:\Users\haneef\Desktop\Interrupt\int.sdb
* Exclude global pins on subcircuits: no

Simulation Settings - Parameters and SPICE Options

MMOSFET_P_1 Vdd N_1 N_2 Gnd PMOS L=0.5u W=1.5u AD=1.8p PD=5.5u AS=1.8p PS=5.5u
MMOSFET_P_2 Vdd N_3 N_4 Gnd PMOS L=0.5u W=1.5u AD=1.8p PD=5.5u AS=1.8p PS=5.5u
MMOSFET_P_3 Vdd N_7 N_9 Gnd PMOS L=0.5u W=1.5u AD=1.8p PD=5.5u AS=1.8p PS=5.5u
MMOSFET_N_7 N_10 N_11 Gnd Gnd NMOS L=0.5u W=0.5u AD=0.6p PD=3.5u AS=0.6p PS=3.5u
MMOSFET_N_8 N_9 CLK N_10 N_10 NMOS L=0.5u W=0.5u AD=0.6p PD=3.5u AS=0.6p PS=3.5u
MMOSFET_N_9 N_11 DATA Gnd Gnd NMOS L=0.5u W=0.5u AD=0.6p PD=3.5u AS=0.6p PS=3.5u

Transient Analysis

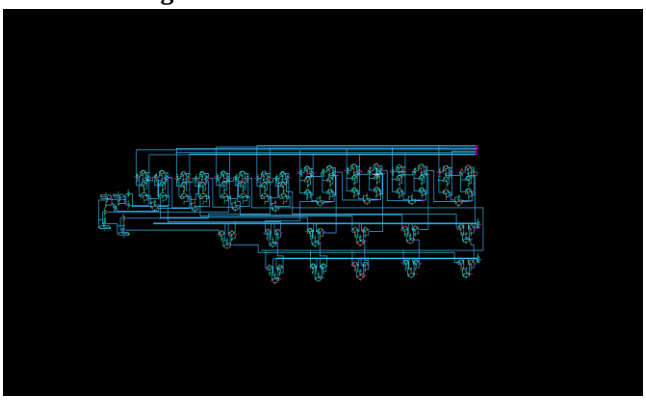


III. ARITHMATIC LOGIC UNIT (ALU)

A 8-bit ALU has been designed for 3V operation. The ALU can perform various arithmetic and logical operations**.** The basic blocks of a computer are central processing unit (CPU), memory unit, and input/output unit. CPU of the computer is basically the same as the brain of a human being. It contains all the registers, control unit and the arithmetic logic unit (ALU).

ALU considered as the most important subsystem in a digital computer. An arithmetic logic unit (ALU) is a digital circuit which performs arithmetic, logic and shift operations on two n-bit digital words[6][13]. Functionally, an ALU can be divided up into three circuits: the arithmetic circuit, the logic circuit and the shift circuit. Once verification was complete parasitics were extracted. To create a test for finding the maximum operating frequency a pseudo-random input stream was applied to each input of the ALU and observed the current during the input transition. Seeing that this is a CMOS design the current drawn by the ALU will approach zero between states if operating correctly. If the switching of the transistors takes longer than the period of the input then the ALU may give a erroneous output.

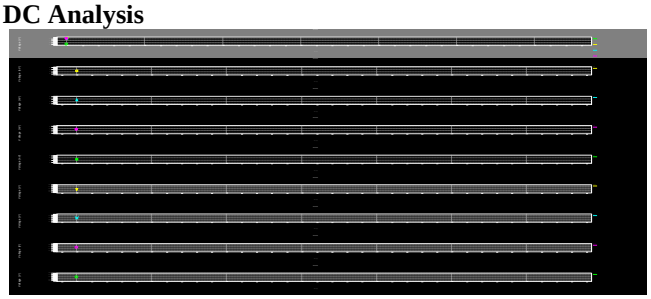
Schematic Diagram



Module

Model NMOS NMOS kp=4.5u vto=1v gamma=0.4
lambda=0.02 phi=0.6v
Model PMOS PMOS kp=3.6u vto=-1v gamma=0.4
lambda=0.02 phi=0.6v
Vdd Vdd Gnd 3.3v
Vin In Gnd Pulse(0 3.3v 0 1n 1n 10n 20n)
*.tran 1n 100n
.dc VIn 0 3.3v .1v
.Power Vdd 1n 100n
print V(I0) V(I1) V(I2) V(I3) V(I4) V(I5) V(I6) V(I7) V(Sel 0) V(Sel 1) V(A) V(B) V(C) V(D) V(E)

DC Analysis

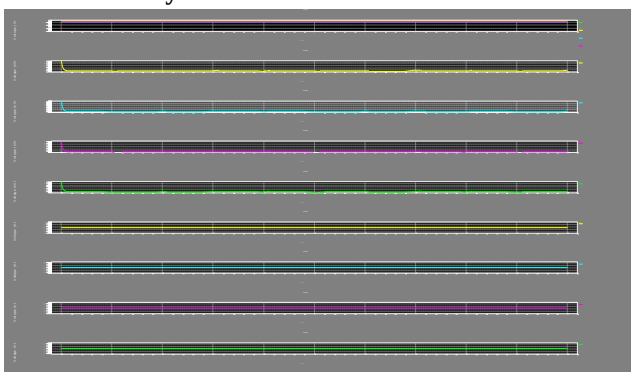


SPICE export from S-Edit 12.50 Mon Aug 13 20:03:41 2012
* Design: fnlalu.sdb
* Cell: Cell100
* View: view0
* Export as: Top-level Cell
Root path: C:\Users\haneef\Desktop\ALU\fnlalu.sdb

Simulation Settings - Parameters and SPICE Options

MMOSFET_**P**_257 N_186 N_154 Vdd Vdd PMOS L=0.5u W=1.5u AD=1.8p PD=5.5u AS=1.8p PS=5.5u
MMOSFET_N_65 Gnd N_232 N_233 N_234 PMOS L=0.5u W=1.5u AD=1.8p PD=5.5u AS=1.8p PS=5.5u
MMOSFET_P_258 N_184 N_185 N_303 N_303 PMOS L=0.5u W=1.5u AD=1.8p PD=5.5u AS=1.8p PS=5.5u
MMOSFET_N_66 N_240 I5 N_244 N_240 NMOS L=0.5u W=0.5u AD=0.6p PD=3.5u AS=0.6p PS=3.5u
MMOSFET_P_170 N_88 N_68 Vdd Vdd PMOS L=0.5u W=1.5u AD=1.8p PD=5.5u AS=1.8p PS=5.5u
MMOSFET_P_259 N_303 N_187 Vdd Vdd PMOS L=0.5u W=1.5u AD=1.8p PD=5.5u AS=1.8p PS=5.5u
MMOSFET_N_67 N_246 I5 Gnd Gnd NMOS L=0.5u W=0.5u AD=0.6p PD=3.5u AS=0.6p PS=3.5u
MMOSFET_P_171 N_279 N_90 Vdd Vdd PMOS L=0.5u W=1.5u AD=1.8p PD=5.5u AS=1.8p PS=5.5u
MMOSFET_N_68 Gnd I5 N_265 Gnd NMOS L=0.5u W=0.5u AD=0.6p PD=3.5u AS=0.6p PS=3.5u
MMOSFET_N_69 N_235 I5 N_265 N_265 NMOS L=0.5u W=0.5u AD=0.6p PD=3.5u AS=0.6p PS=3.5u

Transient Analysis



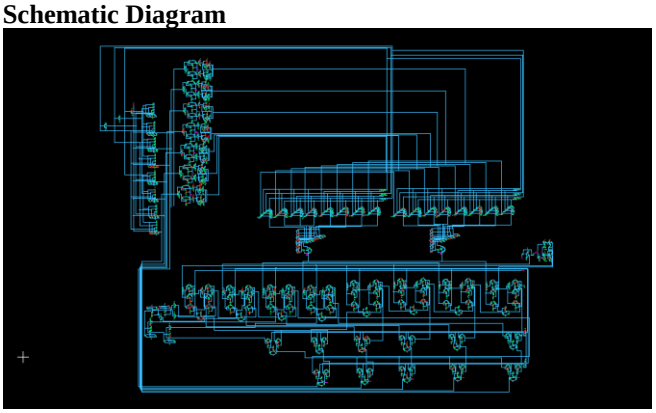
IV. CPU FOR 8051 MICROCONTROLLER

The part of the computer that performs the bulk of data processing operations is called the central processing unit and is referred to as the CPU[8]. The CPU is made up of three major parts, performs a variety of functions dictated by the type of instruction that is incorporated in the computer[10]. Computer architecture is sometimes defined as the computer strcture abd behavior as seen by the programmer that uses machine language instructions. One of the microcontroller features making it so powerful is an integrated UART, better known as a serial port. It is a full-duplex port, thus being able to transmit and receive data simultaneously and at different baud rates. Without it, serial data send and receive would be an enormously complicated part of the program in which the pin state is constantly changed and checked at regular intervals. When using UART, all the programmer has to do is to simply select serial port mode and baud rate. When it's done, serial data transmit is nothing but writing to the SBUF register, while data receive represents reading the same register. The microcontroller takes care of not making any error during data transmission. Serial port must be configured prior to being used.

In other words, it is necessary to determine how many bits is contained in one serial "word", baud rate and synchronization clock source. The whole process is in control of the bits of the SCON register (Serial Control).As seen, serial port mode is selected by combining the SM0 and SM2 bits:

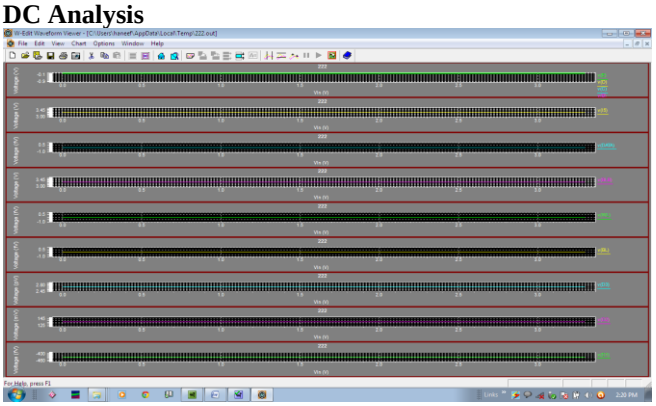
SM0	SM1	MODE	DESCRIPTION	BAUD RATE
0	0	0	8-bit Shift Register	1/12 the quartz frequency
0	1	1	8-bit UART	Determined by the timer 1
1	0	2	9-bit UART	1/32 the quartz frequency (1/64 the quartz frequency)
1	1	3	9-bit UART	Determined by the timer 1

Schematic Diagram



.Model NMOS NMOS kp=4.5u vto=1v gamma=0.4 lambda=0.02 phi=0.6v
.Model PMOS PMOS kp=3.6u vto=-1v gamma=0.4 lambda=0.02 phi=0.6v
Vdd Vdd Gnd 3.3v
Vin In Gnd Pulse(0 3.3v 0 1n 1n 10n 20n)
.tran 1n 100n
*.dc VIn 0 3.3v .1v
.Power Vdd 1n 100n
.print V(DATA) V(CLK) V(BL) V(BLB) V(WL) V(Sel 0) V(Sel 1) V(I0) V(I1) V(I2) V(I3) V(I4) V(I5) V(I6) V(I7) V(A) V(B) V(C) V(D) V(E)

DC Analysis

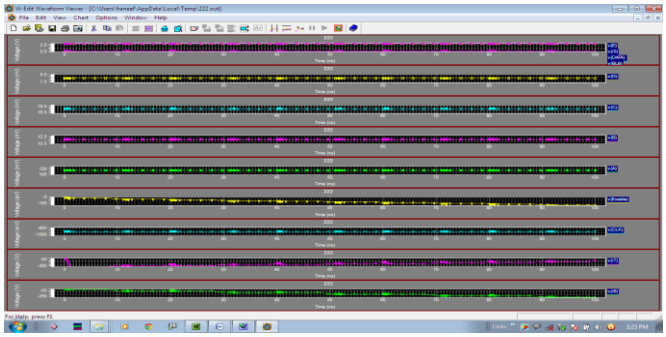


*** SPICE export from S-Edit** 12.50 Wed Jun 27 14:17:24 2012
* Design: design
* Cell: 222
* View: view0
* Export as: Top-level Cell
* Root path: C:\Users\haneef\Desktop\cpu D\design
* Exclude global pins on subcircuits: no

Simulation Settings - Parameters and SPICE Options

MMOSFET_N_225 N_328 N_417 N_410 N_410 NMOS L=0.5u W=0.5u AD=0.6p PD=3.5u AS=0.6p PS=3.5u
MMOSFET_N_226 N_415 D2 Gnd Gnd NMOS L=0.5u W=0.5u AD=0.6p PD=3.5u AS=0.6p PS=3.5u
MMOSFET_N_227 B D1 N_416 N_416 NMOS L=0.5u W=0.5u AD=0.6p PD=3.5u AS=0.6p PS=3.5u
MMOSFET_N_228 C D3 Gnd Gnd NMOS L=0.5u W=0.5u AD=0.6p PD=3.5u AS=0.6p PS=3.5u
MMOSFET_N_229 C N_415 N_414 N_414 NMOS L=0.5u W=0.5u AD=0.6p PD=3.5u AS=0.6p PS=3.5u
MMOSFET_N_230 C Enable N_427 N_427 NMOS L=0.5u W=0.5u AD=0.6p PD=3.5u AS=0.6p PS=3.5u
MMOSFET_N_231 C D1 N_427 N_427 NMOS L=0.5u W=0.5u AD=0.6p PD=3.5u AS=0.6p PS=3.5u

Transient Analysis



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Publication Year: 2003 , Page(s): 551 - 554 Cited by: 3 ;IEEE Journals & Magazines .
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13. Application Specific Low Power ALU Design ;Yu Zhou; Hui Guo Embedded and Ubiquitous Computing, 2008. EUC '08. IEEE/IFIP International Conference on Volume: 1 Digital Object Identifier: 10.1109/EUC.2008.81 Publication Year: 2008 , Page(s): 214 - 220 Cited by: 1; IEEE Conference Publications.