Low Power 128-Point Pipeline FFT Processor using Mixed Radix 4/2 for MIMO OFDM Systems

K. Umapathy, D. Rajaveerappa

Abstract - In this paper, an area and power efficient 128- point pipeline FFT processor is proposed for MIMO - OFDM systems based on mixed-radix 4/2 multipath delay commutator architecture (R2MDC) in terms of lower complexity and higher memory utilization. A conventional mixed radix 4/2 multipath delay commutator FFT processor will increase the hardware capacity and can be used to change the order of the input sequences. The processor is characterized with capable power-consumption for different FFT/IFFT sizes. Unlike the general mixed radix-based architectures which use a larger internal word length to achieve a high signal to noise ratio (SNR), our processor keeps the internal word length the same as the word length of the input data while adopting the block-floating point (BFP) approach to maintain the SNR. The proposed FFT processor uses different commutators which can be used to decrease the delay elements and integrate with other MIMO-OFDM processing blocks. The designed 128-point FFT processor provides 49% reduction in count of logic gates and 67% in power dissipation on 90-nm CMOS technology.

Index Terms: ***FFT, MIMO, OFDM, MDCA.***

I. INTRODUCTION

The Fast Fourier transformation (FFT) and its inverse (IFFT) is one of the indispensible operations in the field of Digital signal processing. It is widely used in various areas such as Telecommunications, Image processing, Medical electronics, Seismic processing, etc. Recently, the FFT is used as one of the important component in OFDM-based wideband communication systems. The integration of the Multiple-input multiple-output (MIMO) signal processing with orthogonal frequency division multiplexing is a definite solution for improving the data rates of the next generation wireless communication systems employing the principle of frequency-selective fading. In this paper, the design of 128-point FFT processor which computes a 128 point FFT including I/O within a time period of 40 µs.

II. TYPES OF FFT ARCHITECTURES

Generally the FFT processors can be divided into three main categories-

I. Pipeline FFTs. They employ concurrent or parallel processing of various stages to achieve high performance.
II. Column FFTs. Each and every stage in the FFT is computed with a set of processing elements and the output is given as feedback to the same processing elements for the computing the next stage.
III. Fully parallel FFTs. The signal-flow graph operations are mapped to a hardware structure in an isomorphic manner. The hardware implementations are intensive with respect to current technology and not suitable for large FFTs.

III. DESIGN ISSUES OF FFT PROCESSOR FOR MIMO OFDM SYSTEMS

A block diagram of the receiver employing IEEE 802.11n standard is shown in Figure 1. It contains four RFs, four analog-to-digital converters (ADCs), four FFTs, a MIMO equalizer, four De-Qam and De-interleaver, a De-spatial parser, a De-puncturer, a Channel decoder, a Synchronization block, and a Channel estimation block. Based upon the on the desired data rate, the modulation scheme can be Binary Phase shift keying (BPSK), Quaternary Phase shift keying (QPSK), or Quadrature Amplitude modulation (QAM) with 1–6 bits. The encoding rates in this specification are 1/2, 2/3, 3/4, or 7/8. The number of spatial sequences is supported by 1, 2, 3, or 4. The guard interval period is either 400 ns or 800 ns. The bandwidth of the transmitted signal is either 20 or 40 MHz. The FFT size is 64 points or 128 point and the FFT processor has to compute either 128 points or 64 points with simultaneous 1–4 data sequences within 3.6 or 4 seconds. In the last three decades, various FFT architectures such as single-memory architecture, dual-memory architecture, pipelined architecture, array architecture, and cached-memory architecture, have been proposed. However to deal with multiple data sequences the FFT architectures are employed.

Generally multiple FFT processors are integrated to deal with multiple data sequences in a MIMO OFDM system as shown in Figure 1 and they cause a large increase in the hardware complexity and power consumption when compared a single FFT processor. A good FFT processor can provide a high throughput rate and can also deal with multiple data sequences in an effective manner for MIMO OFDM applications. In this context, the pipelined FFT architecture must be the best solution for the high throughput rate applications with reasonable hardware cost.

This pipelined architecture divides into the two following categories. One is multipath delay commutator (MDC) and the other is single-path delay feedback (SDF). Generally the MDC style can provide higher throughput rate by using multiple data paths, while the SDF style requires less memory and hardware complexity.

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In order to save power dissipation, higher radix FFT algorithm can be used to reduce the number of complex multiplications. The Three-step radix-8 FFT algorithm is employed in our design to save complex multiplications. Since the 128-point FFT is not a power of 8, the mixed-radix FFT algorithm combining two different styles is required. The Mixed-radix Multipath delay feedback (MRMDF) FFT architecture can provide higher throughput rate with minimal hardware cost by integrating the styles of MDC and SDF. The main Objective of this paper is to design a pipeline unfolding MRMDF structure based 128-point FFT processor using Mixed Radix 4/2 which can deal with 1–4 simultaneous data sequences for MIMO OFDM applications thus saving a lot of hardware complexity when compared to the traditional approach.

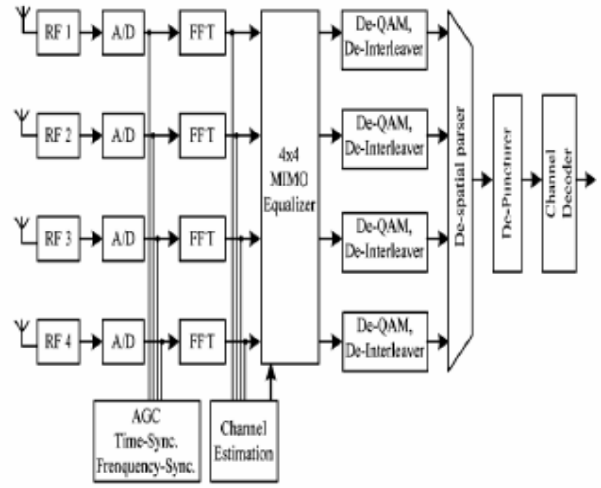

Figure 1. Block Diagram of Receiver using IEEE 802.11n Standards showing the Data Sequences.

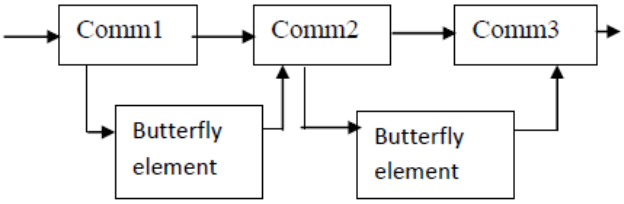

Figure 2. Signal Flow Graph (SFG) of the Proposed Architecture.

IV. PROPOSED FFT ARCHITECTURE

The proposed FFT architecture combining the features of the SDF and MDC styles consists of Module 1, Module 2, Module 3, Module 4 conjugate blocks, a division block, and multiplexers. The key features of the proposed FFT architecture are as follows. First, 128/64-point FFT processor with 1–4 simultaneous data sequences can be operated in our design. Second, the proposed architecture can provide several throughput rates thus meeting the requirements of IEEE 802.11n standards. Third, minimum memory is required by employing the delay feedback scheme to reorder the input data and the intermediate results of each module. The Scheduling approach and the specified constant multipliers can be employed to reduce the hardware complexity of the complex multipliers. Hence the proposed FFT processor has less hardware complexity when compared with the traditional approach using multiple FFT processors. Finally a higher radix FFT algorithm can be implemented to save power dissipation irrespective of the operations of either 64-point FFT or 128-point FFT.

The input data sequences and output data sequences has the specified order in the proposed FFT architecture. Since the order of input sequences, shown in Figure 1 is same as that of the data sequences from the ADC, no extra memory is required to reorder these input sequences before they are loaded into the FFT processor. In general, the order of the output sequences is different from that of the input sequences in the pipelined FFT architecture. Generally the order of the output sequences depends on the FFT algorithm, the number of data paths and the FFT architecture. In our design, the order of four output sequences is the repetition of the order of input sequences as shown in Figure 1.

The operation of 128/64-point FFT/IFFT is controlled by the control signal mode. If the operation of 64-point FFT is performed, then calculated data from Module 1 will skip Module 2 and go into Module 3 directly as shown in figure 3. The function of Module 1 is to reorder the input data sequences from the four data paths into a specific order to implement the operation of FFT/IFFT with multiple data sequences in an efficient manner. Module 2 is to implement a radix-2 FFT algorithm, corresponding to the first stage of SFG, as shown in Figure 2. Module 3 and Module 4 are meant for implementing three-step radix-8 FFT algorithm, corresponding to the second and third stages of the SFG, as displayed in Figure 2. Two different schemes (SDF and MDC) are followed in Module 3 and Module 4 to implement three-step radix-8 FFT algorithm to minimize the memory requirement and to ensure the correction of the FFT output data.

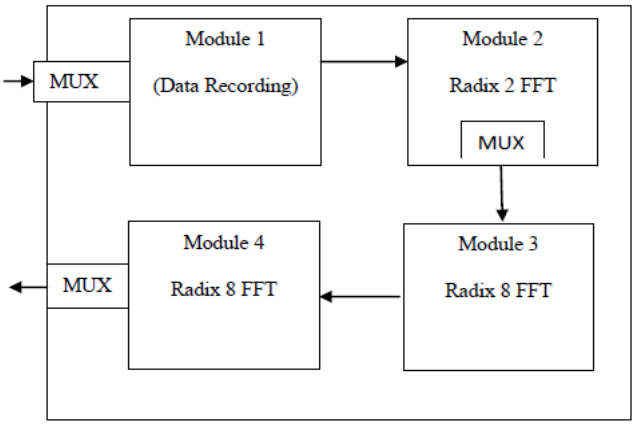

Figure 3. The Proposed 128-point FFT Architecture

V. PERFORMANCE ANALYSIS

In IEEE 802.11n standards, the 128-point and 64-point FFT/IFFT are used for the bandwidth of 40 and 20 MHz respectively. Generally 1–4 simultaneous data sequences must be supported in this specification according to the number of antennas used. Eight operation modes of the FFT/ IFFT processor are required in IEEE 802.11n standards. Two operation clock rates of our scheme, 40 and 20 MHz, are required for the operation of 128-point and 64-point FFT/IFFT respectively. The effective throughput rates of our design depend on the number of data sequences and can be calculated as-

Effective Throughput Rate = 4R * Operation Ratio. Where the operation ratio is defined as the number of data sequences divided by 4. Generally, if the number of data sequences is less than four, the number of operations is less than four in each group. So the effective throughput rate will be less than number of data sequences and only three operations are required in each group. So the operation ratio is 3/4 and the effective throughput rate is equivalent.

VI. SIMULATION AND RESULTS

Initially the 128/64-point selected FFT/IFFT algorithm is coded by MATLAB language. After the selected FFT/IFFT algorithm is valid, the architecture of the processor was modeled in Verilog language and functionally verified using Verilog-XL simulator. The word length of our proposed FFT processor is a parameter determined by the customers. Based on the simulation results, the word length of the proposed FFT/IFFT is determined to be 12 bits in both real and imaginary parts thus meeting the IEEE 802.11n system requirements. According to the operation clock rate listed in Table 1, two clock rates, 40 and 20 MHz, are used for the operation of 128-point and 64-point FFT respectively. Moreover the input sequences are in the specified order when loaded into the proposed FFT processor, as shown in Figure 3. At the operation clock rate of 40 MHz, the computation of 128-point FFT/IFFT with four data sequences requires 3.2 s, i.e., 128 cycles. Further, the computation of 64-point FFT/IFFT with four simultaneously data sequences needs 3.2 s at the operation clock rate of 20 MHz.

TABLE 1. Performance of Operation Modes in our proposed 128-point FFT Architecture

Operation mode		Operation clock rate(R)	Effective throughput
No. Of FFT point	No. of input sequence		
128	4	40MHz	4R
128	3	40MHz	3R
128	2	40MHz	2R
128	1	40MHz	1R

VII. CONCLUSION

A pipeline 128/64 -point FFT/IFFT processor using Mixed Radix 4/2 algorithm for a MIMO OFDM system has been proposed. Based on the concept of data reordering and grouping, the processor can provide different throughput rates to deal with 1–4 simultaneous data sequences more efficiently. Further, the hardware costs of memory and complex multiplier can be saved by adopting delay feedback and data scheduling approaches. Moreover the number of complex multiplications can be reduced effectively by using higher radix FFT algorithm. The proposed FFT/IFFT processor was designed in a 0.13- m 1P8M CMOS process which can meet IEEE 802.11n standards at the operation clock rate of 40 MHz

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