New Ternary Logic Subtractor using Carbon Nanotube Field-Effect Transistors

Tahere Panahi, Saideh Naderi, Tahere Heidari, Elham Zeidabadi nejad , Peiman Keshavarzian

Abstract— In this paper, we present a new Ternary logic Subtractor (TLS) that is implemented by CNTFET. In addition, we investigate the design of two Novel subtractors based on the proposed TLS. Ternary results are better than the Binary ones. Results show large decrements in delay time. Further, the second presented circuit with its Simulation results has demonstrated significant development in speed, area and power consumption. In the past extensive design techniques, Multiple-Valued Logic (MVL) circuits (especially ternary logic inverters) have been proposed by CMOS Technology. Here, the new TLS based on CNTFETs is presented, and wide simulation results have been done by HSPICE.

Index Terms— CNTFET, Subtractor, Multiple-Valued Logic.

I. INTRODUCTION

By adding a new logic value to the Binary logic, we attain Ternary logic, for designing a device to achieve lower power consumption and area saving on the chip. By using ternary logic, we have this horizon to reach faster speed and simplicity in designing.

For the last couple of decades, multiple-valued logic (MVL) has attracted considerable consideration, especially among circuit and system designers [14].

MVL changes the traditional Boolean classification of variables by means of restrictedly and also unlimitedly many values such as ternary logic [15] or fuzzy [16]. Ternary logic has attracted due to its potential benefits over binary logic for the design of digital systems. For instance, it is possible for ternary logic to attain simplicity and saving sin energy in digital design since the logic reduces the complexity of interconnects and also reduce the number of the transistors.

Chip area and power consumption can be decreased more than 50 percent by using MVL completion for a signed 32-bits multiplier compared to its fastest binary corresponding item [17]. Two types of MVL circuits based on MOS technology existed in [17], the current-mode MVL circuits and the voltage mode MVL circuits. Voltage-mode MVL circuits have been obtained in multi threshold CMOS [20].

In addition, serial and Serial-parallel mathematic operations can be performed faster if it is to be used in the ternary logic [1]. Nowadays, new research is being done to replace the silicon technology with Nano technology. For example, CNTFETs are most hopeful parts because of their single one dimensional band structure which can decline backscattering[2-4]. The single-wall carbon nanotube (SWCNT) is one dimensional conductor which can be either metallic or semiconducting based on carbon atoms arrangement [5]. The semiconducting carbon nanotubes display features for creation field effect transistors and logic gates [6].Carbon nanotubes (CNTs) are formed by rolling sheets of graphite. They have been expected for Nano scale electronic devices [1-7-10-19]. Several studies have shown that CNTFETs load resistive based ternary logic can be used to create a variety of electronic functions, such as non-volatile memories[16] and logic gates (Nor, inverter, etc.) [12-13]. Principally, there are two ways to create devices by CNTFETs. The first way is carried out by transferring the logic function directly to the instance technology, i.e. replacing the MOSFET with CNTFET. The second way is done by CNTFET technology characteristics[17]. Because of the limitation on MOSFET technology, such as physical limitation and power consumption in contrast to high speed and low power consumption devices demands, it is predicted that they are facing the dead end [21].The multi-threshold CMOS design is based on transistor body effects that apply different bias voltages to the bulk terminal of the transistors. CNTFET threshold voltage is inversely related to the diameter of the CNT [18] .Here, a novel multi-valued logic design based on multi-threshold CNTFETs is presented and accordingly contrasted with existing MVL designs based on single threshold CNTFETs. Remaining of this paper is organized as follow, and the wide-ranging HSPICE simulation results have displayed substantial advantages in terms of power consumption and rate.

II. REVIEW OF TERNARY LOGIC

In the ternary logic, we have three logical values that show the third value compared to binary logic.

We use 0, 1, and 2 respectively for false, undefined, and true representation.

Where F(x) =(x1,x2,..,xn) we have {0,1,2} as a logical function, if X={x1,x2,…xn}, the main operations of Ternary logic will be implemented as below equivalent:

If xi, xj· {0,1,2}

Then

Xi+Xj=max {Xi,Xj} (1)

Xi.Xj=min {Xi,Xj}

$(X\_i)^{-}=2-Xi$

We assume symbols as following:

+, . , - are correspondingly for OR, AND, NOT [22].

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Table 1. Logic Symbols

Voltage level	Logic value
0	0
½V_{dd}	1
V_{dd}	2

The most important and main part of logic design systems is ternary inverter which is an operator with the following standard while describing X as an input and Y0,Y1,Y2 as three possible outputs, such as :

$$Y(STI) = C_1(x) = \overline{X_1} = 2 - x \quad (2)$$

$$Y(NTI) = C2(x) \begin{cases} 2 \text{ if } x = 0 \\ 0 \text{ if } x \neq 0 \end{cases} \quad (3)$$

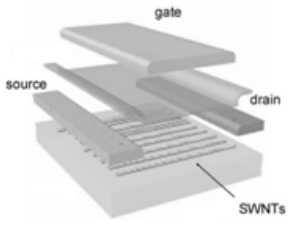
$$PTI) = C3(x) = \begin{cases} 2 \text{ if } x \neq 2 \\ 0 \text{ if } x = 2 \end{cases} \quad (4)$$

For that reason, the achievement of a ternary inverter would involve three inverters, a standard ternary inverter (STI), a positive ternary inverter (PTI), and a negative ternary inverter (NTI), if y0, y1, and y2in Equation (2) are the outputs [1]. The truth table of the three ternary inverters is shown in Table 2 (Stanford University CNFET Model website).

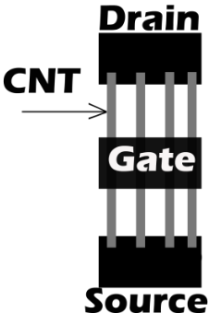
III. CARBON NANO TUBE FIELD EFFECT TRANSISTORS

Carbon nanotube field effect transistors (CNTFETs) used semiconducting single-wall CNTs to collect electronic devices close to MOSFETs [24]. A single-wall carbon nanotube (SWCNT) contains only one cylinder; the simple mechanized process of this device makes it very assuring for use as a transistor in place of today's MOSFET. For instance, a SWCNT can act as a conductor or a semiconductor, depending on the angle of the atom arrangement alongside the tube. This is submitted to as the chirality vector and is corresponding to the integer pair (n,m). A simple technique to determine if a carbon nanotube is metallic or semiconducting is regard to its indices (n, m). The nanotube is metallic if n=m or n-m=3i,i is an integer. Otherwise, the tube is semiconducting. We can calculate the diameter of the CNT based on : [23-25]

$$DCNT = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + m^2 + nm} \quad (5)$$



(a)



(b)

Fig. 1.diagram of a carbon nanotube transistor

Figure 1. (a) side vision; (b) top vision.

While a0 = 0.142nm is the inter-atomic distance among each carbon atom and its around, Figure 1 shows the schematic diagram of a CNTFET [23-25]. Similar to the traditional silicon device, the CNTFET has four terminals as well. As shown in Figure 1, undoped semiconducting nanotubes are located under the gate as channel area [2]. As the gate potential gets higher, the device is electro statically turned ON or OFF through the gate.

The current-voltage (I-V) characteristics of the CNTFET are comparable to the MOSFET's. The threshold voltage is defined as the voltage required turning on the transistor. The threshold voltage of the intrinsic CNT channel can be approximated to the first order as the ½ band gap, which is an inverse function of the diameter [24-25] , i.e.

$$Vth \approx \frac{Eg}{2e} = \frac{\sqrt{3}}{3}\frac{aV\pi}{eD_{CNT}} \quad (6)$$

Wherever a = 2.49 Å is the carbon to carbon atom space, V_π= 3.033e V is the carbon π-π bond energy in the tight bonding model, e is the element electron charge, and DCNT is the CNT diameter. If CNT chirality is (19, 0) and the diameter is 1.487 then according to equation (4) the voltage is 0.293 V. As the chirality vector changes, the threshold voltage of the CNTFET will also modify. For instance, the threshold voltage of a CNTFET using (13, 0) CNTs is 0.428 V though the threshold voltage of a (19, 0) CNTFET is 0.293V.

CNTFETs provide a single option to manage threshold voltage by changing the chirality vector or the diameter of the CNT [17]. In addition, they have reported advances on processes for manufacturing well-controlled CNTs [9].

Therefore, here we use a multi-diameter CNTFET-based design for the ternary inverter implementations, for showing the TLS. According to figure.2, inverses of INA and INB have done by STI circuit.

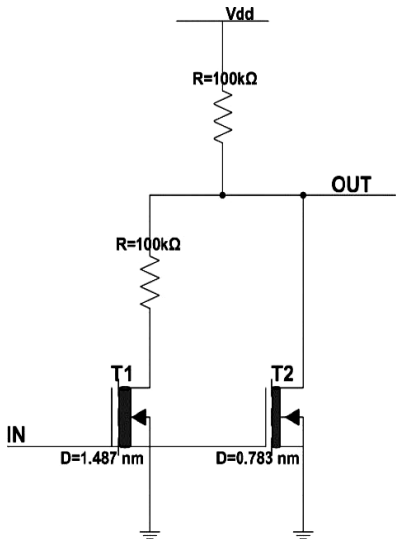


Fig.2. Schematic diagram of CNTFET-based STI proposed in [17]

A. Existing Design

A CNTFET-based ternary logical design has been planning [17]. It uses dual-diameter CNTFETs and resistors.Figure2 shows the schematic diagram of the STI by means of a power supply voltage of 0.9 V (as the default value of the CNTFET [24]. Consequently, logic 0 matches to a voltage value fewer than 0.3 V, logic1 corresponds to a voltage value among 0.3 and 0.6 V. Moreover, logic 2 matches to a voltage value larger than 0.6 V. InFigure2, transistors (T1) and (T2) have a diameter d1 = 1.487 nm,d2 = 0.783 nm respectively.

As a result, the two transistors have threshold voltages of Vth1 =290 mV and Vth2 = 550 mV, consecutively. When input voltage is poorer than 300 mV, both T1 and T2 are OFF, and output voltage will be 900 mV. While the input voltage raises further than300 mV, T1 is ON and T2 is OFF, and the output voltage is near to Vdd/2 till the input voltage reaches toVth2. As soon as the input voltage overVth2, bothT1 and T2 will be ON and the output voltage is pulled to near zero. Selecting CNTFETs by suitable threshold voltages, a ternary logical inverter design will be obtained. Nevertheless, according to Figure2, two large resistors (typically 100 MΩ or larger) are needed to plan the design of [17]. However, their values are too great to be integrated into CNTFET technology. In this paper we use two pass gates transistor's in order to resolve this problem

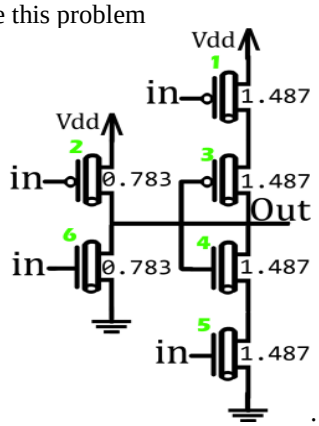


Fig. 3. Proposed CNTFET-based STI designing [17]

B. Proposed CNTFET-based design

The Inverse of INA and INB by STI circuit is shown in figure 3. In this inverter T1 controlled Vdd whereas logic "0" is requisite. Therefore, the power consumption will be lower than the previous STI (figure 2).

IV. SUBTRACTOR BASED ON TERNARY INVERTOR DESIGN BY 30 CNT

Truth table 3.Ternary subtractor Table

A / B	0	1	2
0	0	1	2
1	1	0	1
2	2	1	0

Truth table shows the performance between the Subtractor circuits. When the difference of two inputs is a logical unit, the logic of output will be '1'.

For instance, in the second step (10-20ns) that input A is equal to logic '1' and input B is equal to logic 2, the signal output is logic '1'.

While difference of two inputs is 2 logical unit, the circuit output is equal to logic '2', and it only takes two steps in (20-30ns) and (60-70ns).Finally, when both inputs are equal, the output logic circuit will be 0.

The input signal has the quality to create all of the Ternary logical states.

Truth table3 shows the functionality of the Subtractor value in 0.9 voltage source and at room temperature.

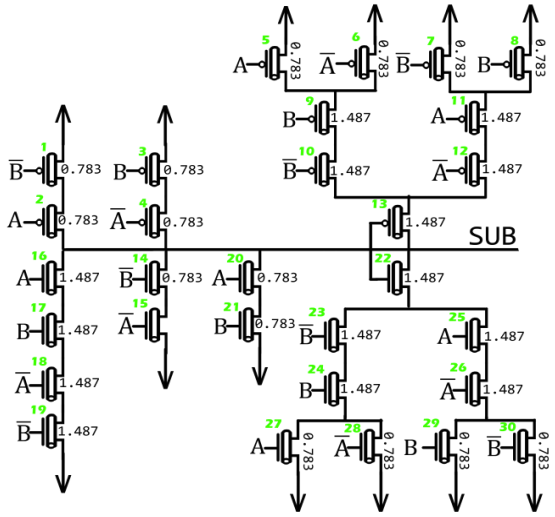


Fig. 4. Schematic of first design

Figure 4 shows subdivided circuit for implementation of ternary logic function by CNTFET, first is related to state zero, second to state one and finally third which contains PCNTFET will produce both states one and two according to truth Table.

Figure 4 demonstrates that, Where A and B are equal to logic zero; both T14, T15 will be ON and the output will be zero. By changing B to statlogic'1';T9,T5,T10 and T23,T24,T28 will be ON The output is equal to1/2Vdd; bear in mind T13 and T22 acting as voltage distributor. By changing B to logic (state) '2', it makes T1, T2 ON and the output will be Vdd. If A equal to logic state '1' and B equal to logic'0' ; T8,T11,T12 will be ON while T25,T26,T30 are ON in this input state, therefor through voltage distributor the output will be 1.

If A and B are equal to '1', T16, T17, T18, T19Will be ON and the output has sate logic 0.

If A equal to logic state '1' and b equal to logic'2'; T25, T26, T29 will be ON while T7,T1,T12 are ON in this input state, therefore through voltage distributor the output will be '1'.

If A equal to logic state '2' and B equal to '0', T3, T4 are ON, which impose the output to Vdd Where A equal to logic '2' and B equal to logic'1', T6, T9, T10and T23, T24, T27are ON in this input state, therefore through voltage distributor the output will be 1/2Vdd.

If both A and B are equal to logic'2'; T20, T21 will be ON and we have logic zero in the output.

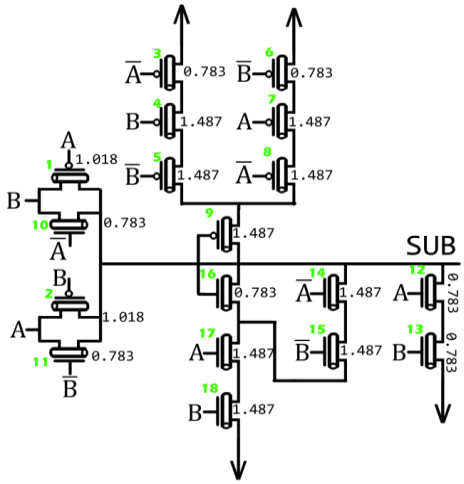


Fig. 5. Schematic of second design proposed Ternary subtractor based CNTFET

V. SUBTRACTOR VALUE BASED ON TERNARY INVERTOR DESIGN BY 30 CNT BY 18 CNT

First:

If B is equal to logic zero, (T11, T2) will be ON and A will be in the Output. On the other side, if A='0' (T1, T10) is ON, B will be in the Output.

Second:

In this state that we have A=B=1/2 Vdd, the output will be controlled via T11, T15, T17, T18.Thatonly in this situation, all of these four transistors will be ON.

Third:

If A=B =Vdd then T12 and T13 will be ON and output will be pulled down to logical '0'.

In the other conditions the output should have half of Vdd . According to truth table , if 'A' is equal to Vdd and 'B' equal to ½ Vdd and vice versa output has state logic '1' (regardless of second and third conditions) the first state is controlled via (T3,T4,T5) and the second state is controlled via (T6, T7, T8); this situation is provided by adding two transistors (T17, T18) to the design. Two transistors T9 and T16 are employed as output voltage distributors.

VI. SIMULATION RESULTS

A. Simulation result for TLS By 18 transistor

A wide simulation on second Subtractor with 6 various voltage sources has been performed. According to figure. 6 (a),(b) by increasing supply voltage, increasing power consumption and reduced delay, the minimum PDP will be achieved in 1V. Figure. 6, shows transient response of inputs and outputs in Vdd=0.9 and in room temperature.

B. Simulation result for TLS By 30 Transistor

The Simulation which has been done in room temperature at 27˚C and shows a variety of source voltages on delay and power consumption.

Results show that the first TLS is the same as second TLS, by increasing voltage. Accordingly, the power will be increasing versus decreasing delay.

According to result of the PDP, we observed that the minimum PDP of first TLS is achieved at Vdd=0.7V.

Figure .8 illustrates one output and two inputs denoted by A and B.

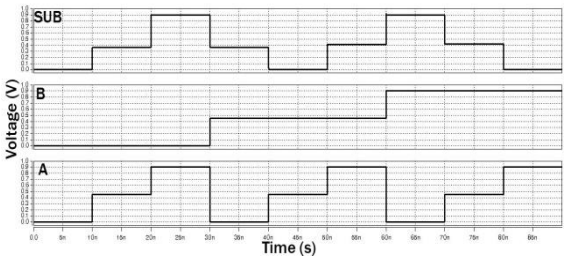


Fig. 6.transient response of first TLS

C. General conclusions

To compare the first and second designs, worse delay, power dissipation and PDP (power-delay product)of our two novel designs are evaluated. Due to making trade-off between the delay and the power consumption, we calculated PDP which is product delay and power, Table4.

The PDP is an important parameter and it is used in measuring and comparing circuits. We have done simulations at different temperatures and voltage by HSPISE. It has been shown in figure (7),(8) that the second design has less power and delay compared to first design. Therefore, the PDP of first design is higher than the second design. Transistor count is an important property in this paper thus we proposed the second design.

Table 4. Simulation results

Design	Delay	Power	PDP
CNTFET with 18 transistor	5.9113E-12	3.5116E-06	20.75812E-18
CNTFET with 30 transistor	17.879E-12	3.6109E-06	64.5593E-18

As the CNTFET transistors threshold voltage is depended on diameter of nanotubes, therefore by changing the CNTFET chirality, circuits can be designed with different supply voltages. Here, we have performed simulation for 5 different Voltages and 3 various temperature for two proposed designs.

Simulation results are shown in figure (7) and (8).

Results have shown that the TLS by second design Subtractor has better performance in terms of PDP than the previous designs and we observe reduction in transistors as well. Changes in voltage and temperature are significant issues in the design of digital circuits. Systematic changes in the supply voltage and temperature is a major challenge in the electronic devices in terms of energy and delay. To determine the effect of temperature and voltage of these designs, simulation has been done by HSPICE.

The simulations for five different voltages (0.7, 0.8, 0.9, 1.0, 1.2, 1.4V)in addition to 3 various temperatures(0, 27, 100 ˚C) have been executed.

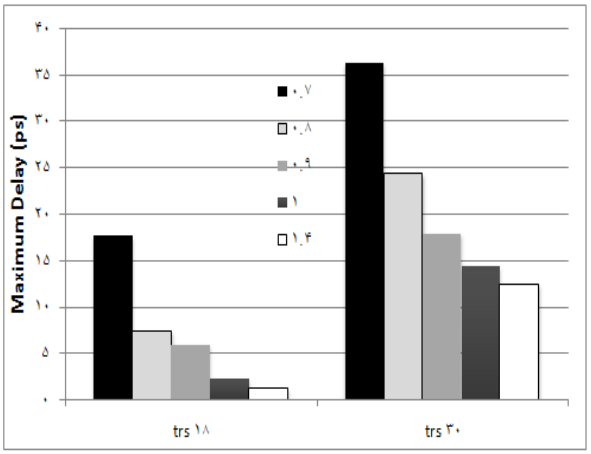
Figure.7 (a) and (b)have shown power and delay for five different voltages. When the voltage increases, the simulation results indicate that the delay will be decreased versus increasing power consumption. In normal situation at 0.9V in second design, power is higher than its counterpart.

Figure.7(c) and 7 (c) have shown bar graph of the power delay product (PDP) with different supply voltages and temperatures for two proposed design.

We have the best PDP for first and second designs in 1.0V and 0.7V, respectively.

In the worst case (1.4V), that is the second TLS, we have approximately 400% improvements (compared to the initial design) in terms of PDP and number of the transistors.

The results indicate that delay of the second TLS for a given voltage transistor is lower than its counterpart.



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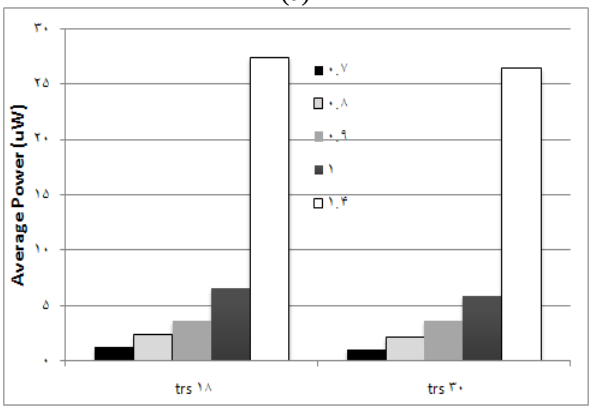

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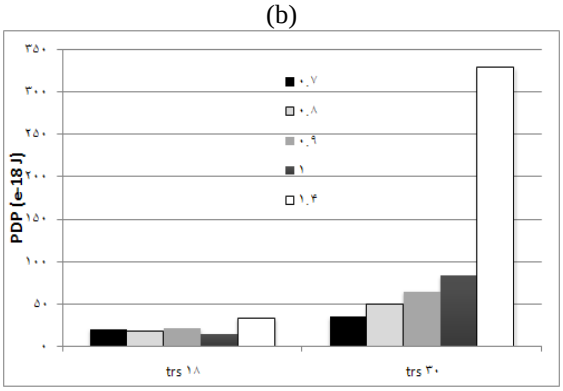


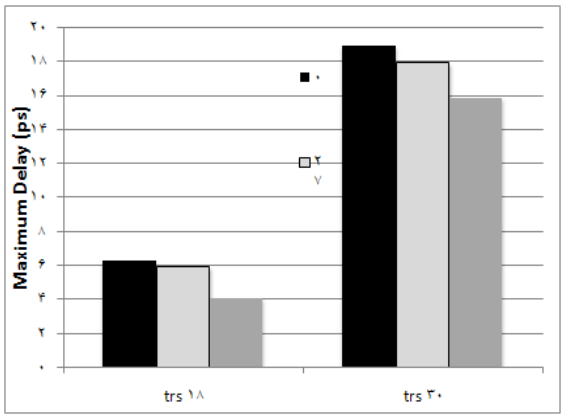
(c)

Fig. 7. (a) Transient average power of CNTFET. (b) Transient worse delay of CNTFET.(c)Power Delay Product (PDP) of two Subtractors with different Voltage.

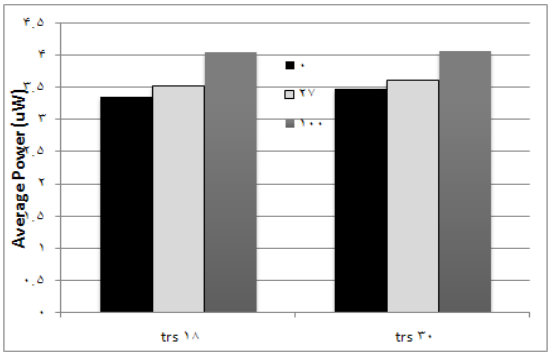
To test the protection of the changes in temperature, modeling designs are simulated in different temperatures. Figure 8(a) shows both Subtractor with various temperatures (0,27,100˚C). In summary, the delay of second design in every temperature is lower than its counterpart.

Figure 8(b) shows power consumption of both designs with 3 different temperatures.

Once the temperature raises the simulation, the results show that the propagation delay will be decreased against increasing power consumption. Figure 8(c) shows that we have the best PDP for both subtractors in temp=100˚C.Simulation results have illustrated that by rising temperature we will have better Delay and worse Power in our subtractor CNTFET designs. In the worst case (100 ˚C) in second TLS we have about 400% development in terms of power and delay than the initial plan.



(a)



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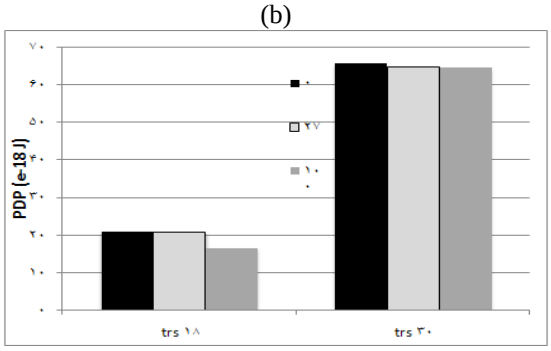

(c)

Fig. 8. (a) Transient average power of CNTFET (b) transient worse delay of CNTFET(c) Power Delay Product (PDP) of two Subtractors with different temperature (˚C).

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Figure9. Illustrates figure of inputs and output in Vdd=0.9 and in room temperature at 27˚C.

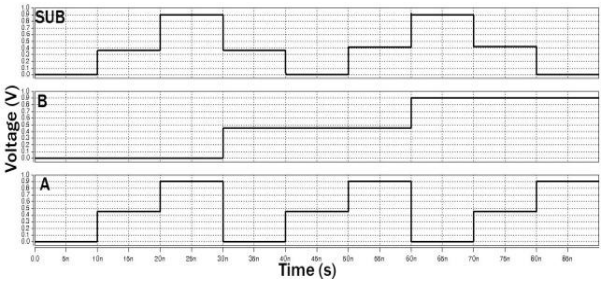

Fig.9.transient response of TLS

In our design to resolve the resistors problems, we use two CNTFET transistors. The Simulations are carried out using HSPICE with CNTFET model (Stanford University CNFET Model website)by the supply voltage at normal voltage in 0.9 V. Table 1demonstrates circuit parameter of TLS that consumes less power. As demonstrated in diagrams, the second proposed TLS has better PDP in comparison to the first TLS.

VII. CONCLUSION

In This paper we have introduced the ternary subtractor by using the entire CNTFET characteristic. Initially, we presented a novel ternary logic Subtractor (TLS) value by 30transistors with CNTFET and then the TLS by 18 transistors. Afterwards, we compared these new designs to each other. The second TLS proposed architecture shows, an average, an improvement in power-delay and it has better PDP than the first circuits. Simulation results have been presented in normal condition show that the 18 TLS circuit has more than 300% improvement in delay. Simulations are carried out using HSPICE simulator by CNTFET model for two presented designs.

REFERENCES

1. P.C. Balla, A. Antoniou, 1984. “Low power dissipation MOS ternary logic family”. In Solid-State Circuits, IEEE Journal of, Vol. 19,Issue 5:739 – 749.
2. J. Appenzeller, 2008. “Carbon Nanotubes for High-Performance Electronics—Progress and Prospect”. Proceedings of the IEEE, Volume 96, Issue 2: 201 - 211.
3. A. Rahman, J. Guo, S. Datta, M.S. Lundstrom,2003. “Theory of ballistic nano transistors”. Electron Devices, IEEE Transactions on, vol. 50,no. 10: 1853 - 1864.
4. H. Hashempour, F. Lombardi,2008. “Device Model for Ballistic CNFETs Using the First Conducting Band”. on IEEE Design &Test of Computers, Vol 25, Issue 2:178-186.
5. Synthesis, Structure Properties and Application, M.Dresselhaus, G. Dresselhaus, Ph. Avouris,2001.“Carbon Nanotubes”. Springer-Verlag, Berlin.
6. Philip G. Collins et al, 2001. “Study of carbon nanotube field effect transistor performance based on changes in gate parameters”.Phys. Rev. Lett. 86: 3128.
7. K. Maehashi, H. Ozaki, Y. Ohno, K. Inoue, K. Matsumoto, S. Seki, and S. Tagawa,2007. “Formation of single quantum dot in single-walled carbon nanotube channel using focused-ion-beam technique”. Appl. Phys. Lett.,vol. 90: 023103.
8. M. Bockrath, D. Cobden, P. McEuen, N. Chopra, A. Zettl, A. Thess, and R. Smalley,1997.“Single-electron transport in ropes of carbon nanotubes”. Science, vol. 275: 1922-1925.
9. Y. Ohno, Y. Asai, K. Maehashi, K. Inoue, and K. Matsumoto,2009.“Roomtemperature-operating carbon nanotube single-hole transistors with significantly small gate and tunnel capacitances”. Appl. Phys. Lett., vol.94: 053112.
10. S. Iwasaki, M. Maeda, T. Kamimura, Y. Ohno, K. Maehashi, and K. Matsumoto,2008. “Room-temperature carbon nanotube single-electron transistors fabricated using defect-induced plasma process”. Jpn. J. Appl. Phys., vol. 47: 2036-2039.
11. T. Rueckes, K. Kim, E. Joselevich, G.Y. Tseng, C.-L.Cheung, C.M. Lieber,2000. "Carbon nanotube based nonvolatile random access memory for molecular computing". Science, vol. 289: 94-97.
12. R. Martel, V. Derycke, J. Appenzeller, S. Wind, Ph. Avouris,2002. "Carbon Nanotube Field-Effect Transistors and Logic Circuits", in Proc. DAC 2002:94-98, June 10-14, New Orleans, Lousiana, USA.
13. A. Bachtold, P. Hadley, T. Nakanishi, C. Dekker,2001."Logic Circuits with Carbon Nanotube Transistors,"Science, vol. 294, no. 9 : 1317-1320.
14. Hurst S.L,1984. “Multiple-valued logic—Its status and its future”. IEEE Trans. Comput., vol. C-33,no. 12: 1160–1179.
15. M.Mukaidono,1986. “Regular ternary logic functions—Ternary logic functions suitable for treating ambiguity”. IEEE Trans. Comput., vol. C-35, no. 2:179–183.
16. T. Araki, H. Tatsumi, M. Mukaidono, and F. Yamamoto,1998. “Minimization of incompletely specified regular ternary logic functions and its application to fuzzy switching functions”. in Proc. IEEE Int. Multiple-Valued Logic: 289–296.
17. Raychowdhury A, Roy K, 2005 .“Carbon-Nanotube-Based Voltage-Mode Multiple-Valued Logic Design” IEEE Trans. Nanotechol., vol 4, no.2: 168-179.
18. [18] Raychowdhury A, Roy K,2007. “Carbon Nanotube Electronics: Design of High-Performance High-Performance and Low-Power Digital Circuits”. IEEE Trans. Circuits Syst. I, Reg. Papers, vol.54, no.11: 2391-2401.
19. Y. Yasuda, Y. Tokuda, S. Taima, K. Pak, T. Nakamura, and A. Yoshida,1986.“Realization of quaternary logic circuits by n-channel MOS devices”. IEEE J. Solid-State Circuits, vol. 21, no. 1: 162–168.
20. Timarchi S, Navi K,2009.“ Arithmetic Circuits of Redundant STU-RNS”. IEEE Trans, Instrum. Meas., vol 58, no 9: 2959- 2968, DOI: 10.1109/TIM.2016793.
21. Sheng Lin, Yong-Bin Kim and Fabrizio Lombardi, 2011.” A Novel CNTFET-Based Ternary Logic Gate Design”. Department of Electrical and Computer Engineering IEEE Transaction on Nanotechnology, vol. 10, NO. 2.
22. Stanford University CNFET Model website,http://nano.stanford.edu/model.php?id=23.
23. Jie Deng, H.-S.P. Wong,2007.“A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Non idealities and Its Application—Part I: Model of the Intrinsic Channel Region”. in Electron Devices, IEEE Journal of, Volume 54, Issue 12: 3186 – 3194.
24. Jie Deng, H.-S.P. Wong,2007. “A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Non idealities and Its Application—Part II: Full Device Model and Circuit Performance Benchmarking”. In Electron Devices, IEEE Journal of, Volume 54, Issue 12: 3195 – 3205.
25. Y. Li, W. Kim, Y, Zhang, M, Rolandi, D. Wang,2001. “Growth of Single-Walled Carbon Nanotubes from Discrete Catalytic Nanoparticles of Various Sizes”. J. Phys. Chem., Vol. 105:11 424.
26. Y. Ohno, S. Kishimoto, T. Mizutani, T. Okazaki, H. Shinohara,2004 .“Chirality assignment of individual single-walled carbon nanotubes in carbon nanotube field-effect transistors by micro photo current spectroscopy”. Applied Physics Letters, Vol. 84, no.8.