Analysis of Stability in Carbon Nanotube and Graphene Nanoribbon Interconnects

Sandip Bhattacharya, Subhajit Das, Debaprasad Das

***Abstract*—This paper analyzes the stability of carbon nanotube (CNT) and graphene nanoribbon (GNR) based interconnects for future VLSI technology node. We have analyzed both Bode and Nyquist stability of single-wall CNT, multi-wall CNT, GNR, and copper based interconnect systems. The stability analysis is performed for different interconnect systems for 16nm ITRS technology node. It is shown that densely packed single-wall CNT bundle based interconnect has highest gain margin for a wide range of interconnect length (1 μm to 100 μm) as compared to the other interconnect systems.**

***Index Terms*—Carbon nanotube (CNT), graphene nanoribbon (GNR), stability.**

I. INTRODUCTION

With the advancement of VLSI Technology the interconnect dimensions are reduced from micron to submicron range and submicron to nanometer range. In the nanometer regime the traditional copper based interconnects will suffer serious problems due to increased resistivity and susceptibility to electromigration. The carbon nanotube (CNT) and graphene nanoribbon (GNR) are proposed as the possible replacement for traditional copper (Cu) based interconnect systems [1]. CNT and GNR can support large current densities and have long mean free paths. In this paper we have analyzed Bode and Nyquist stabilities in different CNT and GNR interconnect systems and compared the results with that of Cu based interconnects.

The paper is organized as follows. Section II describes the formulation of transfer function of interconnects systems in s-domain. Analysis of Bode stability and Nyquist Stability is presented in Sections III and IV. The results are presented in Section V, followed by the conclusions in Section VI.

II. TRANSFER FUNCTION FORMULATION

To investigate the stability of CNT and GNR based interconnect system, we have formulated the transfer function of the interconnect system. We have modeled the interconnect system by a bundle of single-wall CNT, multi-wall CNT, and GNR. The dimensions of the interconnect are obtained from the ITRS corresponding to 16 nm technology node. Fig. 1 illustrates the *RLC* network interconnect systems. The *RLC* equivalent circuit model is constituted with series connected resistance (*R*), inductance (*L*), and capacitance (*C*).

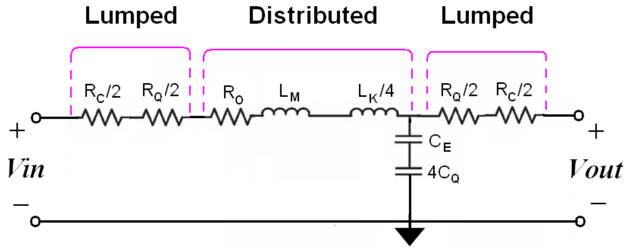

Fig. 1: Equivalent circuit of CNT/GNR interconnects.

The transfer function of the *RLC* circuit is given by

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{(LCs^2 + RCs + 1)} \quad (1)$$

where R is the series combination of imperfect contact resistance (R_C), quantum resistance (R_Q), and ohmic resistance (R_O), L is the series combination of kinetic inductance ($L_K/4$) and magnetic inductance (L_M), and C is the series combination of electrostatic capacitance (C_E) and quantum capacitance ($4C_Q$). The *RLC* parameters are obtained from [2–4] for SWCNT bundle, MWCNT and GNR based interconnects for 16 nm technology node. Substituting the *RLC* values into (1) we have obtained the transfer function of the interconnect system.

III. BODE STABILITY ANALYSIS

We have used the stability analysis model as shown in Fig. 2 [5]. A single horizontal interconnect segment connected with load and driver is considered. We have applied a step input to the system to check the step response of the system. To investigate the stability of the system we have considered three different conditions for stability: (i) whether the system is over damped, (ii) under damped, or (iii) critically damped. Generally damping condition is determined by damping ratio (ζ). If $\zeta > 1$, the system is over damped, if $\zeta = 1$, the system is critically damped, and if $0 < \zeta < 1$, the system is under damped.

Consider an under damped system and an over damped system with the same un-damped natural frequency, but damping ratios ζ_u and ζ_o, respectively. It is shown that the under damped system is more stable and faster than the over damped system if and only if [5]

Manuscript received on January, 2013.
Sandip Bhattacharya, Dept. of Electronics and Communication Engineering, Bengal College of Engineering and Technology, Durgapur, India.

Subhajit Das, Dept of Electronics and Communication Engineering, ADAMAS Institute of Technology, Barasat, India.

Debaprasad Das, Dept. of Electronics and Communication Engineering, Meghnad Saha Institute of Technology, Kolkata, India.

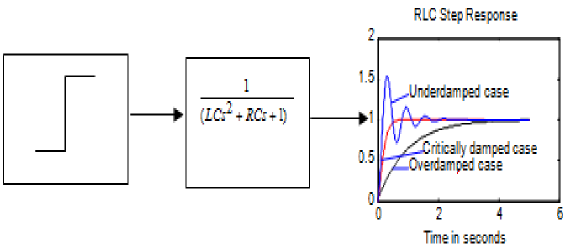

Fig. 2: Step response of an RLC network.

$$\zeta_o > \frac{\zeta_u^2 + 1}{2\zeta_u} \tag{2}$$

In this work we have studied stability of the interconnect system by increasing the length of both interconnect from 1 µm to 100 µm. As the length of the interconnect is increased the switching delay of the *RLC* network is also increased. Thus the system becomes over damped and it is said to be sluggish system and it reaches to the unstable condition [5].

We have analyzed the Bode stability using MATLAB version 10. In Bode plot, the magnitude (in dB) and phase (in deg.) are plotted along the Y-axis with respect to frequency along the X-axis. Using MATLAB programming we have calculated the gain margin (GM) and phase margin (PM) of the interconnect system. Phase margin is basically the difference between -180^o and the phase at 0 dB cross point of the gain curve. Gain margin is just the amount of gain that can be added to move to the 0 dB line at the phase crossover frequency. The system becomes more stable if the GM and PM increase [6].

IV. Nyquist Stability Analysis

Nyquist stability analysis technique is implemented on the same model for further verification. Using this stability analysis we can further verify that our previous model gives us same response or not. A Nyquist plot is a parametric plot of a transfer function used in automatic control and signal processing. The most common use of Nyquist plots is for assessing the stability of a system with feedback. In Cartesian coordinates, the real part of the transfer function is plotted on the X axis. The imaginary part is plotted on the Y axis. The frequency is swept as a parameter, resulting in a plot per frequency. Alternatively, in polar coordinates, the gain of the transfer function is plotted as the radial coordinate, while the phase of the transfer function is plotted as the angular coordinate [7].

Assessment of the stability of a closed-loop negative feedback system is done by applying the Nyquist stability criterion to the Nyquist plot of the open-loop system (i.e., the same system without its feedback loop). This method is easily applicable even for systems with delays and other non-rational transfer functions, which may appear difficult to analyze by means of other methods. Stability is determined by looking at the number of encirclements of the point at (–1,0). Range of gains over which the system will be stable can be determined by looking at crossing of the real axis.

The Nyquist plot can provide some information about the shape of the transfer function. For instance, the plot provides information on the difference between the number of poles and zeros of the transfer function [8] by the angle at which the curve approaches the origin.

V. Stability Analysis Results

In this work we have varied the length of the CNT and GNR interconnects from 1 µm to 100 µm for 16 nm technology node and generated various Bode plots and Nyquist plots. From the Bode plot plots we have studied the relative stability of the system shown in Figures 3 to 9. Table I shows the gain margin and phase margin of different interconnect systems.

From Nyquist diagram Figures 11 to 17, we also studied the relative stability of the GNR, CNT and Copper interconnects. Here Most of the interconnects shows stability because there is no pole in right hand side of the S Plane and also the number of encirclements of the point present at (–1, 0). Beyond the -1 of the real axis the system will become unstable. But our analysis shows that all encircle pass through the origin and overlapped for SWCNT bundle with densely packed CNTs with different interconnects length shown in Figure 11. So stability is higher than other interconnects in SWCNT bundle with densely packed interconnects. But in case of GNR interconnects it shows poor stability when length is equal to 1µm, 5 µm, and 10 µm. If we want to increase the interconnect length of GNR from 50 µm to 100 µm it shows some stability because the encirclements of the contour presents between -1 to 0 in the real axis.

TABLE I
GAIN MARGIN AND PHASE MARGIN OF DIFFERENT INTERCONNECT SYSTEMS
GAIN MARGIN (GM) IN dB, PHASE MARGIN (PM) IN Degree.

Interconnect Length (µm) →	1		5		10		50		100	
Types of Interconnect ↓	GM	PM	GM	PM	GM	PM	GM	PM	GM	PM
SWCNT bundle densely packed	293	90	283	90	280	90	277	90	277	90
SWCNT bundle sparsely packed	270	90	258	90	253	90	245	90	243	90
Single MWCNT	244	90	232	90	228	90	223	90	222	90
MWCNT bundle of 2 MWCNTs	244	90	232	90	228	90	223	90	222	90
MWCNT bundle of 8 MWCNTs	248	90	238	90	235	90	231	90	231	90
Graphene Nanoribbon (GNR)	250	90	245	90	244	90	243	90	225	90
Copper (Cu)	285	90	282	90	281	90	279	90	278	90

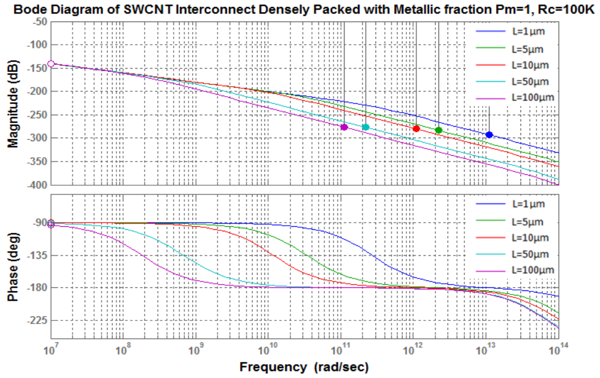

Fig. 3: Bode plot for SWCNT bundle with densely packed CNTs.

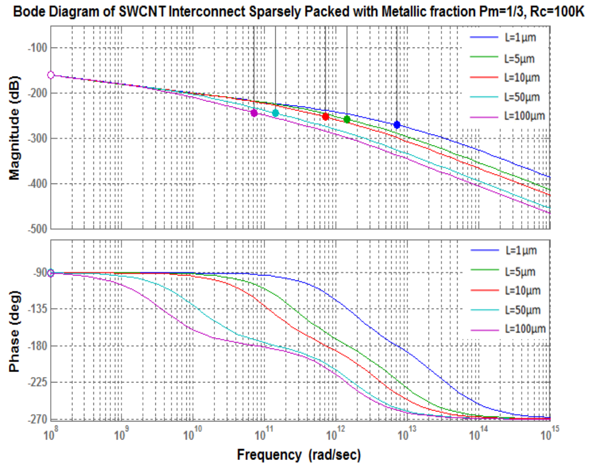

Fig. 4: Bode plot for SWCNT bundle with sparsely packed CNTs.

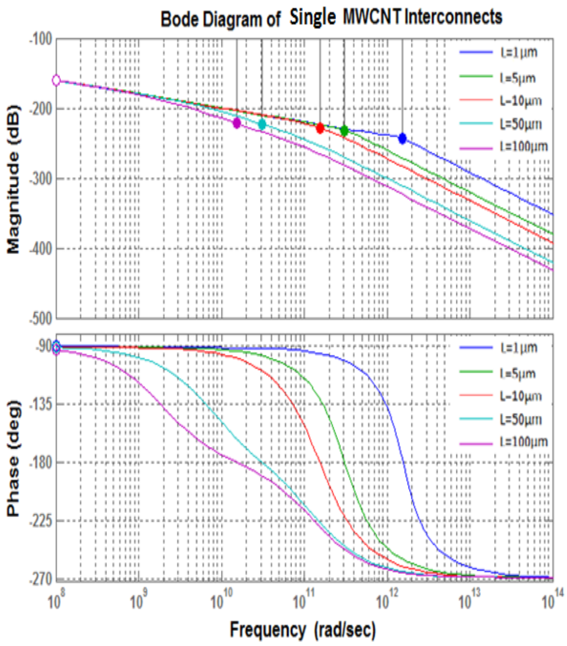

Fig. 5: Bode plot for single MWCNT.

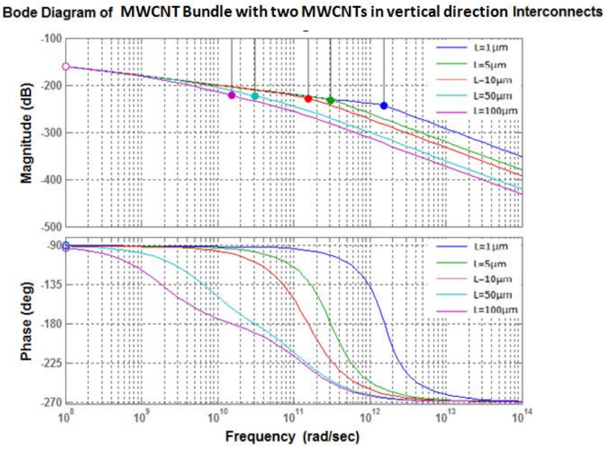

Fig. 6: Bode plot for double MWCNT.

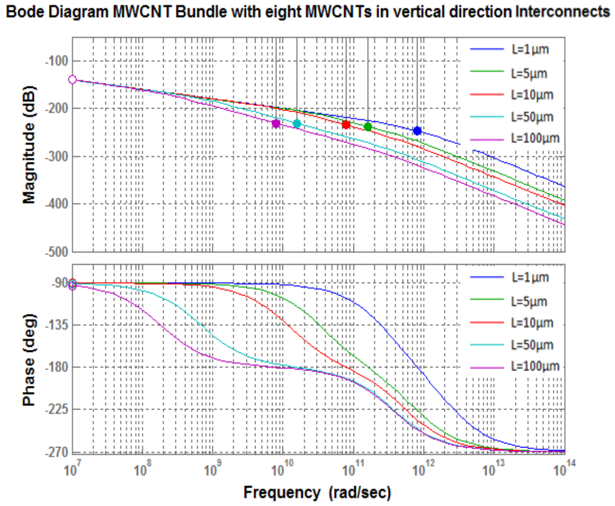

Fig. 7: Bode plot for MWCNT bundle with eight MWCNTs.

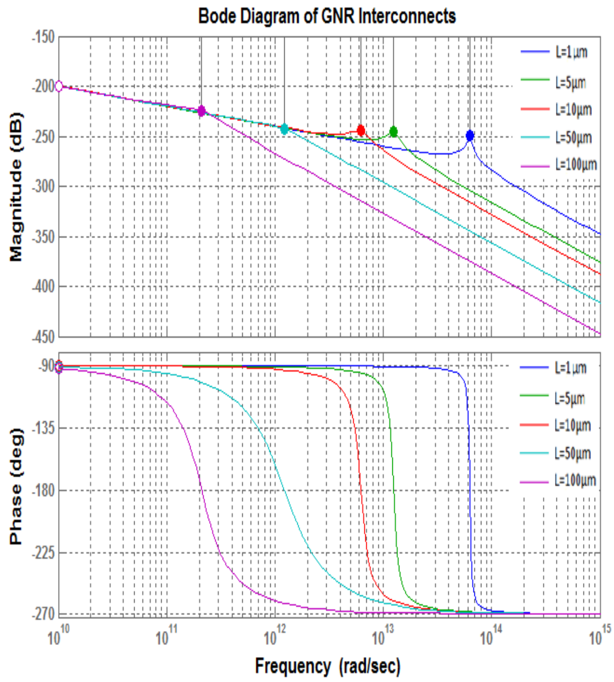

Fig. 8: Bode plot for GNR interconnect.

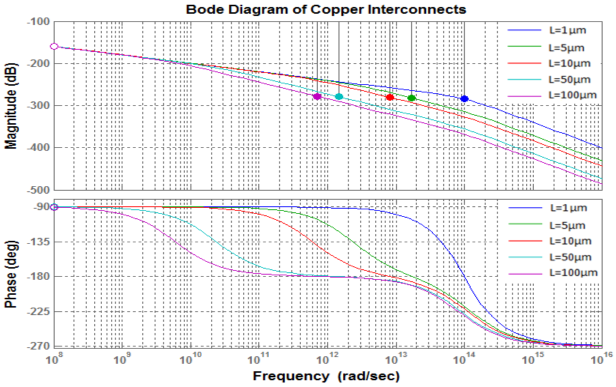

Fig. 9: Bode plot for copper interconnect.

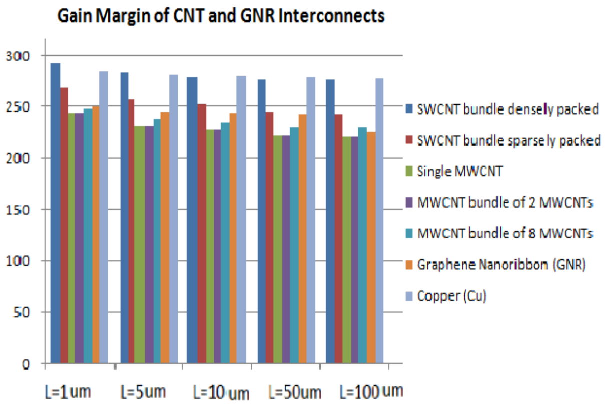

Fig. 10: Experimental data for GNR, CNT and Copper interconnects.

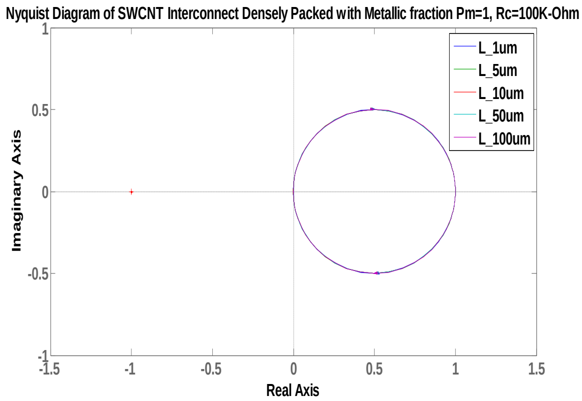

Fig. 11: Nyquist plot for SWCNT bundle with densely packed CNTs.

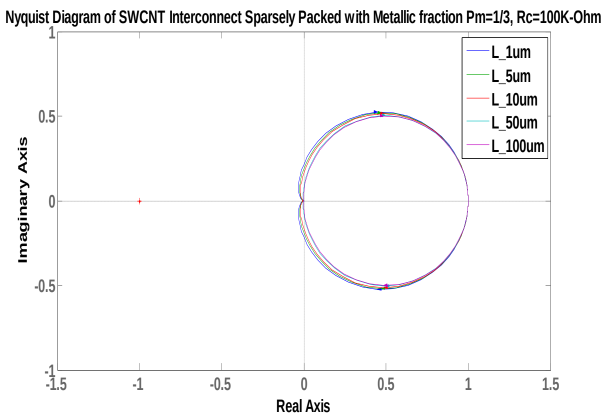

Fig. 12: Nyquist plot for SWCNT bundle with sparsely packed CNTs.

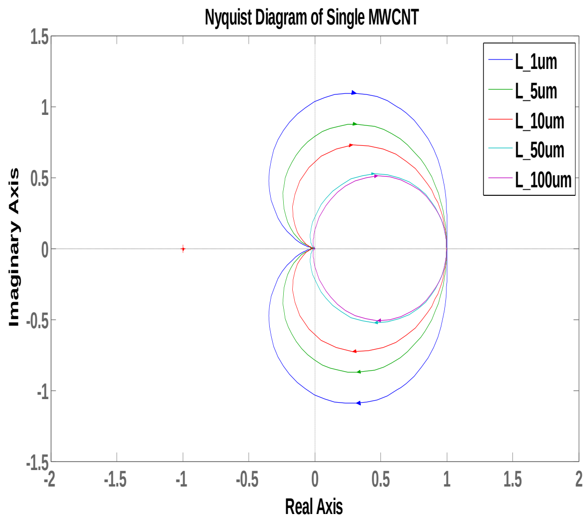

Fig. 13: Nyquist plot for single MWCNT.

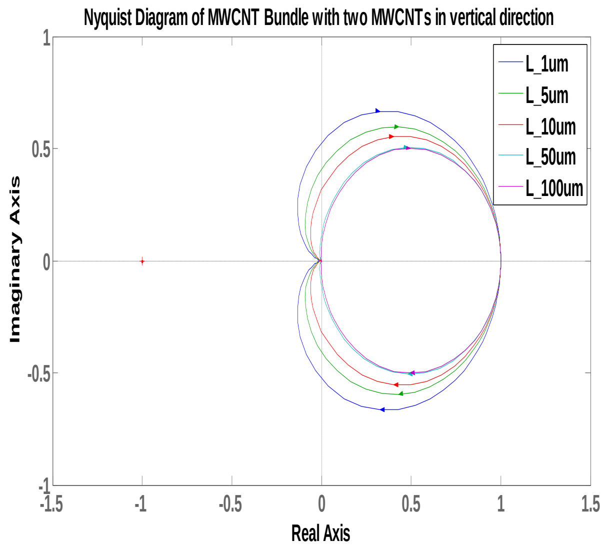

Fig. 14: Nyquist plot for MWCNT Bundle with two MWCNTs in vertical direction.

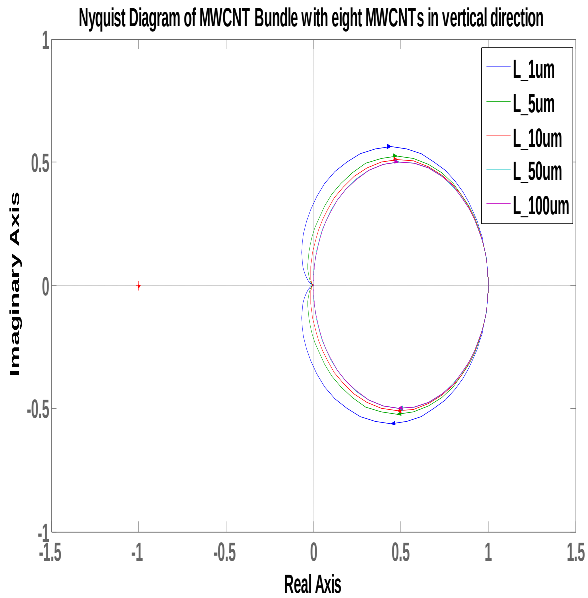

Fig. 15: Nyquist plot for MWCNT Bundle with eight MWCNTs in vertical direction.

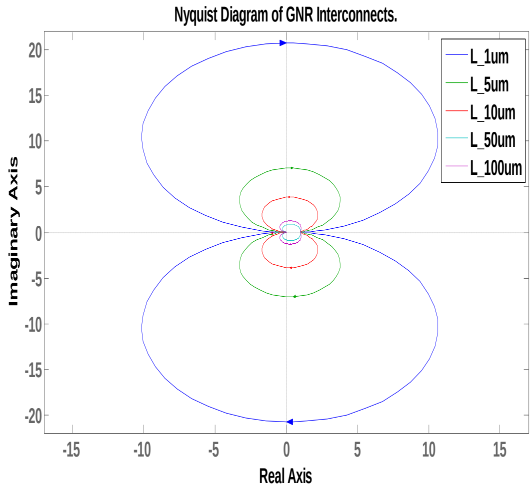

Fig. 16: Nyquist plot for GNR interconnects

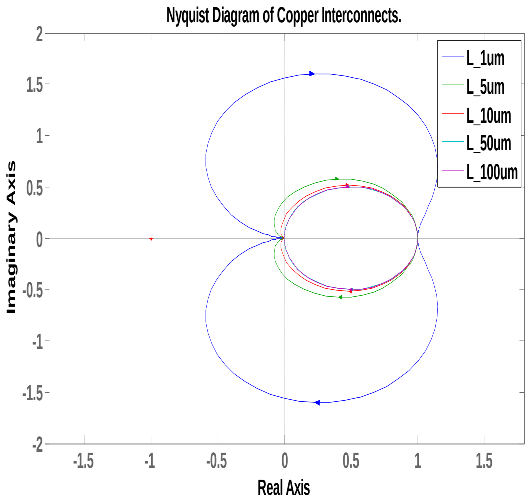

Fig. 17: Nyquist plot for copper interconnect.

VI. CONCLUSIONS

In this paper we have investigated the relative stability of carbon nanotube and graphene nanoribbon interconnects for 16 nm ITRS technology node. From the Bode plots, we have shown that as the length of interconnects increases, the relative stability decreases. This is due to fact that, the increase in interconnect length of the system will cause increased interconnect delay. Thus, the step response of the system tends to become more sluggish in nature (over damped), and hence the system becomes more unstable.

REFERENCES

[1] International Technology Roadmap for Semiconductors (ITRS) reports, 2006. [Online]. Available: http://www.itrs.net/reports.html

[2] Debaprasad Das and Hafizur Rahaman, "Crosstalk overshoot/ undershoot analysis and its impact on gate oxide reliability in multi-wall carbon nanotube interconnects", *Journal on Computational Electronics, Springer*, vol. 10, no. 4, pp. 360-372, Dec. 2011.

[3] Debaprasad Das and Hafizur Rahaman, "Analysis of Crosstalk in Single- and Multiwall Carbon Nanotube Interconnects and Its Impact on Gate Oxide Reliability", *IEEE Transactions on Nanotechnology*, vol. 10, no. 6, Nov. 2011.

[4] Debaprasad Das and Hafizur Rahaman, "Crosstalk and Gate Oxide Reliability Analysis in Graphene Nanoribbon Interconnects", *in Proc. 2nd International Symposium on Electronic System Design* (*ISED*), 19-21 Dec. 2011, pp. 182-187.

[5] Sandip Bhattacharya, Subhajit Das, Debaprasad Das, "Analysis of Stability in Carbon Nanotube Interconnects", *in Proc. National Conference on Recent Advances in Applied Mathematics* (*NCRAAM*), 18th Feb. 2012, pp. 34-39.

[6] R. C. Dorf, R. H. Bishop, Modern Control System, 11th Ed., Englewood Cliffs, NJ: Prentice-Halls, 2008.

[7] http://en.wikipedia.org/wiki/Nyquist_plot.

[8] http://www.facstaff.bucknell.edu/mastascu/econtrolhtml/Freq/Freq6.html

Sandip Bhattacharya was born in Pandaveswar, Burdwan, West Bengal, India, on July 21st, 1983. He received the B.E. degree in Electronics and Communication Engineering from University Institute of Technology, University of Burdwan, India in 2006 and the M.Tech. degree in Electronics and Communication Engineering (Embedded Systems) from Haldia Institute of Technology, in 2011. From 2006 to 2009, he was a Software Engineer in Indus net Technology, Salt-Lake Kolkata, India. He joined the Department of Electronics and Communication Engineering, Bengal College of Engineering and Technology, Durgapur, India in 2011, where he is currently an Assistant Professor. His research interests include VLSI design, digital CMOS logic design, and modeling of nanoelectronic devices and interconnects, FPGA based application development.

Subhajit Das was born in Diamond Harbour, South 24 pgs, West Bengal, India, on December 3rd, 1981. He received the B.Tech degree in Electronics and Communication Engineering from Kalyani Govt. Engineering College, Kalyani, India in 2006 and the M.Tech degree in Electronics and Communication Engineering (Embedded Systems) from Haldia Institute of Technology, in 2011. From 2006 to 2008, he was a Senior Project Engineer at the embedded systems research & development section, Wipro Tech., Bangalore, India. Presently he is working in the Department of Electronics and Communication Engineering, ADAMAS Institute of Technology, Barasat, as an Assistant Professor. He also contributed as guest lecturer in University Institute of Technology, Burdwan, India. His research interests include VLSI design, digital CMOS logic design, and modeling of nanoelectronic devices and interconnect.

Debaprasad Das was born in Haria, Purba Medinipur, India, on May 10, 1975. He received the B.Sc. (Hons.) in Physics in 1995, B.Tech. in Radio Physics and Electronics in 1998, and M.E. in Electronics and Telecommunication Engineering in 2006 degrees from the Vidyasagar University, University of Calcutta, and Jadavpur University, respectively. He was with the ASIC Product Development Centre, Texas Instruments, Bangalore, as a senior engineer from 1998 to 2003. He joined the Dept. of Electronics and Communication Engineering, Meghnad Saha Institute of Technology, Kolkata, in 2003, where he is currently an Assistant Professor. He is also working for the Ph.D. degree at School of VLSI Technology, Bengal Engineering and Science University, Shibpur. He has authored or co-authored several research papers in National and International Journals and Conferences. He is author of the book *VLSI Design* (New Delhi: Oxford University Press, 2010). He has also authored two books published by Lambert Academic Publishing, Germany. His research interests include VLSI design, developing of EDA tools for interconnect modeling, analyzing crosstalk and reliability, digital CMOS logic design, and modeling of nanoelectronic devices and interconnects. Mr. Das received gold medal from Vidyasagar University in 1997 for ranking first in the undergraduate degree. He received First Place Award in PhD forum at VDAT 2012.